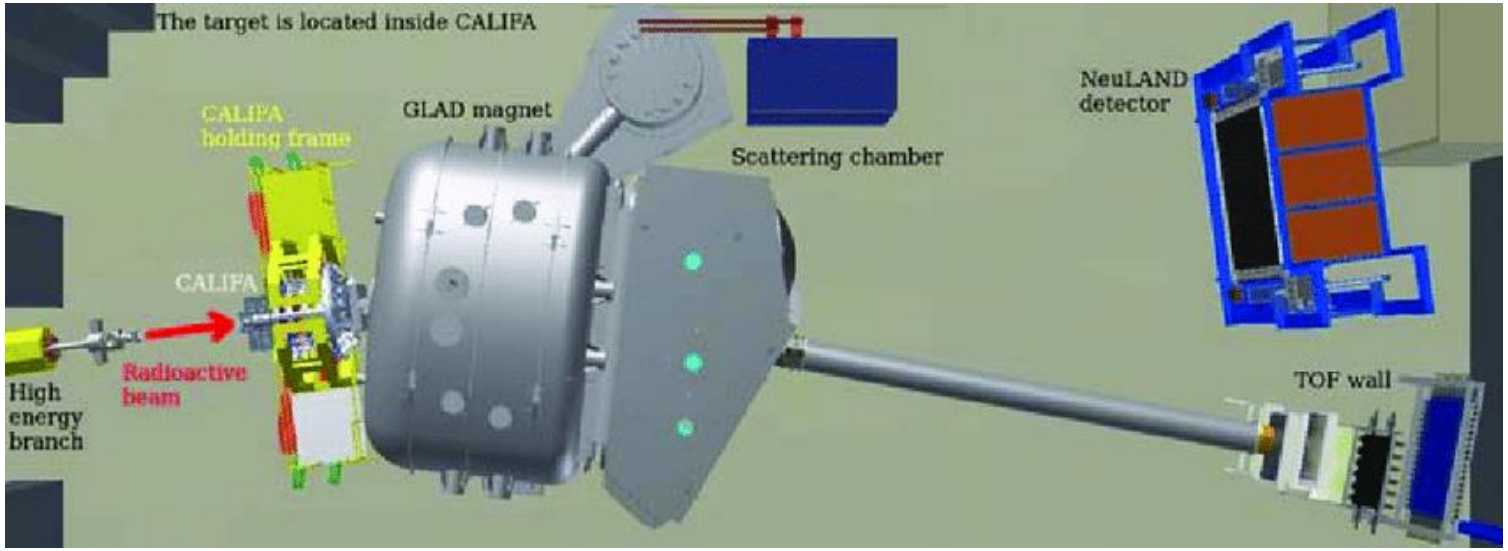
Detectors and readout at R3B, GSI

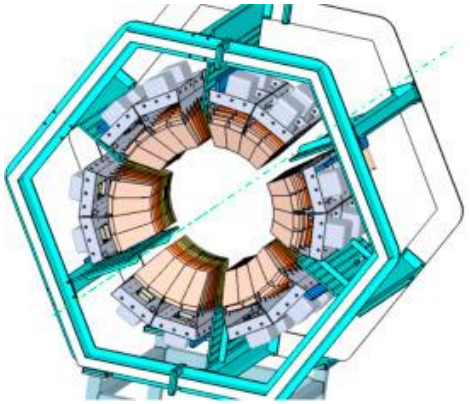
Hans T. Törnqvist, Technische Universität Darmstadt + GSI Darmstadt
Oleg Kiselev, GSI Darmstadt

R3B – Reactions with Relativistic Radioactive Beams

- Inverse kinematics setup at **GSI**, Germany
- Energies **~ 100 MeV – 1 GeV**
- **~ 20 m** start detector ↔ ToF and neutron detectors, big superconducting dipole magnet in the middle
- Experimental collection currently confined in one cave, sometimes take a few channels up-streams via long cables (*ugh*)



Detector types



- Lots of **plastic scintillators + PMT:s**
- **Silicon** detectors
- **Crystal scintillators** for gamma/proton
- **Gaseous chambers**
- Currently **4000-5000** channels (will grow a lot)
- Many **time** channels, but some **energy** readout necessary

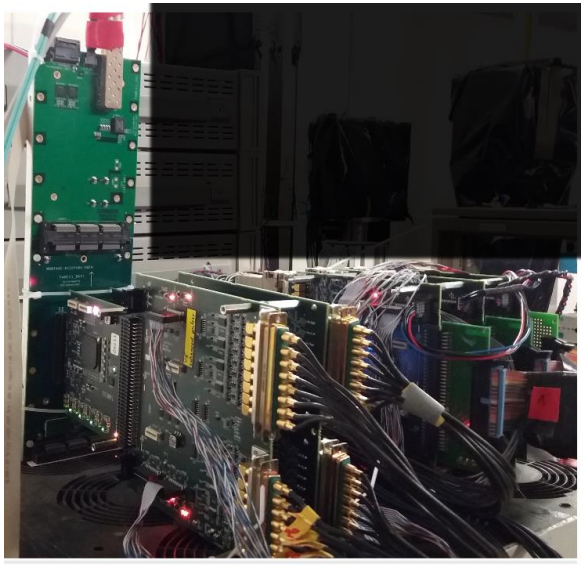
DAQ and readout electronics

- **GSI MBS**, **trigger-based** throughout the R3B cave
- Some timestamped (**White Rabbit** (**WR**)) systems
  - Also **ratatime**, light-weight single-wire serial protocol, used in **TRLO II** firmware for the FPGA-based logic module[1]
- **FPGA TDC:s** for **~ 10 ps** times and **time-over-threshold** (**ToT**)
- **VME** use diminishing**, optical PC** readout growing
  - **GOSIP**, in-house protocol
- Slow control, clock, triggering over electrical **I2C** and **LVDS**
  - Source of most hickups/re-initializations

1 *http://fy.chalmers.se/~f96hajo/trloii/*

Electronics show-case: TAMEX

- Most # ch at R3B
  - **NeuLAND** neutron detector, currently **1600** channels, in the end **6000**
  - Start detector + ToF wall **~ 200** channels
- **FPGA TDC**, **~ 10 ps** times of edges at discrimination crossings, **ToT** offline
  - FPGA driven by common **LVDS clock**
  - Talks **GOSIP** over optical to **PEX PCIe** card
- **FQT** frontend discriminates and **collects trigger**
  - Talks **I2C** over **TRIPLEX**
- Currently trigger-based

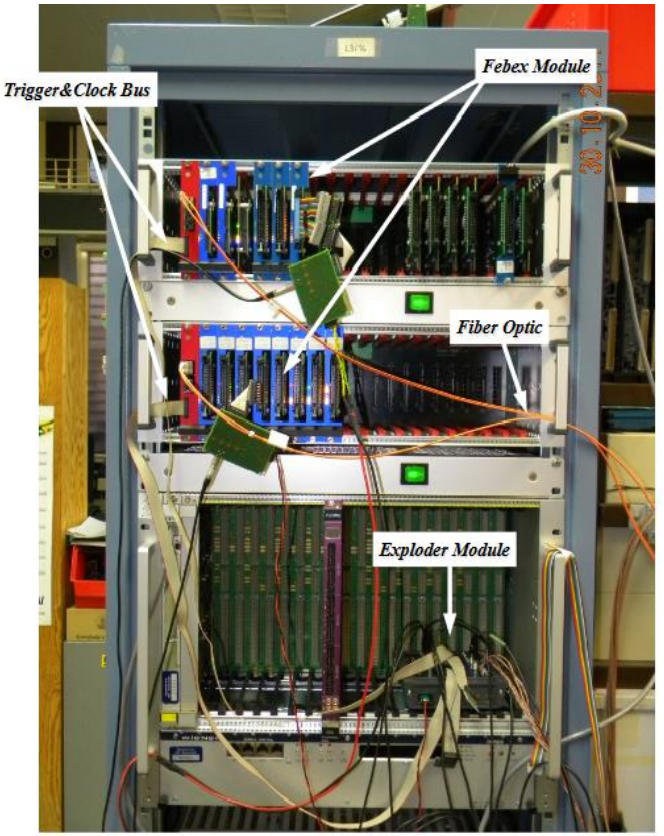


Electronics show-case: TAMEX

- **~ 60 EUR/ch**
- TAMEX ↔ PEX **optical**, FQT inputs galvanically **isolated**, most other electrical
- Best performance case:
  - 1 card = 16 ch, 1 PEX input, 1 PC → **30 kHz**
- Current **NeuLAND** performance case:
  - 104 cards = 1600 ch (some unused), 1 PEX input, **4 PC:s → 13 kHz**

Other show-cases, condensed

- **GSI Clock TDC**
  - **~ 200 ps** FPGA TDC, 128 ch/board
- **GSI FEBEX**
  - **50 MHz** sampling ADC
- All infrastructure very similar to TAMEX
  - Trigger-based
  - Readout over optical, electrical clock + trigger
- **Fast** sampling ADC for **PSA** still undecided
- Some timestamped legacy systems to be phased out



Future plans

- **1: Near-term: Keep triggered mode**
  - Lots of infrastructure in place
  - Trigger-less capable electronics can often run triggered
- **2: Long-term: Trigger-less mode**
  - Nearline event reconstruction should do a better job than online analog trigger
  - Micro-structure of beam from the accelerator difficult for good old trigger-based

Interests

- Let’s get it out of the way: money...
- “Good enough” **<= 10 ps** time resolution but CERN PicoTDC ASIC (3 ps bin, 64 ch, 3-5 CHF/ch) is an interesting alternative
- Multi-level **ToT**?
  - I.e. many discrimination levels, corresponding lead/trail
- **QDC piggy-back** on front-end?
  - Other solutions for charge/energy?
- **Triggered;** Region Of Interest (**ROI**)
- **Free-running;** time-stamped hits dumped on the net
  - **WR**, **ratatime**, whatever if open source
- Lots of optical cables, few electrical

The end

- Interesting good-looking development, would have loved to attend, but I have to help with on-site beam-time preparations :)

  / Hans T