iFTDC Architecture

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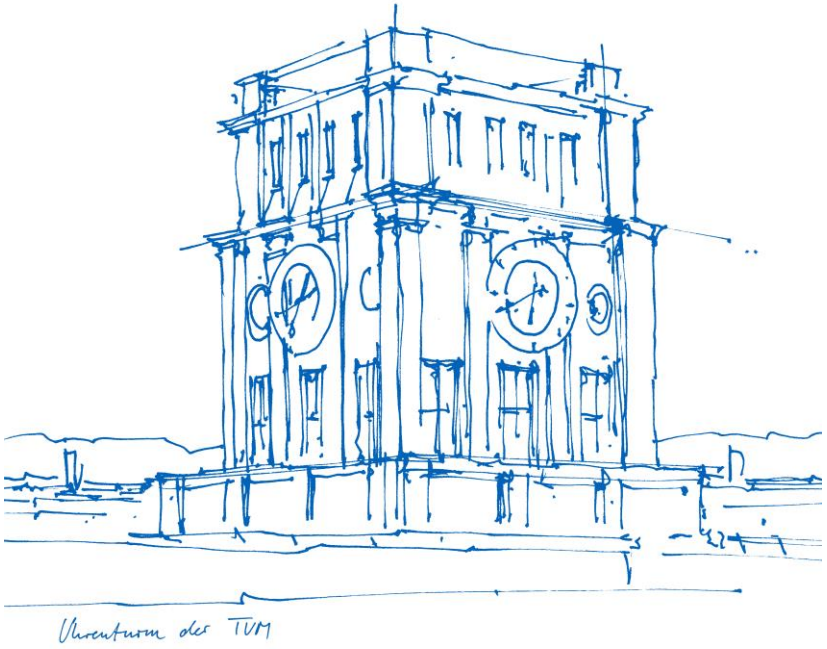
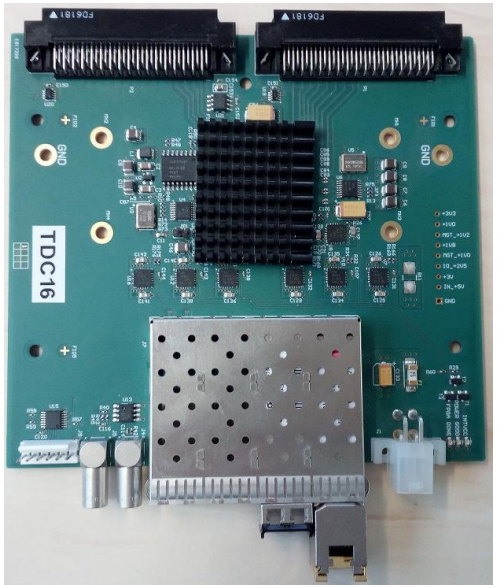


iFTDC

Specification

- ARTIX7 FPGA XC7A-35
- 64 channels,
- Programmable signal edge or both edges
- **Bin size : 1 ns, 0.5 ns, 0.25 ns (32 channels)**
- **Time resolution : 300ps, 170 ps, 10 ps**
- **Differential nonlinearity : 10%, 20%, 40%**
- **Trigger less capable data flow**

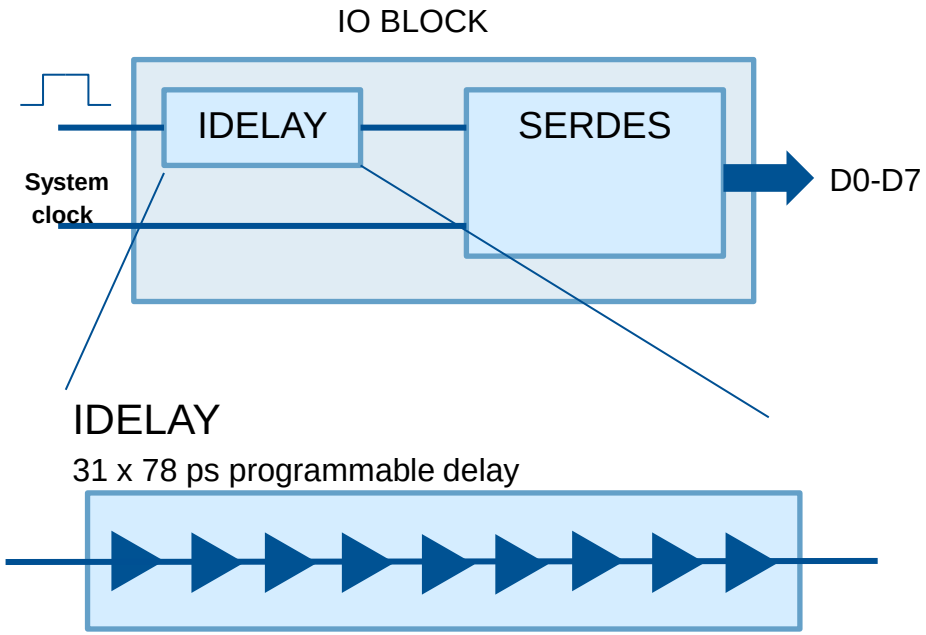


Applications

- MWPC(tested), Drift Chambers
- Scintillation Counters with limited requirements for time resolution

Time Measurement in FPGA

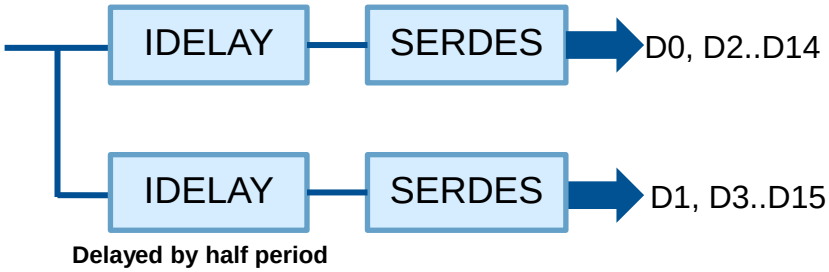
Infrastructure for serial data transmission is built-in in IO blocks of modern FPGAs



System clock maximum frequency 600 MHz

- DDR mode => 1200 Mbps => 0.84 ns bin
- QDR mode => 2400 Mbps => 0.42 ns bin

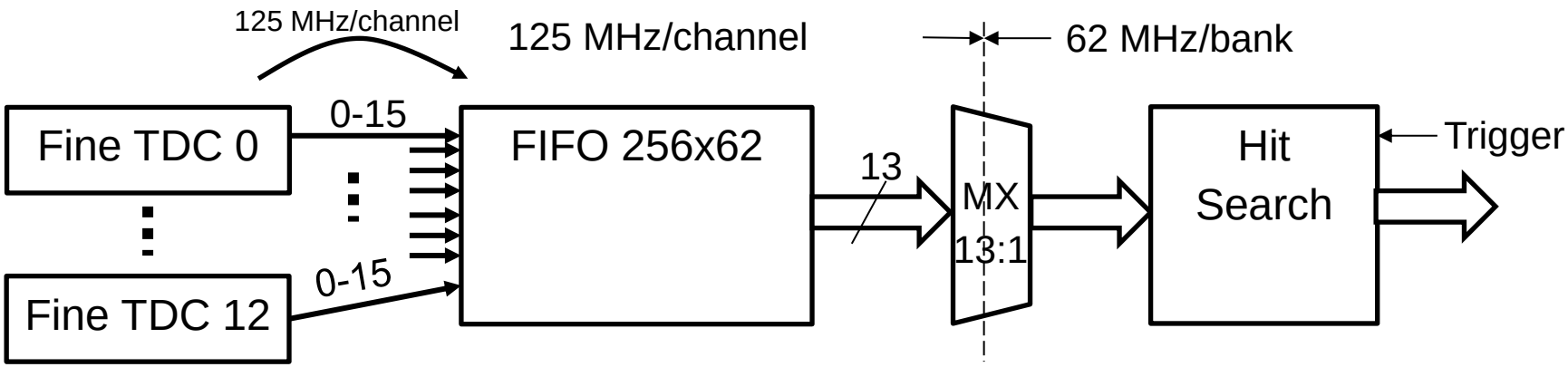
Two SERDES per channel:



Time resolution limitations :

- Fixed tap delay of 76 ps increases differential nonlinearity
- Internal Clock jitter performance is 90 ps

iFTDC Bank Architecture



Double pulse resolution 16 ns

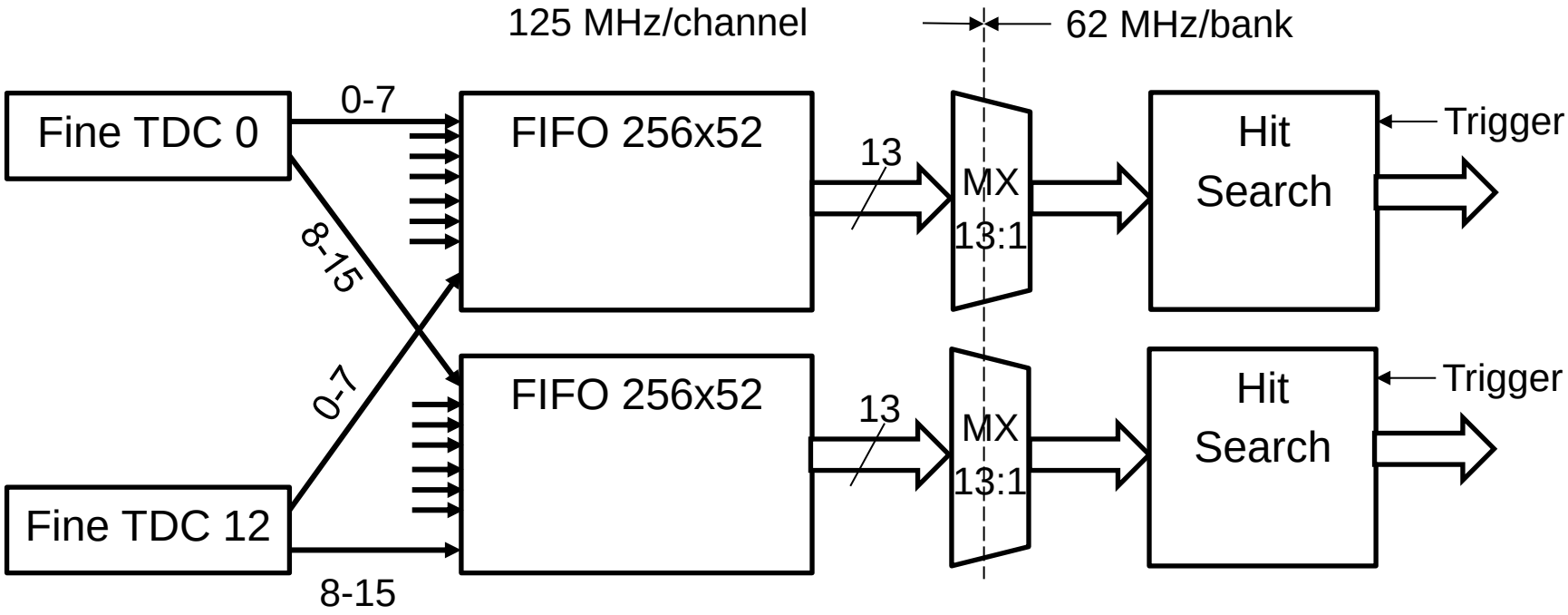
Hit search supports overlapping triggers i.e. dead time less

Hit rate performance is limited by Hit search algorithm to 60 Mhits/s/bank

Hit rate performance examples

- 13 channels/bank => 5 MHz/channel
- 4 channels/bank => 15 MHz/channel
- 1 channel/bank => 62 MHz/channel

iFTDC Bank Architecture

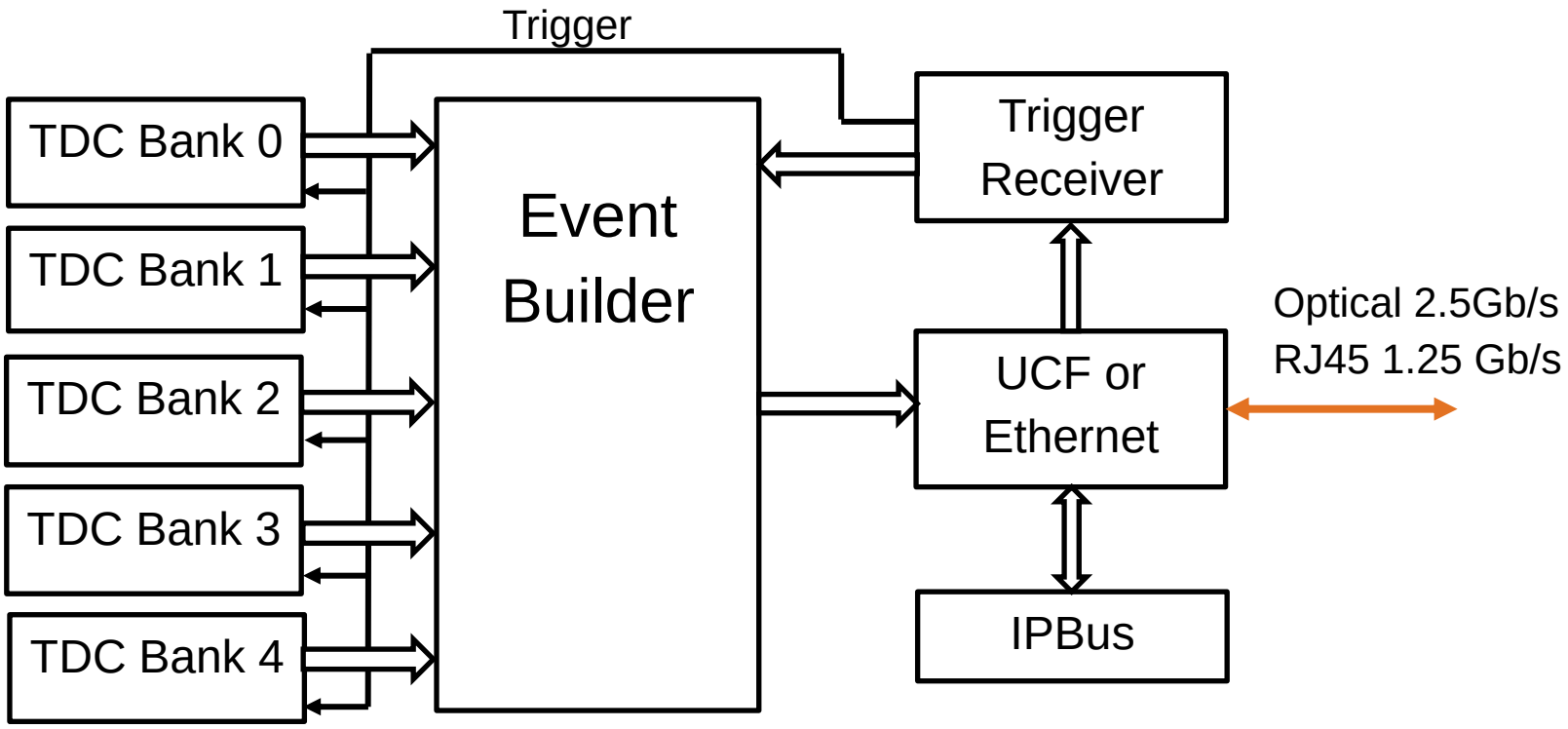


Double Hit resolution 8 ns

Hit rate performance examples

- 13 channels/bank => 10 MHz/channel
- 4 channels/bank => 30 MHz/channel
- 1 channel/bank => 120 MHz/channel

iFTDC Architecture



Data Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Number of 32-bit words in this frame [30:0]																														
1	Trigger number [30:0]																														
1	Trigger time [30:0]																														
If channel is configured for single edge detection:																															
1	Channel ID [6:0]							Coarese time [23:4]																				Fine t [3:0]			
...																															
If channel is configured for both edge detection:																															
1	Channel ID [6:0]							Coarese time [23:4]																				Ft [3:1]			x
...																															
1	CRC [30:0]																														

Table 1: Output frame format. x is 1 for a rising edge and 0 for a falling edge

CEDAR Read Out

- CEDAR is equipped with 8 MPMTs i.e. 64 channels
- 4 iFTDC modules
- 16 channels per module and it was expected to have not more than 2 channels per bank

Observed problems

- No Data from one or more TDCs. Problem occurred very often
  - Caused by too big event size, which exceeded 100 hits/event – too high rate
  - No possibility to measure real hit rate

- Wrong hit timing
  - Problem induced by radiation, required reloading FPGA

Origin of problems:

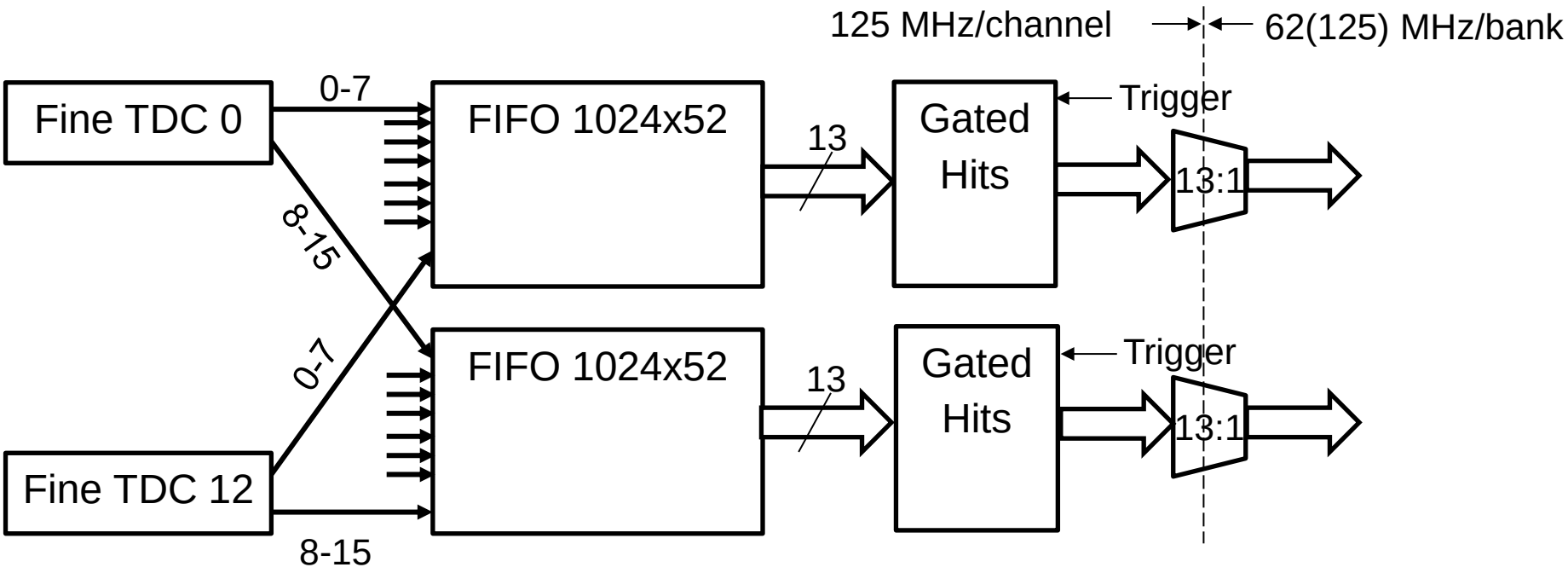
- Wrong TDC interconnection => 3 channels/bank
- Hit rate per channel exceeded 10MHz for some channels

Improvement of iFTDC Firmware

- Implementing scalers for every channels accessed via IPBus
- It turned out to be very convenient feature for detector calibration and monitoring

Firmware architecture was changed to increase significantly hit rate capability:

- Hit FIFO depth increased to 8 us to compensate trigger latency
- Delayed hits are gated by trigger signal and only afterwards they are multiplexed
- No sharing hits between consecutive events => dead time == gate length was about 100 ns

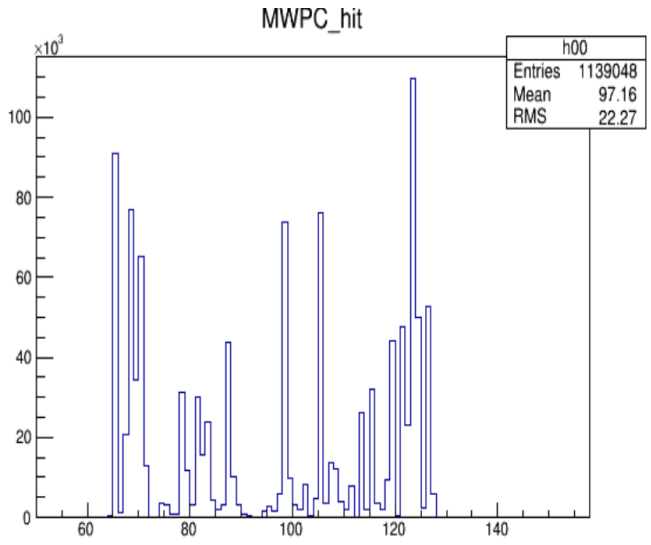


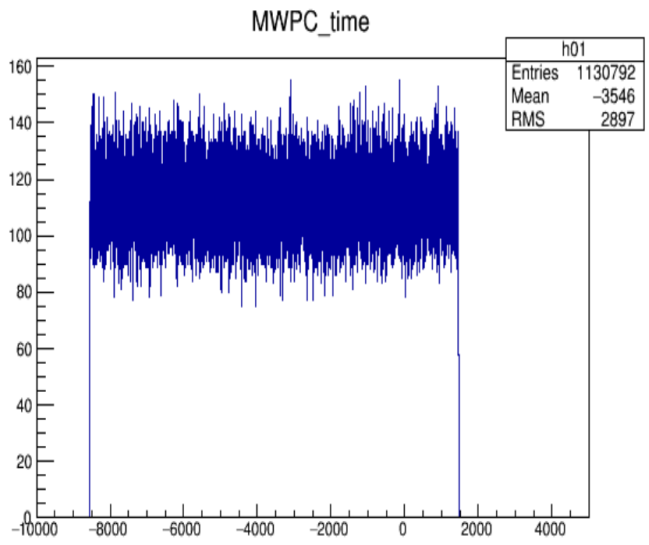
Test of iFTDC in Trigger less Mode

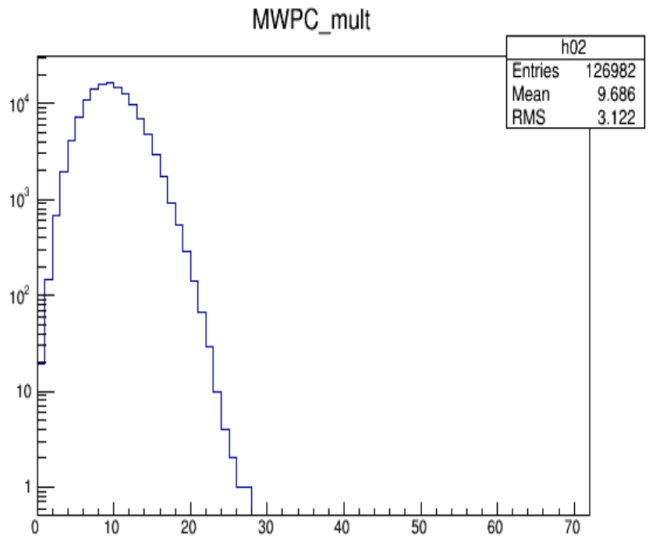
Test setup

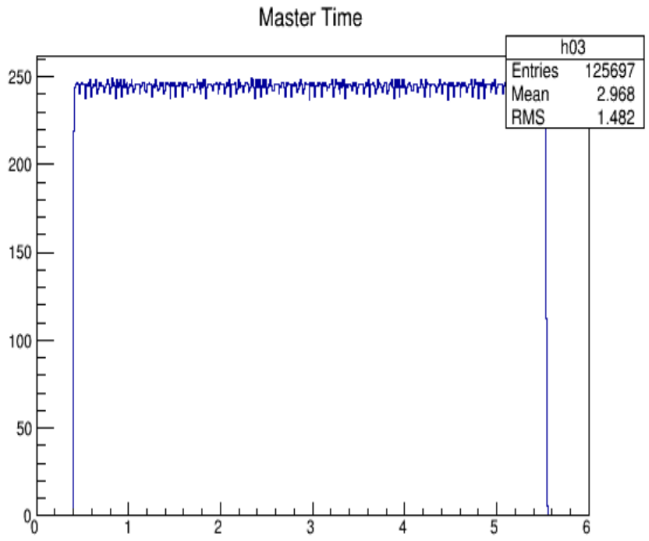
- 3 iFTDC cards were installed on MWPC PA06X;
- 4 Readout Engines were used for this test;
- Recording enabled (run # 287544);
- TCS controller generated triggers at time intervals of 10μs i.e. 100kHz;
- iFTDC settings :
  - trigger latency 10μs
  - Trigger window 10us -16 ns;
- Thresholds set to 3fC that it generated ~10 hits per each 10μs time slice (~65 bytes/slice or ~6.5MB/s);
- Only one DAQ multiplexer was used with connected SrcID 2, 84 and 459(iFTDC) (total event size was ~420 bytes);

Test of iFTDC in Trigger less Mode (2)









iFTDC Experience

- SERDES based TDC have precision down to 150 ps with 20% nonlinearity
- To precision below 100 ps one shall use alternative FPGA implementation or TDC ASIC
- Hit rate measurement via slow control is a powerful feature
- UCF protocol allows to use single fiber for data transmission, time/trigger distribution and slow control.
- UCF worked quite well but there are still one issues. Sometimes links do not come up after power up or reconnection
- Possibility to provide lab version with Ethernet protocol

- To design new front-end card one would need existing IP cores IPBus, UCF, Ethernet, TCS Receiver => COMPASS++ FrontEnd Frame Work
- Currently supported FPGAs : Virtex6 and Artix7. Kintex UltraScale will be next

THANK YOU