SRS VMM:
A next generation generic readout system

Michael Lupberger (CERN)

COMPASS DAQFEET, Garching, 12.02.2019

Outline

Introduction: What is SRS?

VMM3a ASIC - features – known issues

VMM integration in SRS

Status and applications

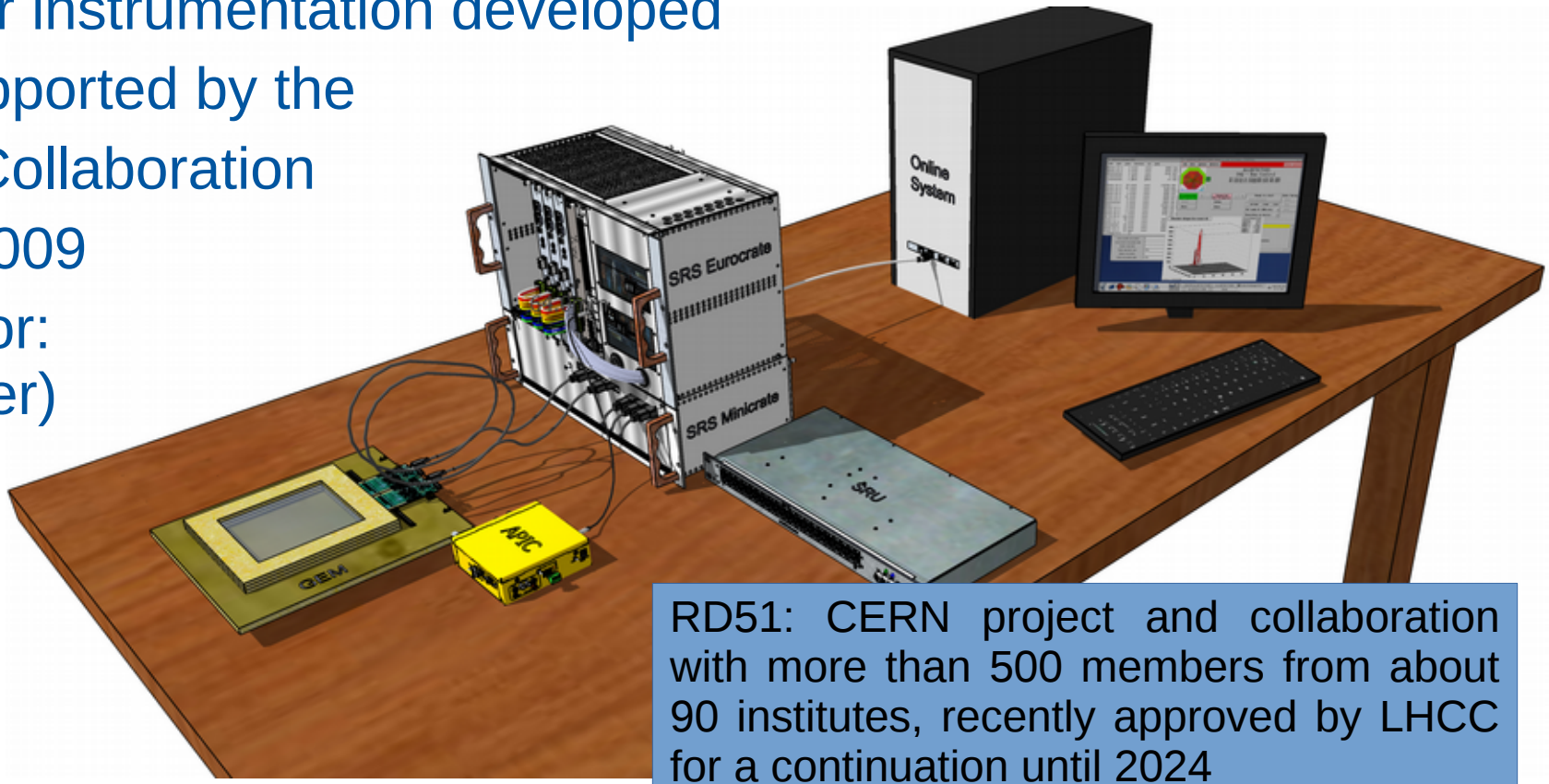
Conclusion

(Personal) ideas for the future of SRS

Introduction: What is SRS?

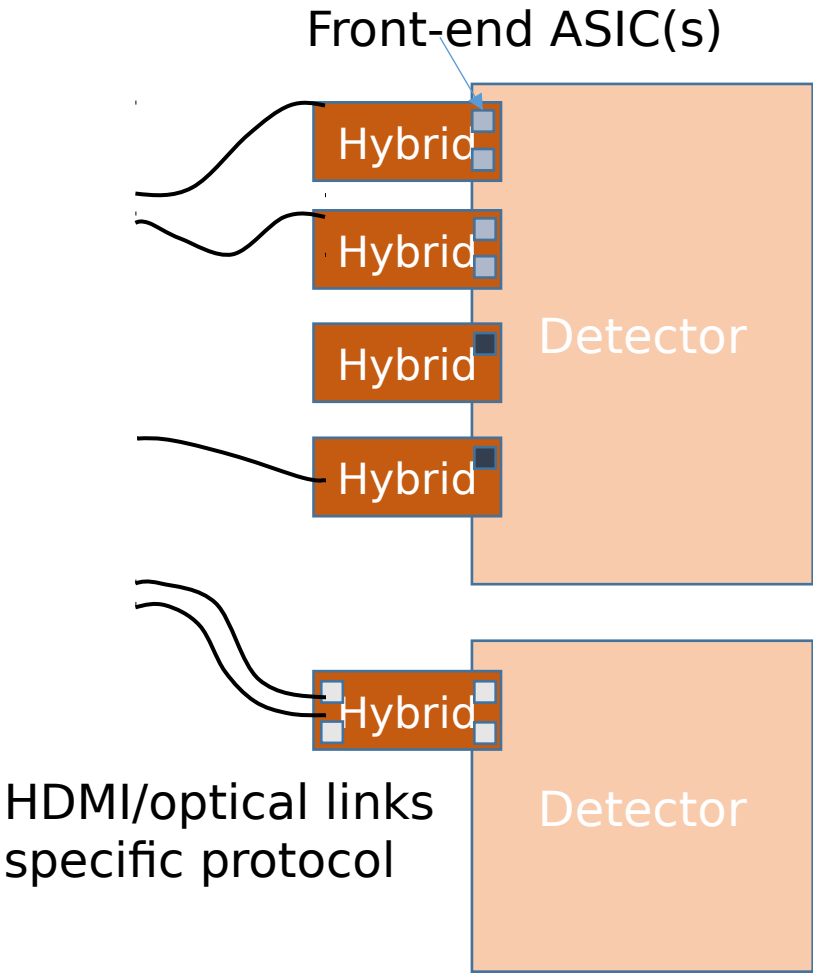
What is SRS?

Scalable Readout System:
A generic readout system for laboratory and detector instrumentation developed and supported by the RD51 Collaboration since 2009
(Inventor: H. Müller)

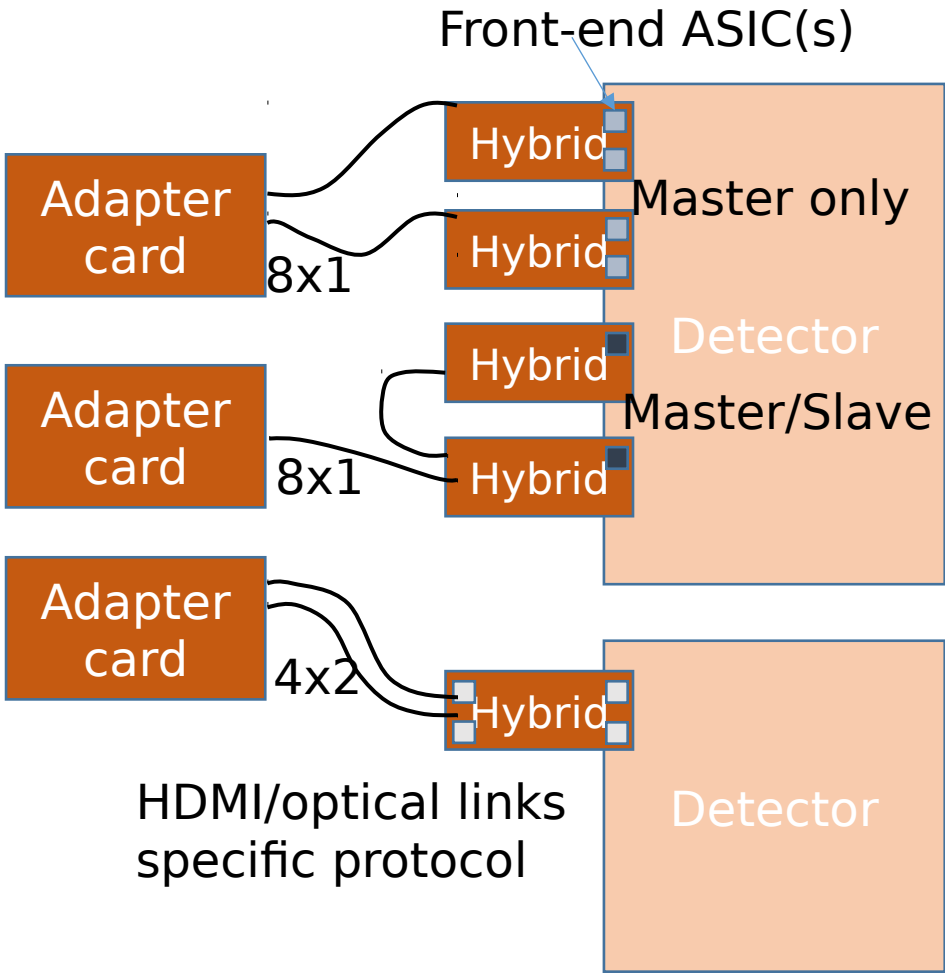


RD51: CERN project and collaboration with more than 500 members from about 90 institutes, recently approved by LHCC for a continuation until 2024

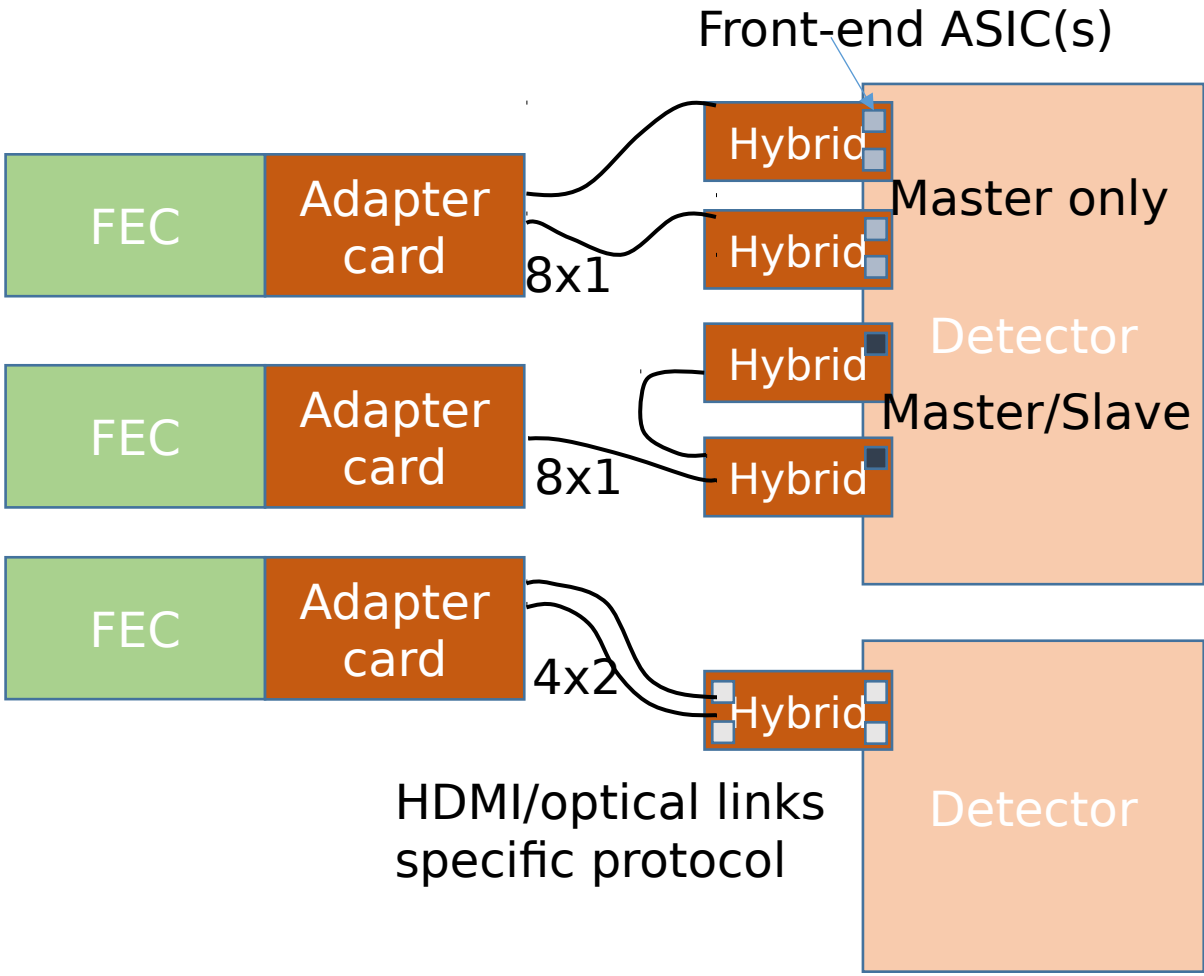
What is SRS?


Front-end ASIC(s)
Hybrid
Hybrid
Hybrid
Hybrid
Detector
Hybrid
Detector
HDMI/optical links
specific protocol

What is SRS?


Front-end ASIC(s)
Adapter card
8x1
Hybrid
Hybrid
Master only
Detector
Adapter card
8x1
Hybrid
Hybrid
Master/Slave
Adapter card
4x2
Hybrid
HDMI/optical links
specific protocol
Detector

What is SRS?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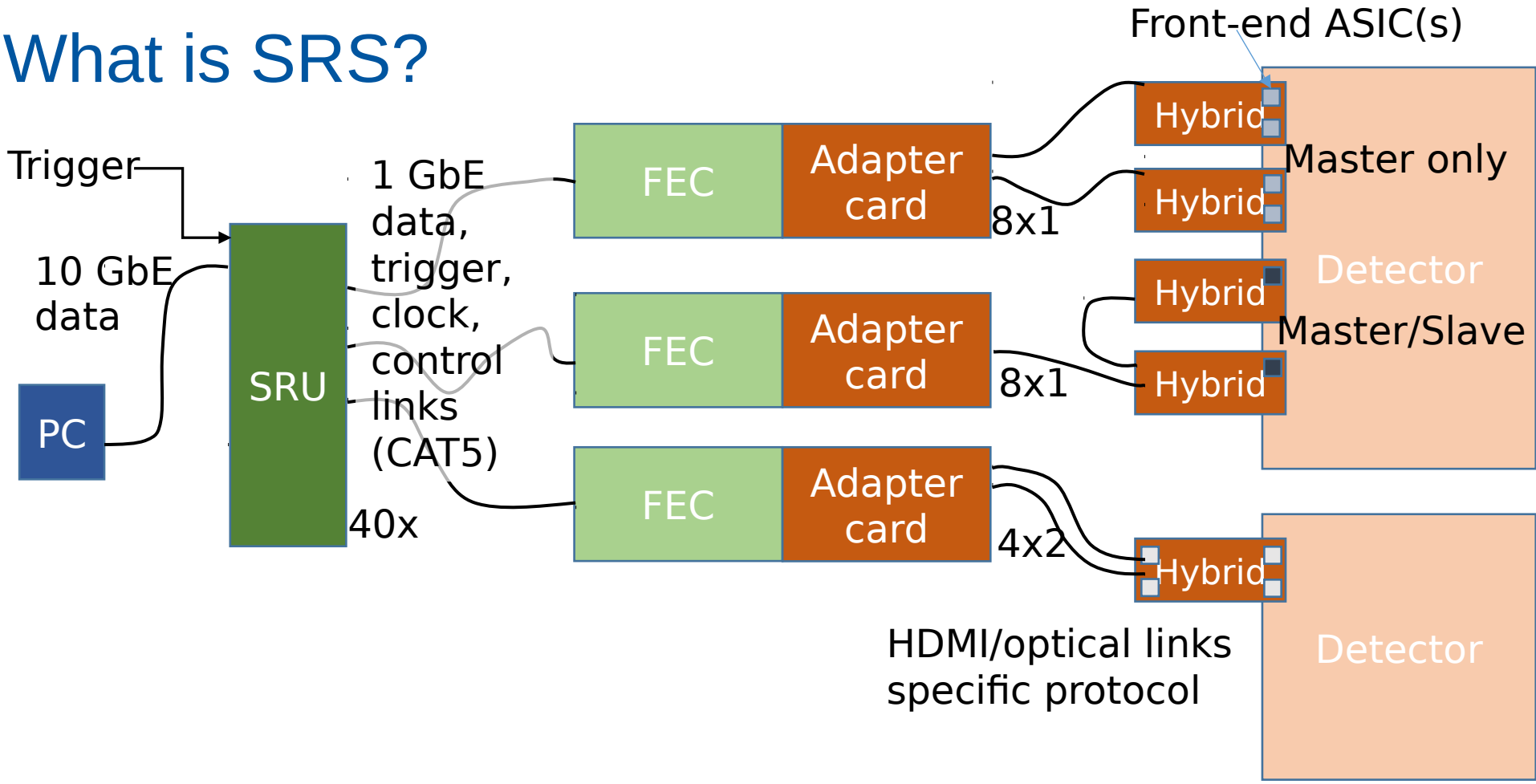
Front-end ASIC(s)
Trigger
10 GbE data
PC
SRU
1 GbE data, trigger, clock, control links (CAT5)
40x
FEC
Adapter card
FEC
Adapter card
FEC
Adapter card
8x1
8x1
4x2
Hybrid
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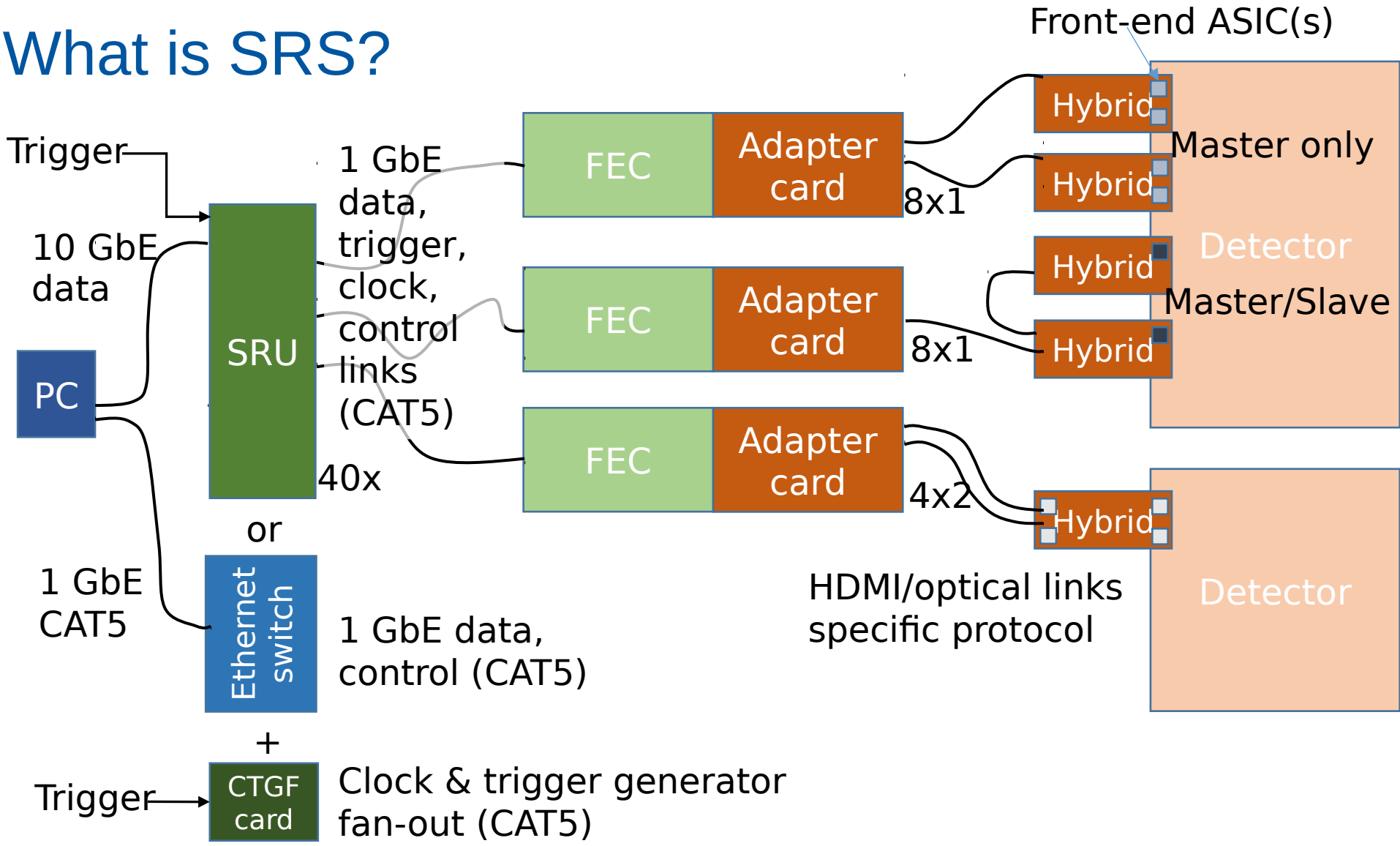
Front-end ASIC(s)
Trigger
10 GbE data
PC
SRU
1 GbE data, trigger, clock, control links (CAT5)
40x
or
1 GbE CAT5
Ethernet switch
1 GbE data, control (CAT5)
+
Trigger
CTGF card
Clock & trigger generator fan-out (CAT5)
FEC
Adapter card
8x1
FEC
Adapter card
8x1
FEC
Adapter card
4x2
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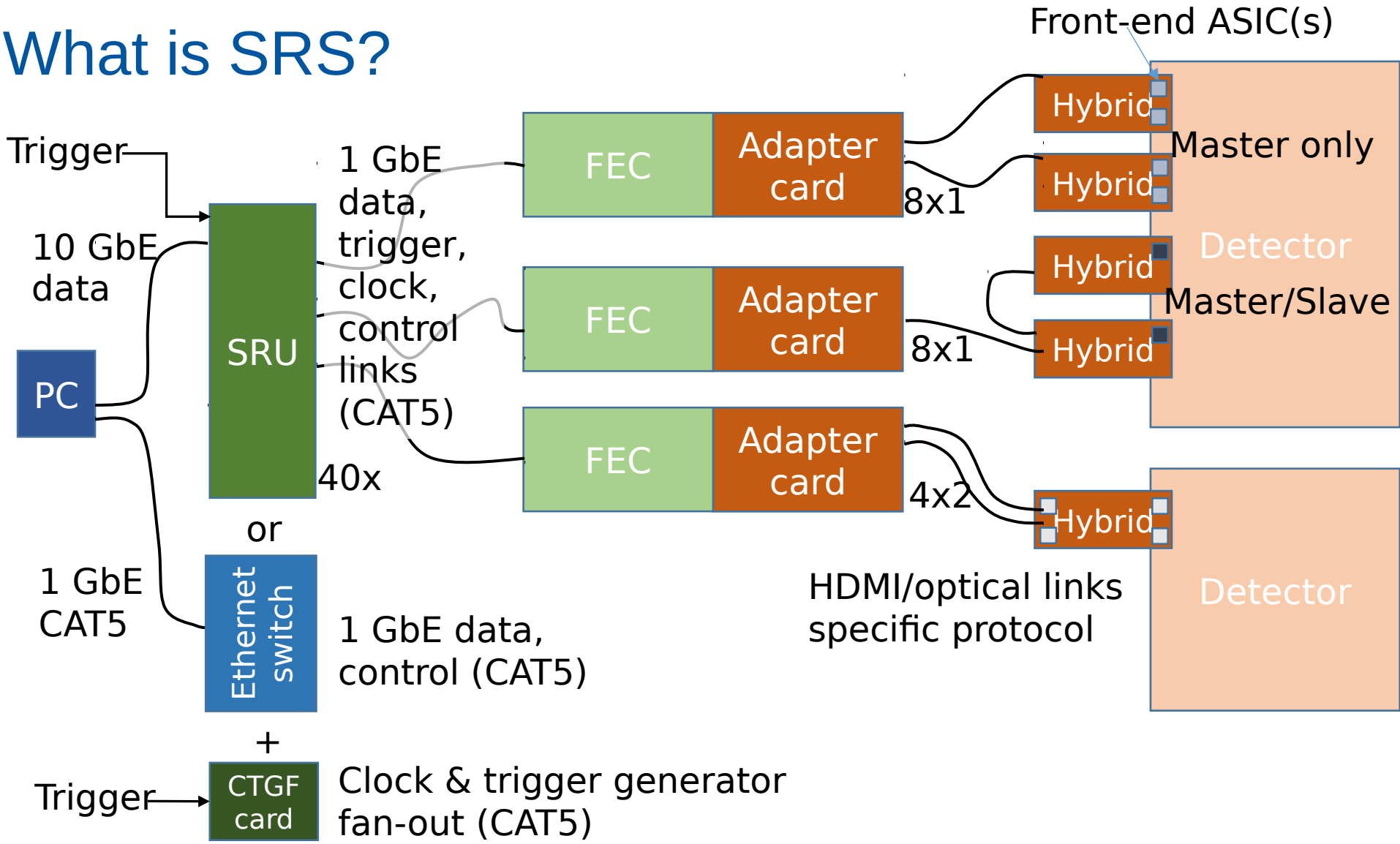
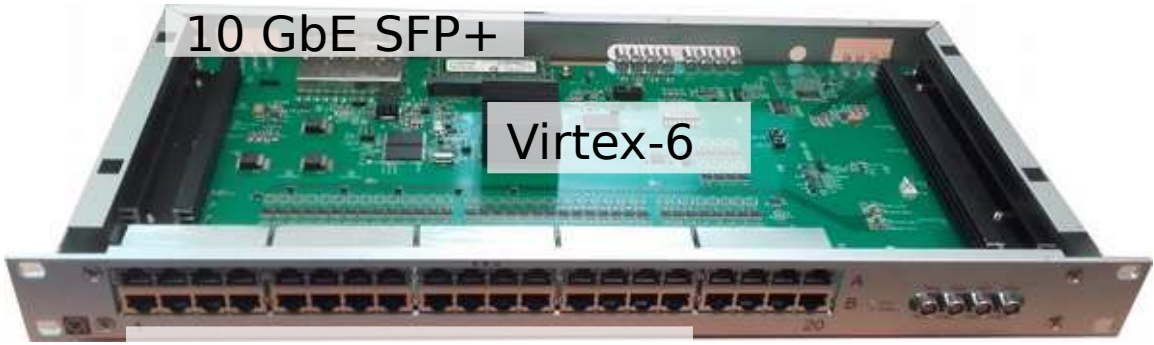


Example AVP25 (strip readout) up to:

82k ch/SRU 2048 ch/FEC 128 ch/hybrid + (master/slave)

What is SRS?

SRU



40x DDTC from FECs

FECv6 (2013)

1 GbE or DDTC to SRU

CTGF v3

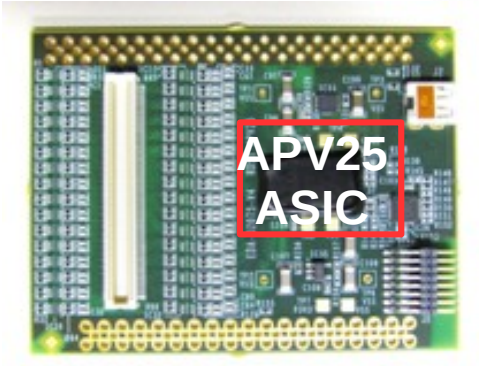
FECv3 (2010)

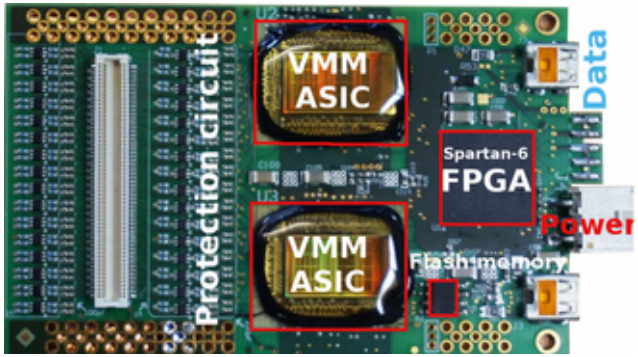
SRS and front-end ASICs

Different ASICs are implemented in SRS:

- APV25 (backbone of MPGD R&D)
- Beetle
- VFAT
- Timepix
- SiPMs

Implementation of ASIC in SRS requires: Hybrid, adapter card, FEC FPGA firmware





Ongoing:

- Timepix3 (Bonn University)
- VMM (future backbone, as APV25 is discontinued)

Just started:

SAMPA (with São Paulo team)

SRS APV - Drawbacks

- ASIC is more than 15 years old
- Low trigger rate O(10 kHz)
- Low data rate due to multiplexed analog output of ASIC
- Limited input capacitance range < 50 pF
- Limited gain range
- No zero suppression in ASIC (only on FEC)
- Export restrictions
- No new production of the ASIC, CERN store stock ~ 0 hybrids

⇨ New ASIC implementation required

VMM3a ASIC

Detailed (public) information on the VMM ASIC: Gianluigi De Geronimo, presentation given at the EIC tracker workshop, 2018

VMM3a ASIC - features

ASIC for the ATLAS NSW upgrade MM and sTGCs detectors

- Designed by BNL: Gianluigi de Geronimo & team
- 130 nm Global Foundries 8RF-DM
- 64 input channels for positive & negative signals

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4 independent data paths:

- Multiplexed 10 bit ampl. + 20 bit time (+ 6 bit channel + 2 flags)
- Serial Address in Real Time (ART) synchronised to 160 MHz
- Parallel prompt output of all 64 channels (e.g. fast 6 bit ampl.)
- Multiplexed analogue amplitude and timing

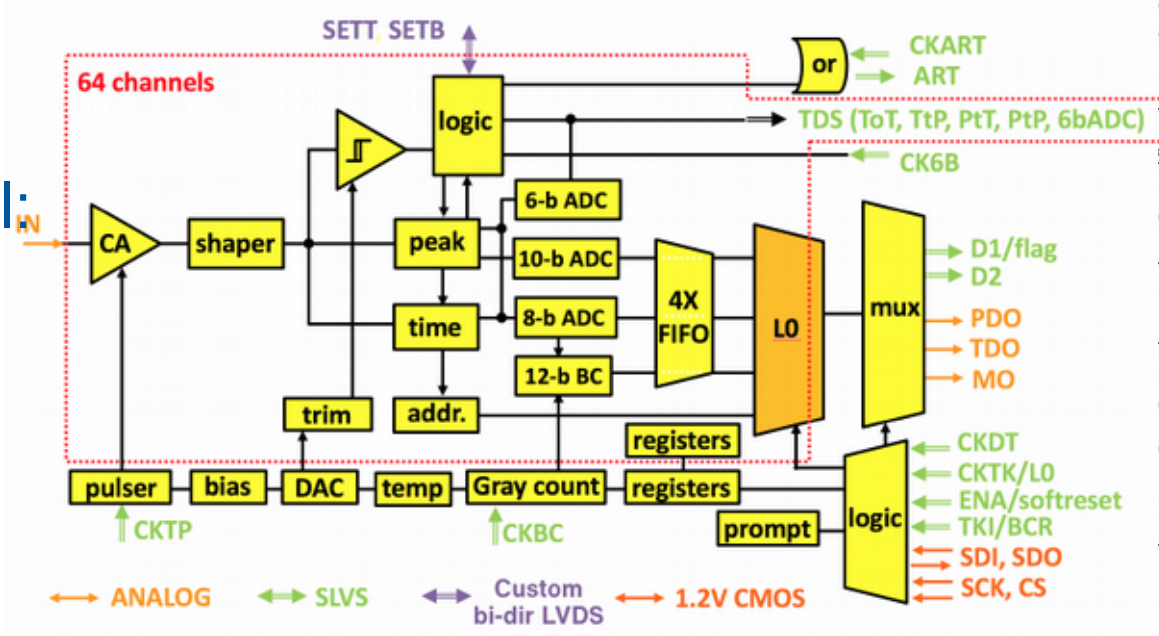
VMM3a ASIC - features

Block diagramme (1ch)

Congigurable per channel:

Shaper peaking times
25, 50, 100, 200 ns

Amplifier gain 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC



Individual 5 bit threshold trim (10 bit global threshold)

Peak detector with neigbouring logic -> amplitude

Time: clocked counter + TAC with slopes 60, 100, 350, 600 ns

4 hit deep buffer + 64 hit deep buffer in L0 external trigger mode

Up to 4 Mhits/channel (theoretically)

VMM3a ASIC - features

Global:

Pulse generator adjustable with 10 bit DAC + 10*C_p

Analogue output of shaper signal (MO), amplitude(pdo) and time (tdo)

Temperature sensor, band gap voltage, pulser DAC and threshold DAC read back via MO

Data output: 2x up to 200 Mhz DDR (D1,D2) = 800 Mbit/s
= 21 MHits/s (38 bit/hit) or 12.5 Mhits/s (64 bit/hit) in L0 mode

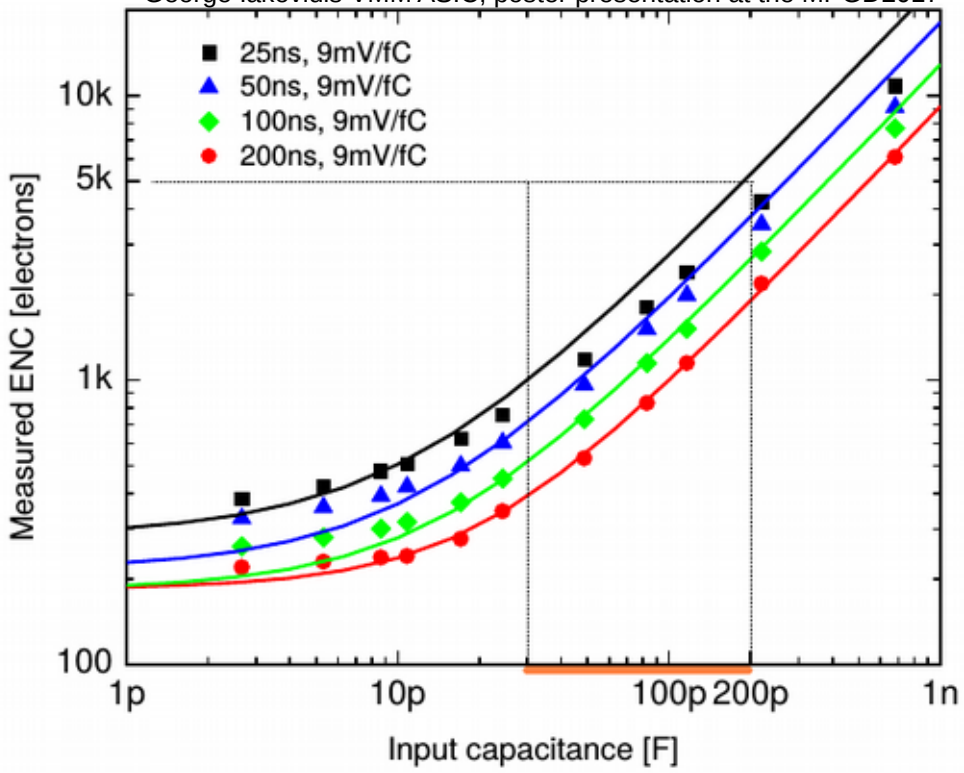
VMM3a ASIC - features

Dynamic range, noise

MM stips (Negative charge -):
Up to ~300 fC, capacitance:
50 – ~200 pF, noise: 3000 e

sTGC:
Wire (-): 6pC -> recover within 200 ns, linearity up to 2pC
Pad (+): 3 pC, 2 nF
Strip (+): 1 pC
Max. DC Input current: 100nA, 1nA oposite polarity

George Iakovidis VMM ASIC, poster presentation at the MPGD2017



VMM3a ASIC - features

Power, all at 1.2 V:

- Vddp: Charge amplifier supply connected to the sources of the p-channel input MOSFETs (max. ≈150 mA)
- Vdd: Powers all other analog circuits (max. ≈400 mA)
- Vddad: Mixed Analog–Digital (ADC) (max. ≈200 mA)
- Vddd: Supplies digital circuits and SLVS drivers (max≈150 mA)

→ ≈ 400 – 800 mW

Cooling: 1 W/chip → cooling required!

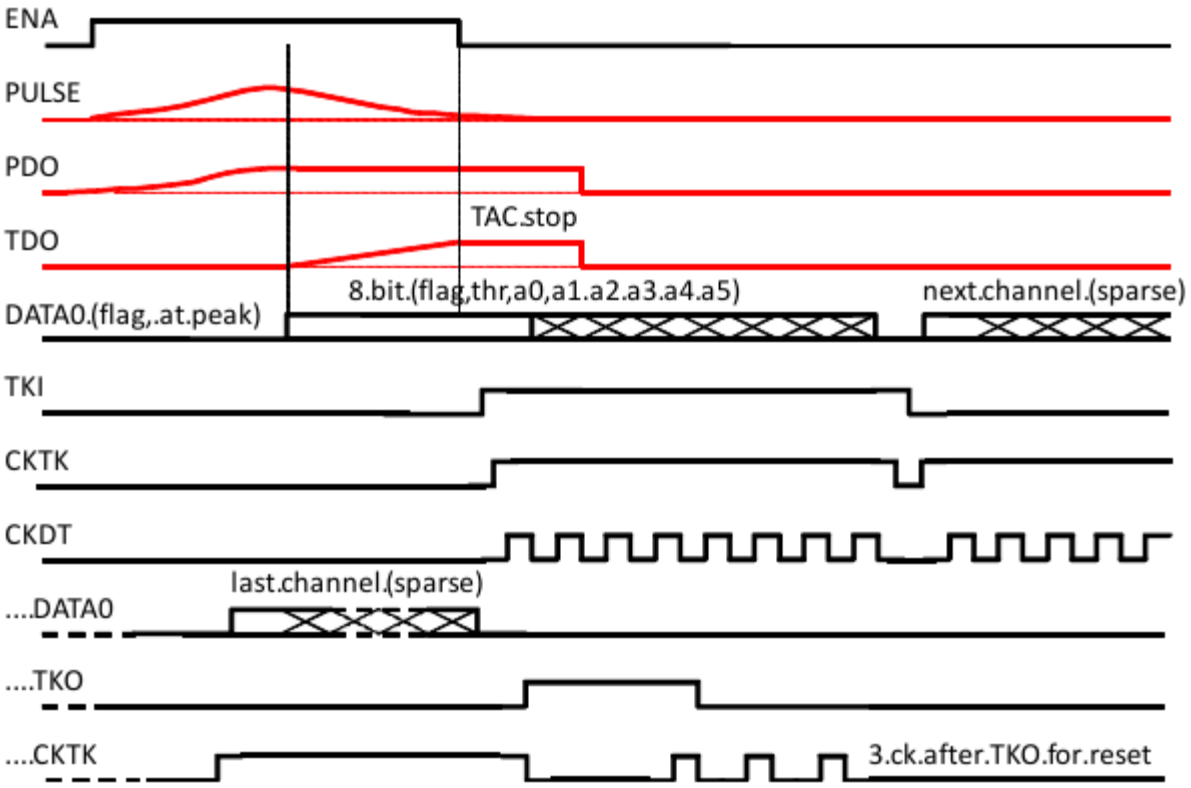
Conversion of internal temperature sensor voltage:

$$°\mathrm{C} = \frac{725 - V_{\mathrm{sensor}}}{1.85}$$

VMM3a ASIC - features

Readout modes: 2 phase analogue mode

Analogue time and amplitude signals made available at pdo & tdo



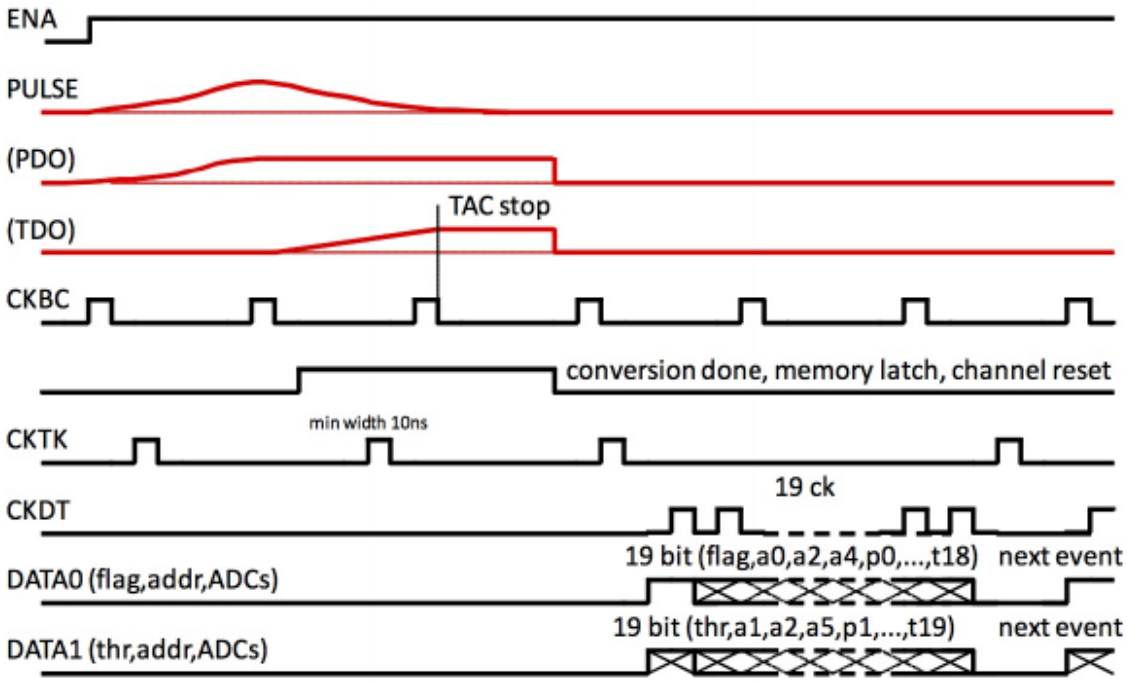
V. Polychronakos et al. ATLAS NSW Electronics Specifications v3_3, June 2017

VMM3a ASIC - features

Readout modes: Contineous mode

- 1 direct output/input per channel: ToT, TtP, PtT, P (10ns pulse)
  or: fast (25ns) conversion of peak amplitude for 6 bit ADC
- 10 bit amplitude, 8 bit time, 10 bit time counter, 6 bit channel,
  1 bit neighbour flag,
  1 bit data flag

→ 38 bit event,
conversion time ≈200 ns



V. Polychronakos et al. ATLAS NSW Electronics Specifications v3 3, June 2017

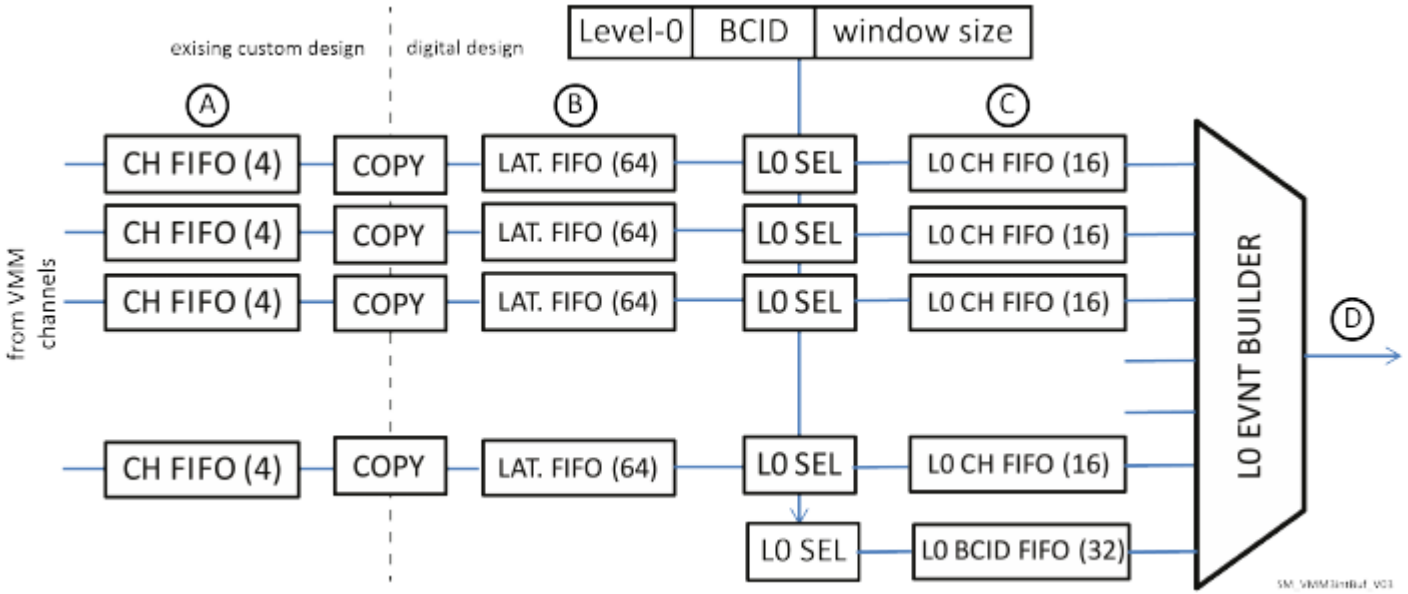
VMM3a ASIC - features

Readout modes: Contineous mode

(1) non-ATLAS mode: 38 bit hit to 4 hit deep FIFO (per channel)

Token to read out hits through D1/D2 serially multiplexed

(2) ATLAS mode: L0 readout with external time window



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VMM3a ASIC - features

Address in RealTime (ART):

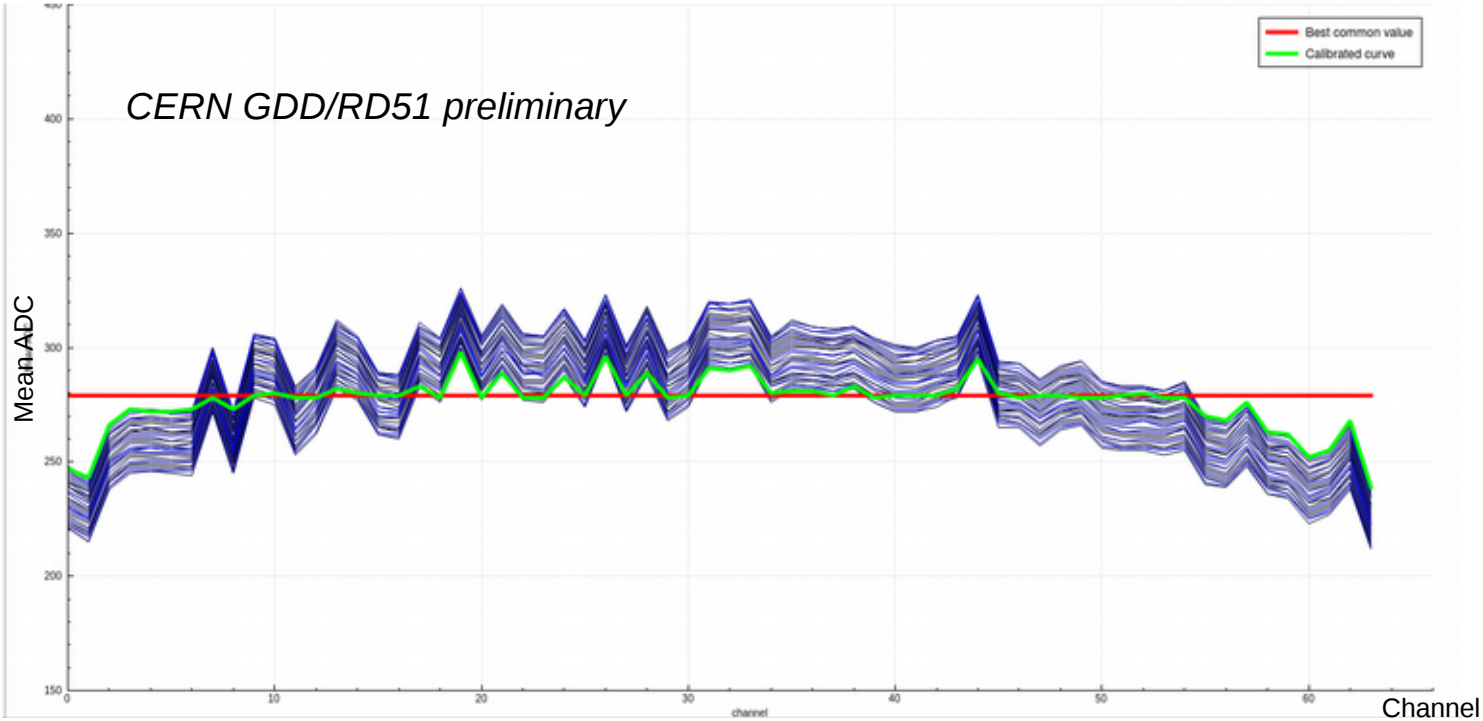
- Fast OR (15 ns after peak or threshold) of all 64 channels
- Available at differential LVDS output

$\Longrightarrow$ can be used as trigger for other detectors

VMM3a ASIC – known issues

Amplitude measurement – ADC gain ununiformity ~10 %

10-bit ADC (pdo) zero calibration using test pulses, VMM0
Parameters: gain 3mV/fC, peaking time 200 ns, sbip/stcl off
Threshold DAC: 300, Pulser DAC 300

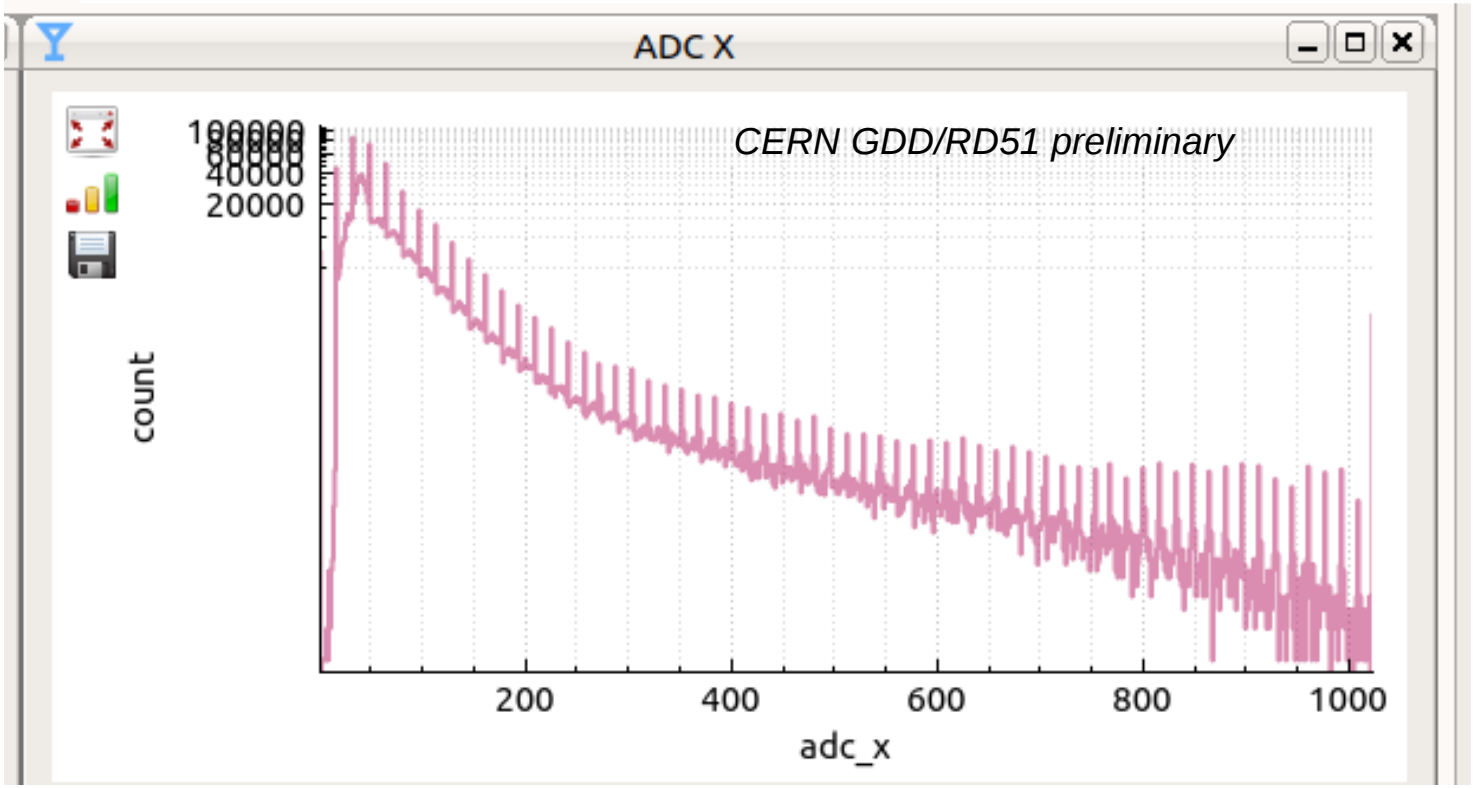


Cannot be fully compensated by baseline calibration ~3 %
→ offline data correction with such a test pulse sample if high ADC resolution required

VMM3a ASIC – – known issues

Amplitude measurement – ADC spectrum

Accumulation in preferred ADC values
→ reduced resolution for amplitude and time measurement



VMM integration in SRS

M. Lupberger et al., Implementation of the VMM ASIC in the Scalable Readout System, Nucl.Instrum.Meth. A903 (2018) 91-98

Implementation of the VMM ASIC in SRS

Project in Gaseous Detector Development group at CERN

- funded by EU **BrightnESS** and AIDA2020 project and the detector group of the European Spallation Source ESS
- Project driver: NMX instrument at ESS
- Benefit for whole RD51 community and beyond
- Goal: replace SRS APV as backbone for MPGD R&D
  - THE readout for the next decade within the community
  - Application beyond the community
  - Application beyond R&D → experiments

VMM3a SRS hybrid

2 VMM3a ASICs

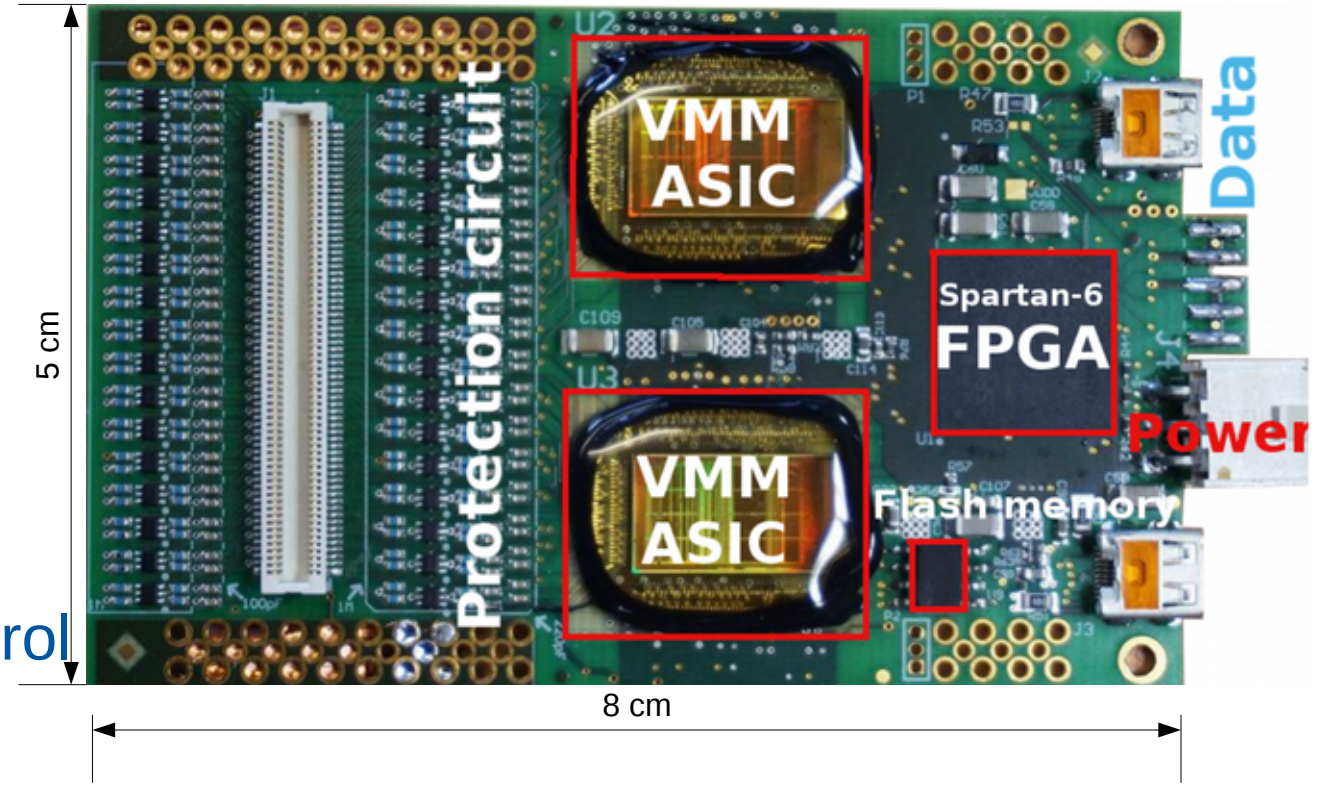
1 Spartan-6 FGPA

1 Flash memory

128 input channels spark protection

2x Micro HDMI:

- Power, data, control
- ART



1 Power

2 I2C ADCs for MO, pdo, tdo of each ASIC

Powering on back side: 5 LDOs, capacitors
2 Supply voltages: min. 1.5 V (VMMs), min 2.8V (FPGA, flash)

VMM3a SRS hybrid

Unused VMM3a features

- 64 direct outputs/ASIC

VMM3a SRS hybrid

Unused VMM3a features

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Not implemented:

- 2 phase analogue mode (could be implemented in firmware using external I2C ADCs)
- ATLAS L0 triggered mode

VMM3a SRS hybrid

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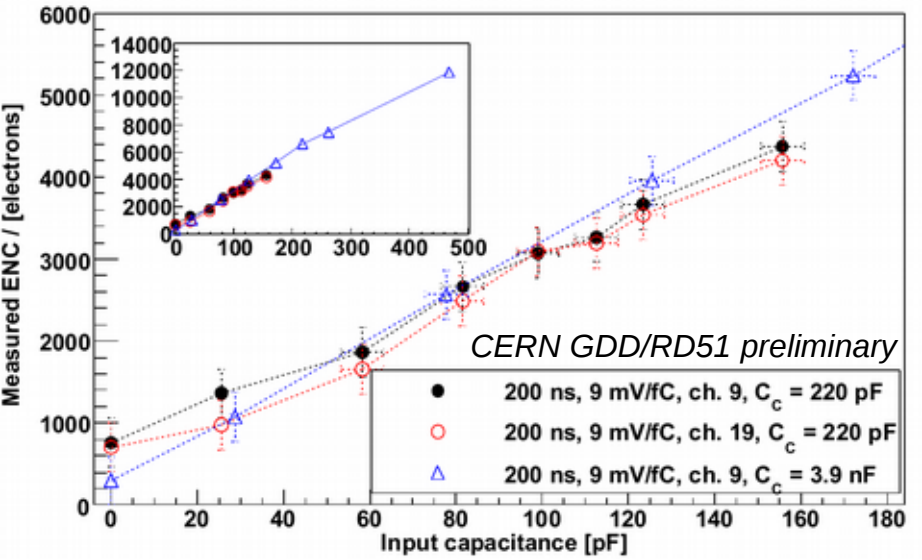
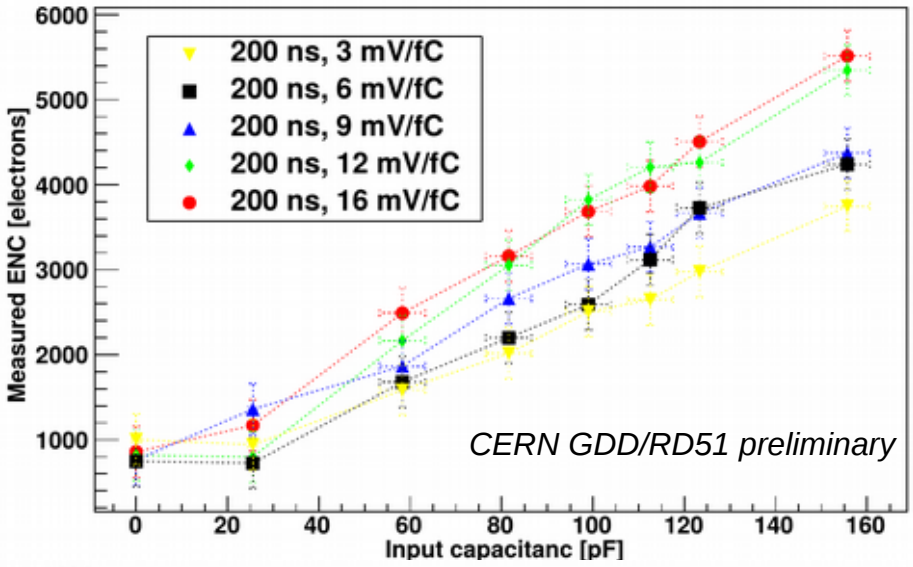
Readout speed VMM→Spartan-6: 160 MHz DDR(*2) = 640 Mbit/s (Possible: 200 MHz, bit errors when tested with 180 Mhz, VMM2 | chip or firmware?)

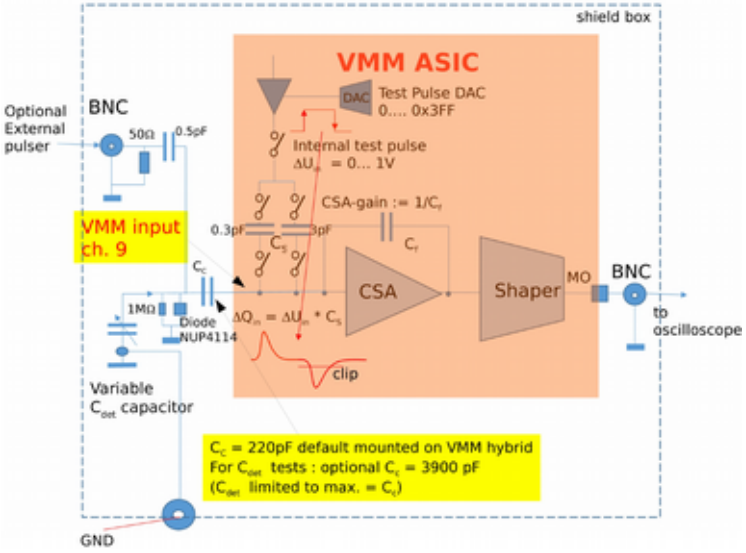
Speed Spartan-6 FPGA → HDMI: 8b10b, 400 MHz = 320 Mbit/s (per VMM, possible: 950 MHz = 760 Mbit/s)

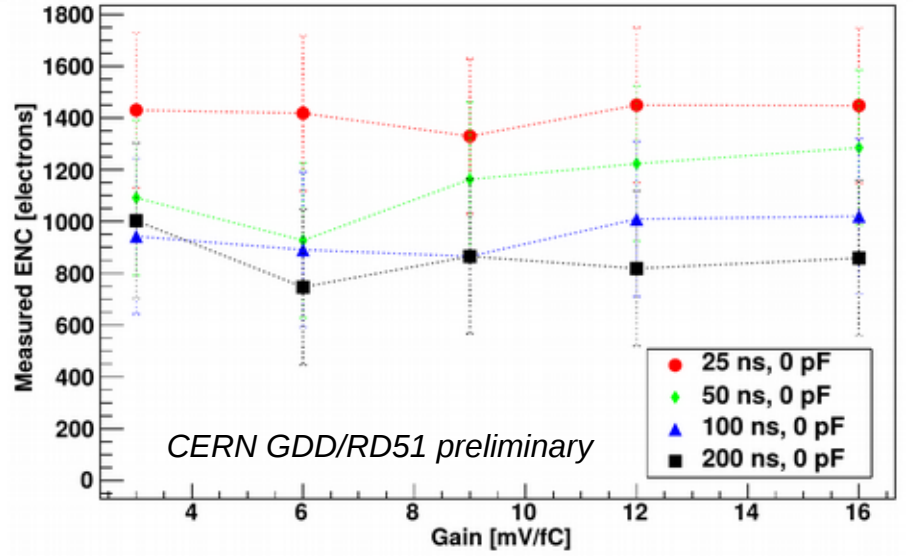
1024 hit deep FIFO on hybrid

VMM3a SRS hybrid - Hybrid noise tests (VMM3)



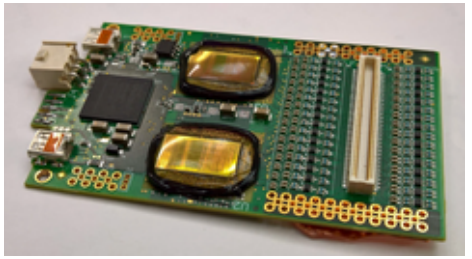






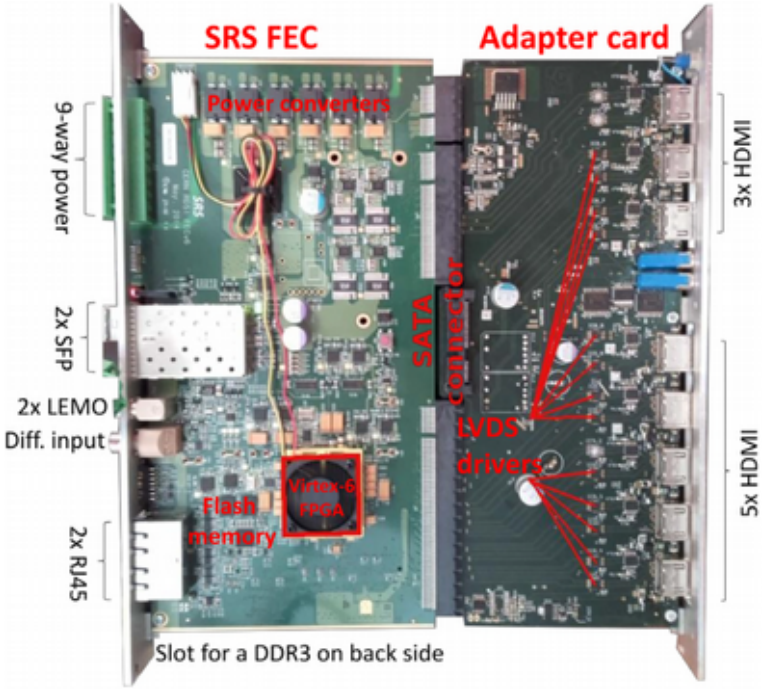
Status and applications

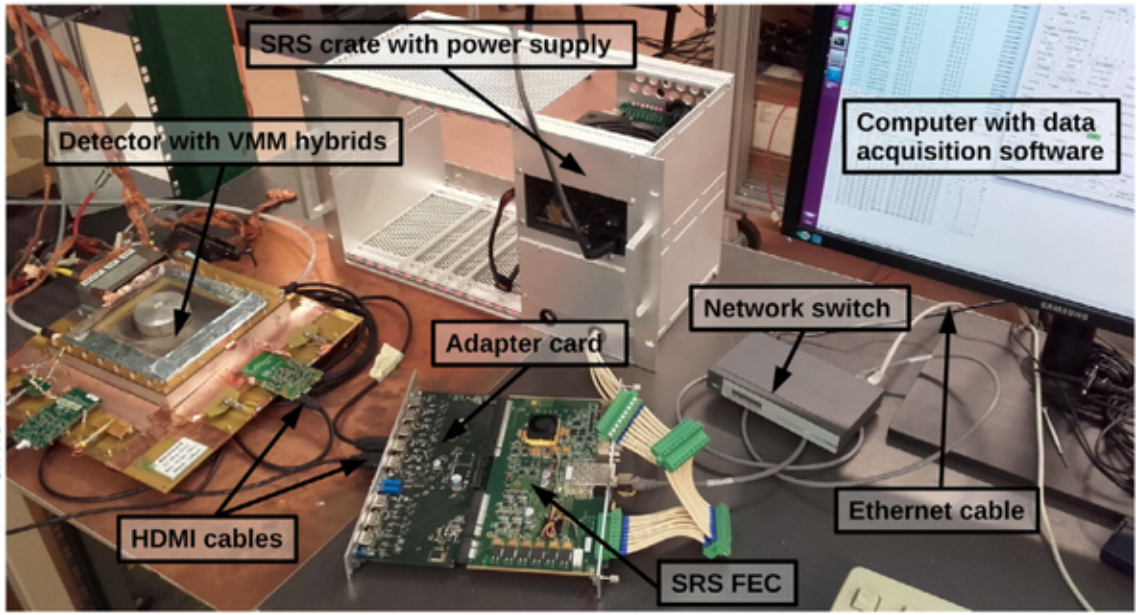
Status



Hardware components:

- SRS FEC: general SRS component → ✔
- Hybrids: 4 v3 (VMM3, VMM3a), 4 v4 (VMM3a, final), industrial test production started with 20 v4 (VMM3a, final) → ✔
- Adapter Card: 4 prototypes v4, final v5 submitted → 🔧





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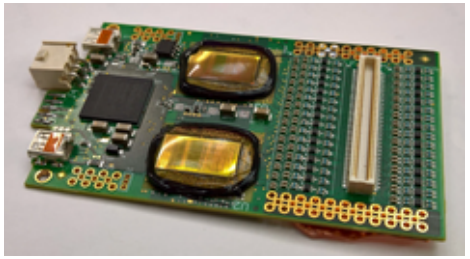

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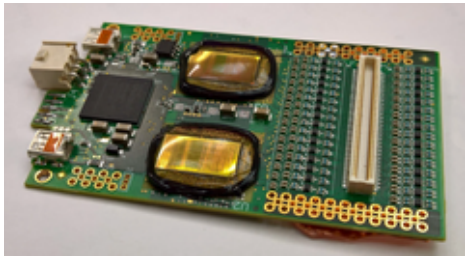

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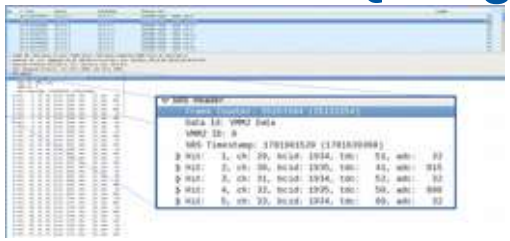
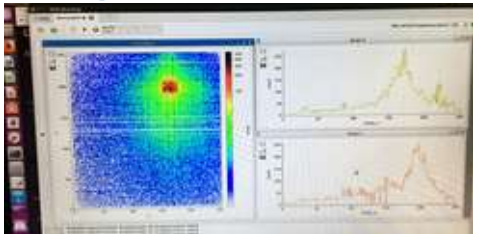
Software:

- Slow control, online monitoring, DAQ working → ✔
- Redesign into VMM DAQ ongoing with CERN EP-DT-DI → 🔧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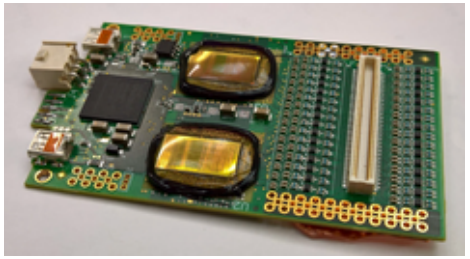

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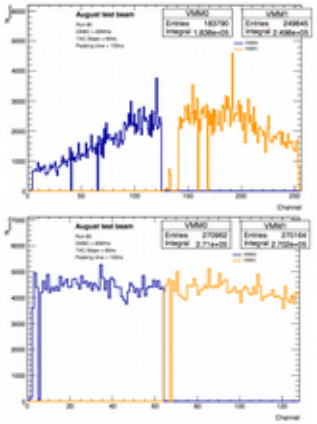
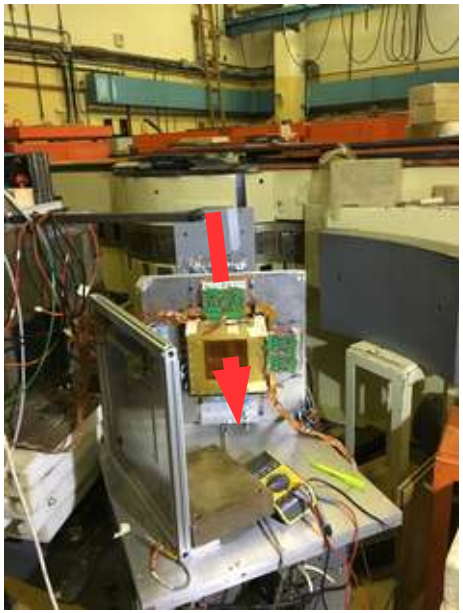
Integration

- Single FEC (4 hybrids) used at many test beams → ✔
- Multi-FEC systems only tested in lab → 🔧

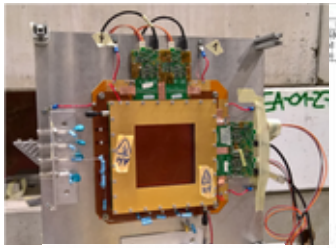
Applications - Test beams

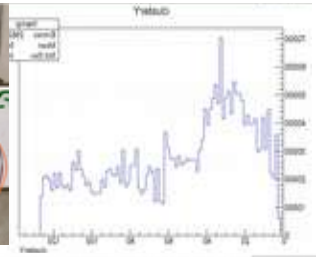


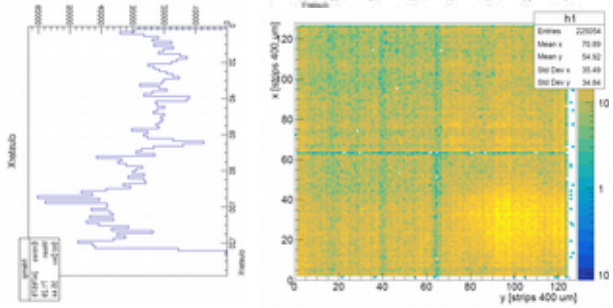
August 2017 (SPS): 3 VMM3 hybrids



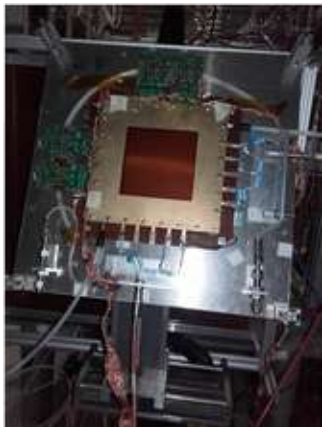
July 2018 (Neutrons@Wigner): 3 VMM3 + 1 VMM3a hybrids

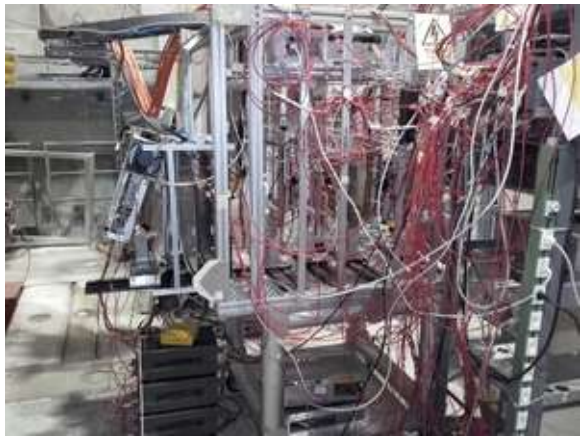






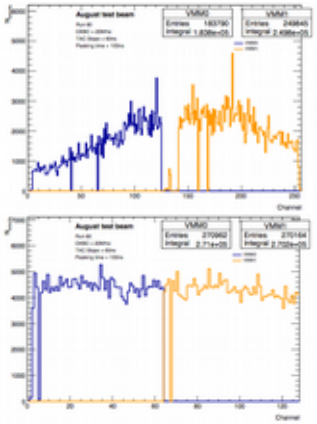
October 2017 (SPS): 4 VMM3 hybrids



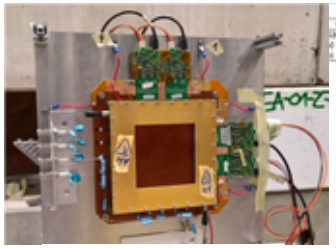


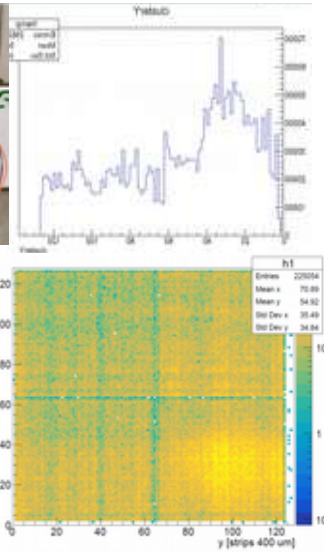
August 2018 (SPS): 3 VMM3 + 1 VMM3a hybrids, GBAR proto

Applications - Test beams



August 2017 (SPS): 3 VMM3 hybrids

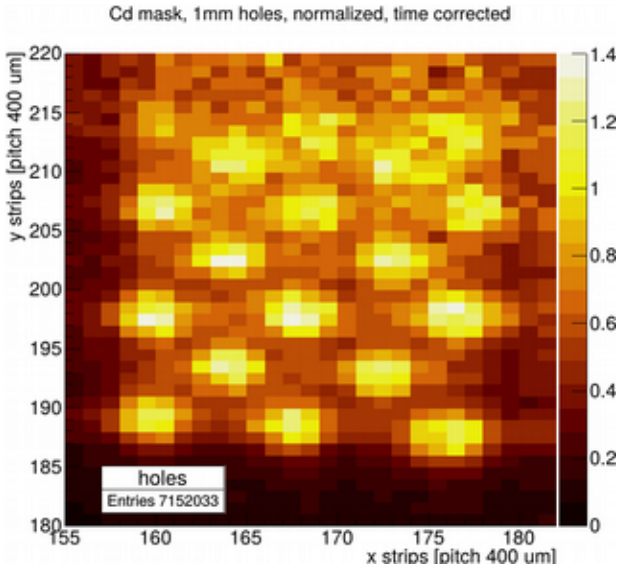




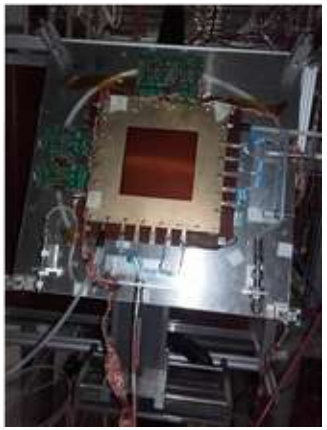
October 2017 (SPS): 4 VMM3 hybrids

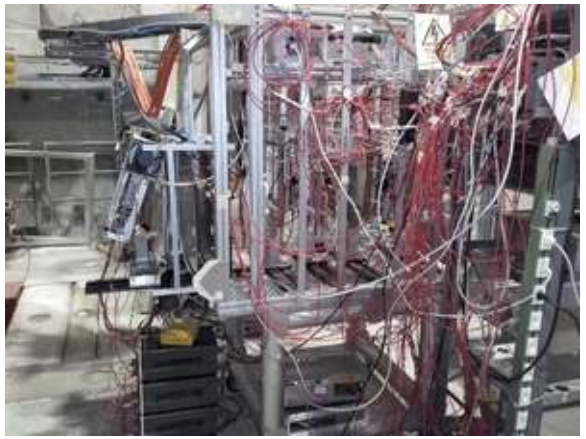
Cadmium mask, 1 mm holes

Reconstructed neutron hits



July 2018 (Neutrons@Wigner): 3 VMM3 + 1 VMM3a hybrids





August 2018 (SPS): 3 VMM3 + 1 VMM3a hybrids, GBAR proto

Applications - Future SRS VMM users / interested parties

Group	Application	VMM hybrids	Contact
ESS Lund / BrightnESS	NMX instrument @ ESS	164	Dorothea PFEIFFER
University of Science and Technology of China	RICH R&D for future colliders in China (CEPC and STCF)	156	LUI Jianbei
Bonn University	BASTARD neutron detector	71	Jochen KAMINSKI Markus KÖHLI
Mainz University	MAGIX experiment @ MESA*	211	Stefano CAIAZZA
Budker Institute of Nuclear Physics, Novosibirsk	μWell MPGD R&D	22	Lev I. SHEKHTMAN
INFN Tieste	Generic R&D	10	Silvia DALLA TORRE
Tsukuba University	ALICE FoCal, Si Pads	50	CHUJO Tatsuya
GDD group CERN	Generic R&D	16	Eraldo OLIVERI
Peking University	CMS GEM upgrade	52	Dayong WANG
LMU Munich	Ion Tomography with Micromegas	16	Felix KLITZNER
LMU Munich	Medical physics with MPGDs, Si	48	Jona BORTFELDT
ETH Zurich	GBAR experiment @ CERN	≈40	Gianluca JANKA
CERN	BGV(Beam Gas Vertex) beam monitor*	200	Robert KIEFFER
University of Virginia, Charlottesville	EIC tracker @ RHIC*	Not known yet	Kondo GNANVO

*: not yet approved

Conclusion

- VMM ASIC has been implemented in the Scalable Readout System within the BrightnESS project, outcome is a prototype
- VMM was correct choice due to flexible configuration
- The system will become the new workhorse within the MPGD community and beyond and replace APV25-based version
- Upcoming R&D projects and experiments rely on the system
  - → highest priority: provide hardware
  - → train users with current software and firmware
  - → collaborate with experiments
- Secure continuation of developments

(personal) Ideas for the future of SRS

What will/should happen in the next years

SRS claims to be a multi-purpose readout system, implementation of VMM was/is big step forward:

- SRS VMM will replace SRS APV and become THE readout option in RD51 and projects even outside our collaboration and other research fields.
- System needs to be further developed to fully exploit the capabilities of the VMM and current SRS hardware.
- SRS users and developer groups must continuously improve the system such that it can be operated reliably in the lab and at experiments.
- Supply with hardware, firmware, software, training and know how must be organised.

⇨ more and more users (also running experiments or such in the design phase) will join

BUT: System and current ASIC implementations have drawbacks

- Application in harsh environments (radiation, magnetic field)
- Output bandwidth of FEC (limited to 1 GbE ↯up to 800 Mb/s/VMM)
- FPGA capabilities on FEC (XC6VLX130T, limited transceiver speed)
- Links to front-end (usually HDMI cables, limited bandwidth, frequency)

⇨Hardware upgrade of FEC (from 2013) and other front-end ASICs and links needed for wider range of application and modern (streaming) readout.

(personal) Ideas for the future of SRS

What will/should happen in the next years (continued)

Implement new ASICs in SRS

- VMM implementation most advance (BrightnESS and AIDA2020)
- Timepix3 and GEMROC ongoing (AIDA2020)
- future candidates: SAMPA, a radiation hard ASIC of the SiPixel community

Upgrade of SRS core hardware (FEC)

Learn from state-of-the-art and ongoing developments in HEP (like CaRIBOu, FELIX, PCIe40, USBpix, SPIDR, RCE…) ⇨ design new FEC. Current ideas:

- Go from pure FPGA to System on Chip
- Significantly improve output bandwidth to handle data from larger system (streaming readout) and cope with high data rates of VMM (up to 800 Mb/s/VMM) and recent ASICs in general (e.g. Timepix3: 5.12 Gb/s), optimum would be 100 Gb/s Ethernet output
- FEC PCB layout for lpGBT/VL+ links and latest PCIe standard to implement radiation hard and high bandwidth ASICs

The End

Thanks for your attention

SRS APV

APV25 ASIC: Readout chip for CMS tracker

- 250 nm CMOS technology
- Delivered: 2001
- Configuration via I2C
- 128 channels with preamp and shaper
- Output: multiplexed analogue levels
- 40MHz clock

APV25 hybrid:

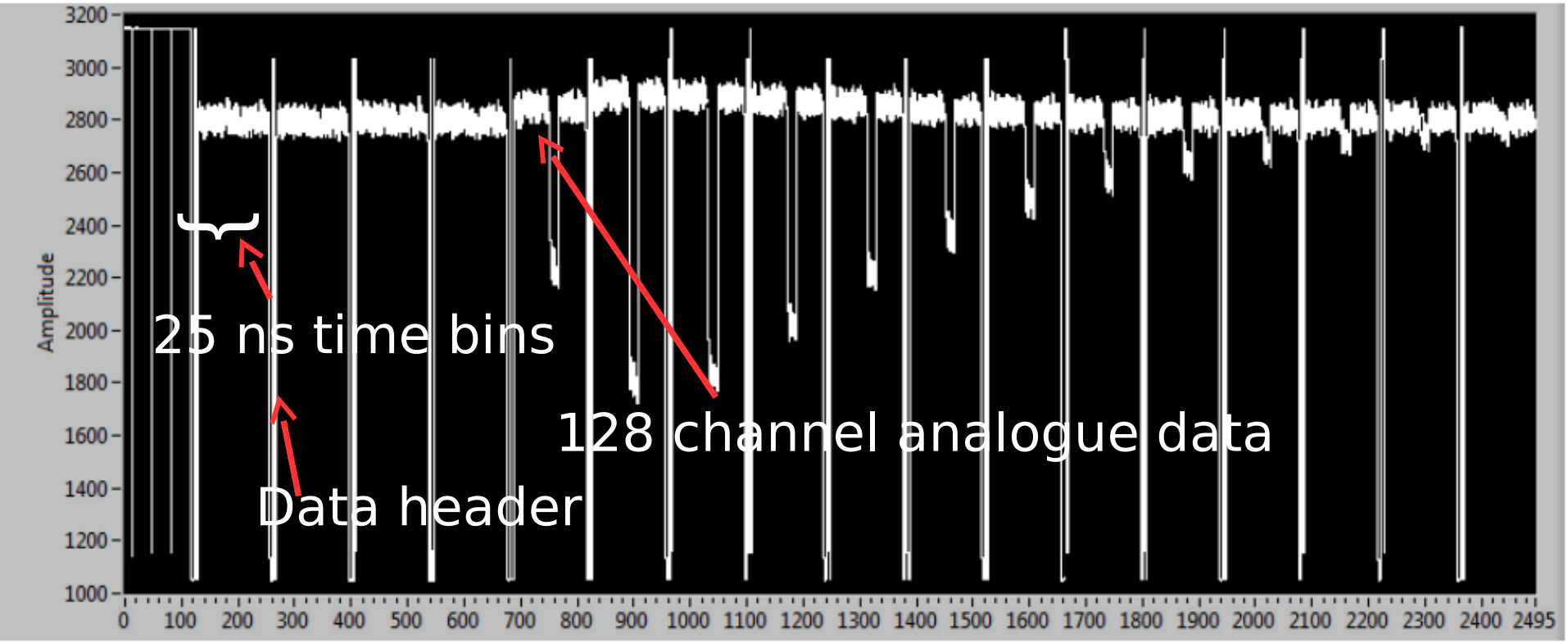
- One APV25 ASIC
- PLL
- LDO for power
- Master/Slave
- Protection circuit

Adapter card:

- Mainly ADCs
- Can read up to 16 APV25 hybrids

S. Martoiu et al., Development of the scalable readout system for micro-pattern gas detectors and other applications, JINST 8.03 (2013), C03015

SRS APV



Maximum trigger rate with special firmware: 5 kHz

(K. Gnanvo @ RD51 Collaboration Meeting Aveiro 2016)

Up to ≈ 40 kHz with different readout system, reduced time bins in COMPASS experiment

SRS APV

1) Detection and imaging of high-Z materials with a muon tomography station using GEM detectors
K. Gnanvo et al., Nuclear Science Symposium Conference Record (NSS/MIC), 2010 IEEE. IEEE, 2010.

2) Performance in Test Beam of a Large-area and Light-weight GEM detector with 2D Stereo-Angle (U-V) Strip Readout
K. Gnanvo. et al., Nucl. Inst. and Meth. A808 (2016): 83-92.

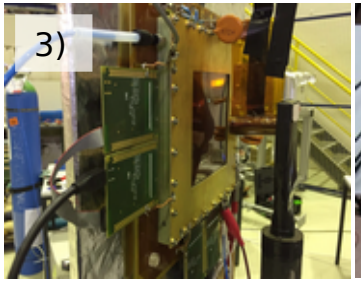
3) GEM-based polarimeter detector development for storage ring EDM experiment
S. Park, Presentation given at the AFAD2018, Jan 2018.

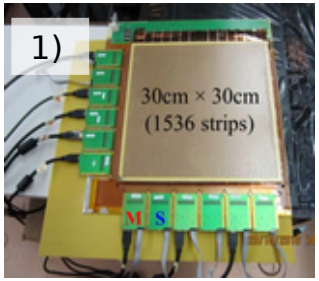
4) Development and test of the DAQ system for a Micromegas prototype installed in the ATLAS experiment
M. Bianco et al., Journal of Physics: Conference Series. Vol. 664. No. 8. IOP Publishing, 2015.

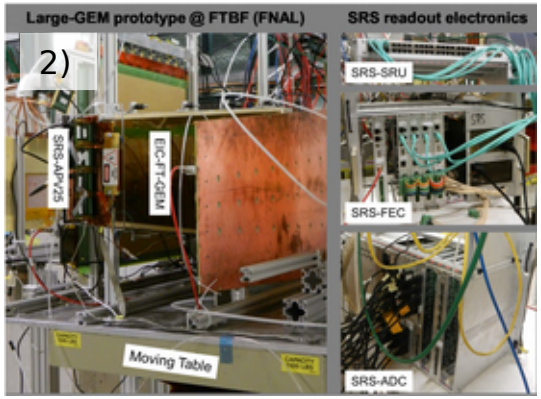
5) Performance studies under high irradiation of resistive bulk Micromegas chambers at the CERN Gamma Irradiation Facility
O. Sidiropoulou et., PoS (2017): 1216.

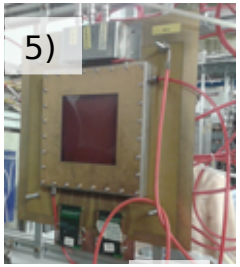
6) Characterization of triple-GEM detectors for the Phase I Muon System Upgrade of the CMS Experiment at LHC
R. Venditti, Advances in Sensors and Interfaces (IWASI), 2017 7th IEEE International Workshop on. IEEE, 2017.

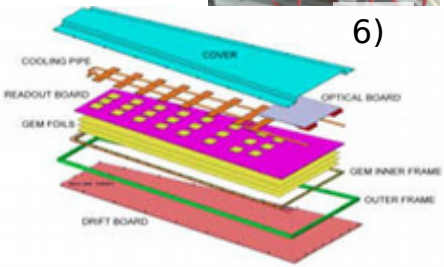
7) More than 100 systems sold via CERN store



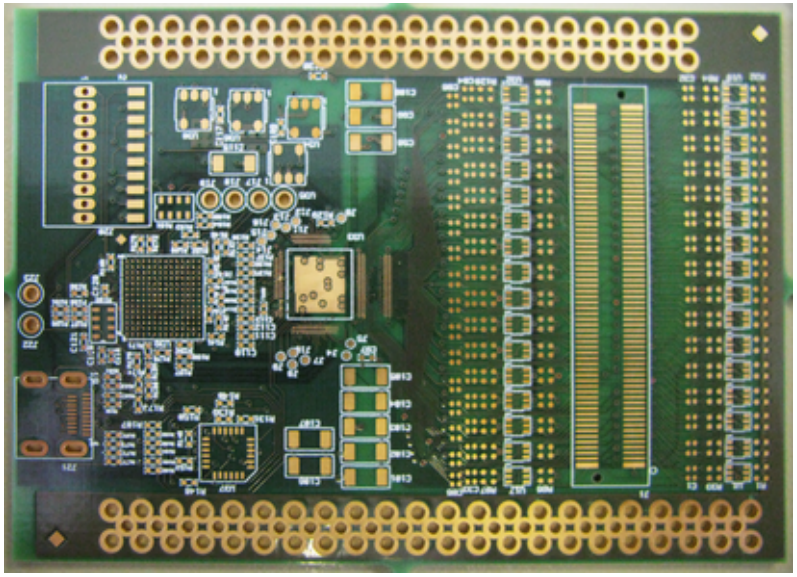




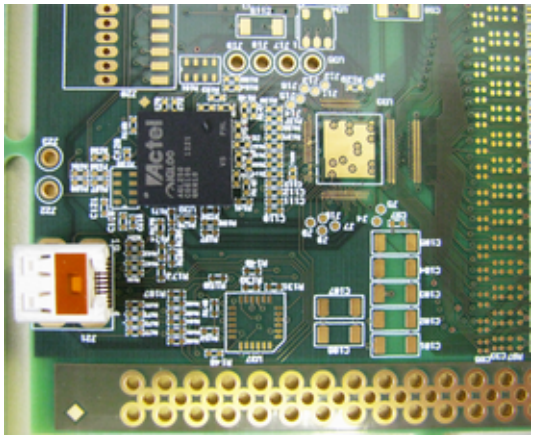




SRS Beetle



Common project with ATLAS NSW before VMM was available



Project had to be stopped

- ACTEL FPGA proposed for radiation hardness – could not be verified
- Company could not deliver hybrids due to problems with four row wire bonding

SRS VFAT

RD51 VFAT hybrid

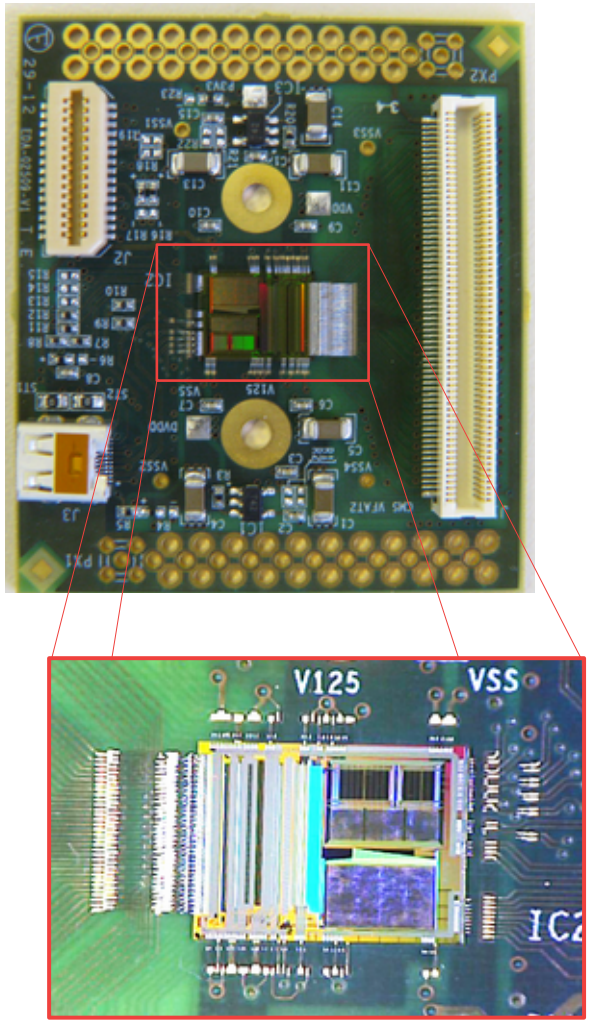
Not successful:

- too much noise

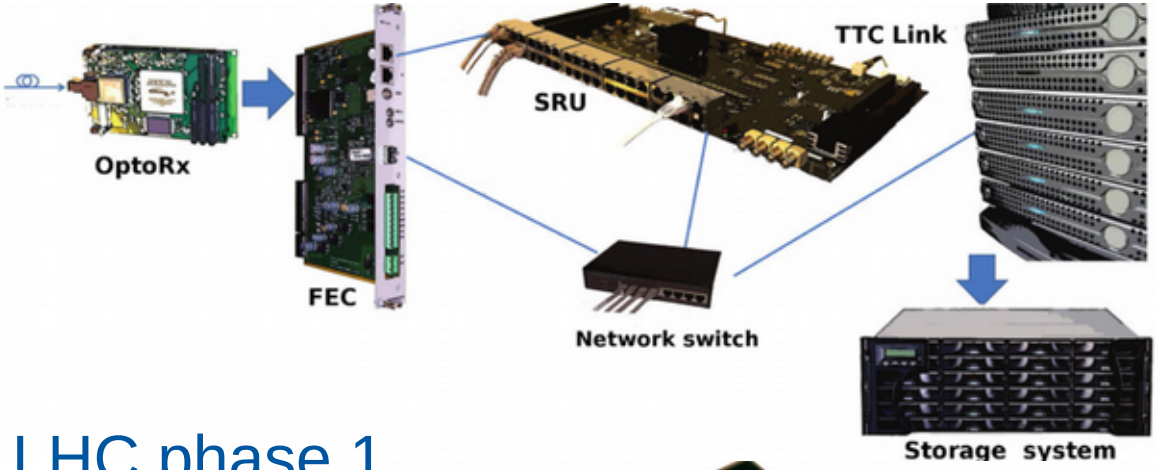
- wrong information from designers

→ abandoned

But...



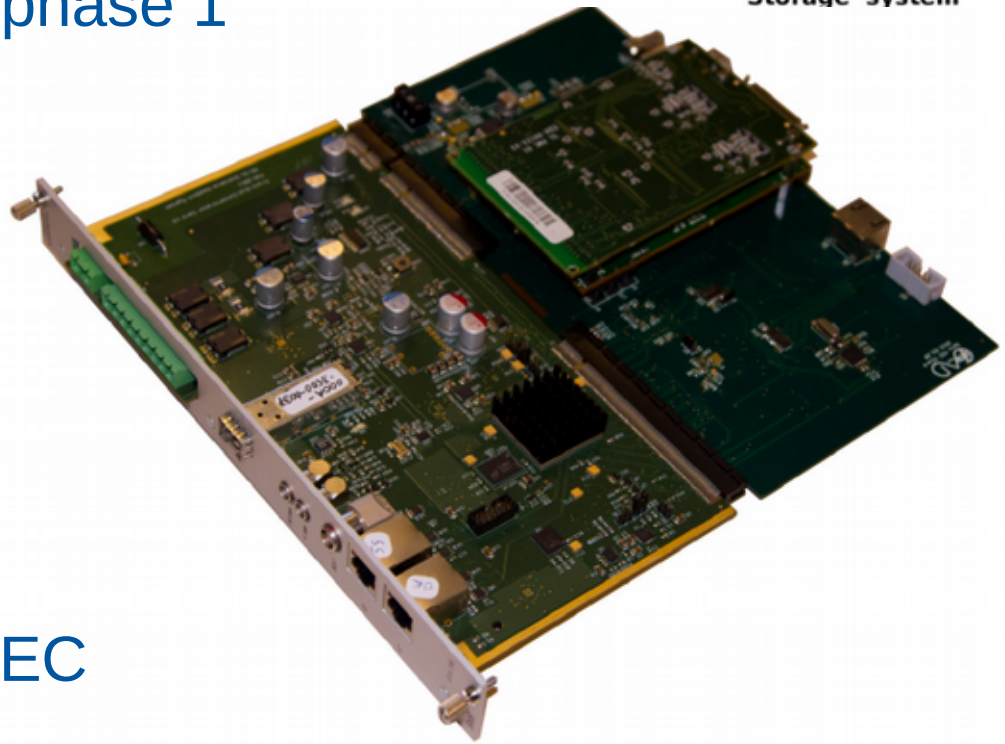
SRS VFAT



TOTEM DAQ upgrade

VME based electronics in LHC phase 1

for VFAT opto carrier board



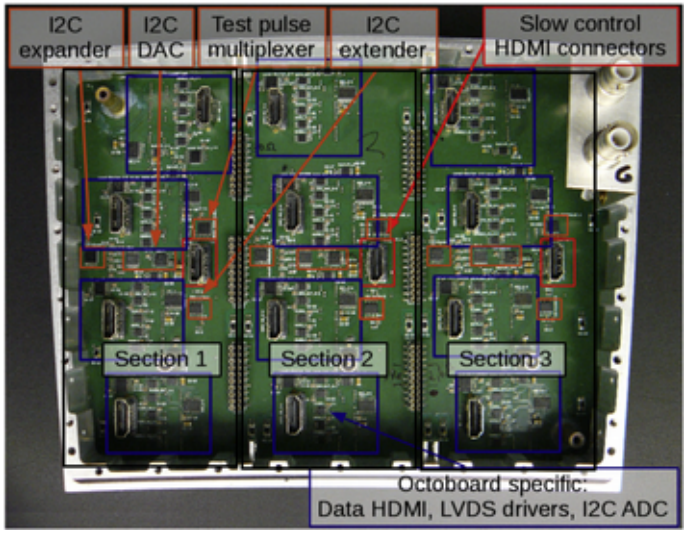
SRS for phase 2:

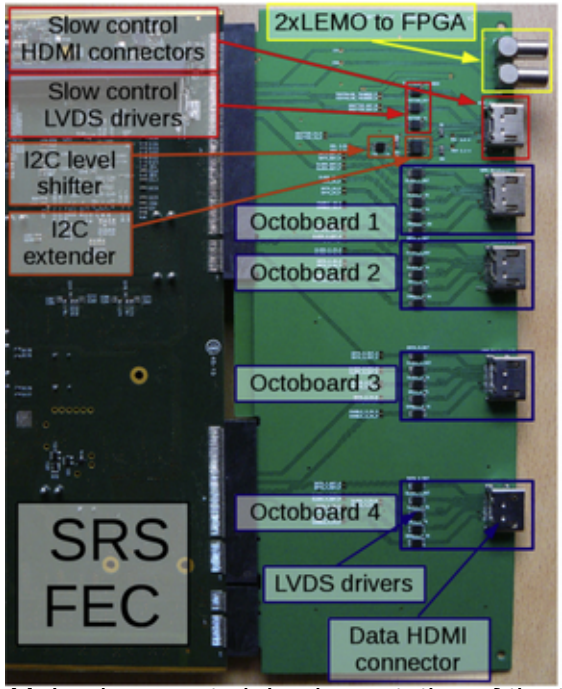
- trigger rate 1 kHz → 24 kHz
- Zero suppression
- L2 hardware algorithms in FEC

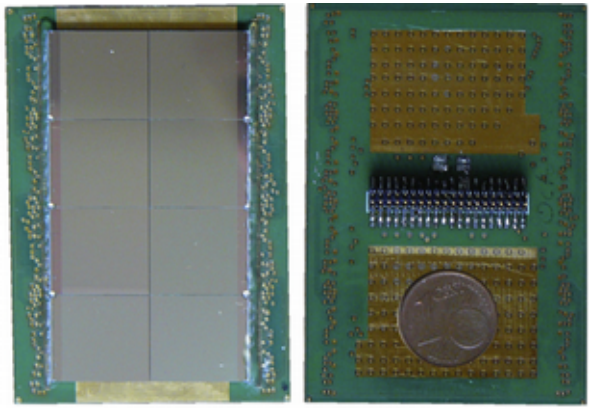
M. Quinto et al., The TOTEM DAQ based on the Scalable Readout System (SRS), EPJ Web of Conferences. Vol. 174. EDP Sciences (2018).

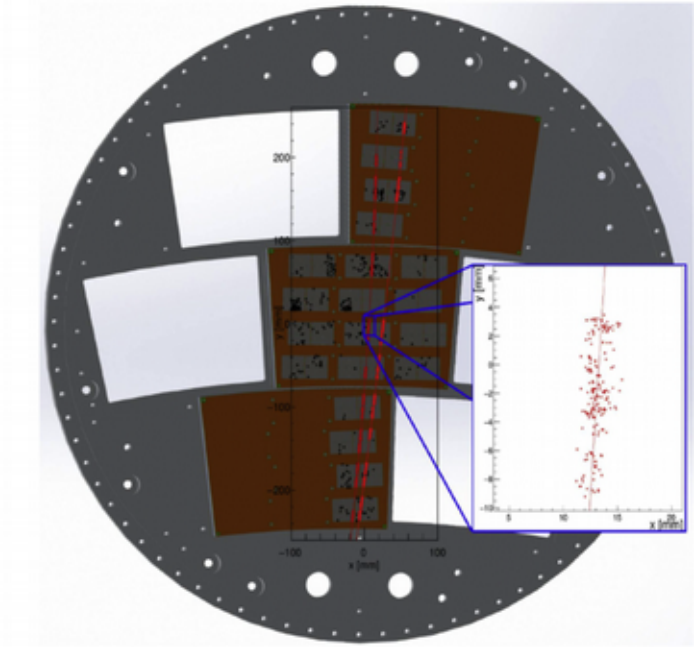
SRS Timepix

Implementation in framework of feasibility study for a pixel-TPC at ILC
→ InGrid/GridPix readout









M. Lupberger et al.,Implementation of the timepix ASIC in the scalable readout system." Nucl. Inst. and Meth. A830 (2016): 75-81.

SRS SiPM

NEXT readout system

SRS in ATCA, upgrade for next White detector

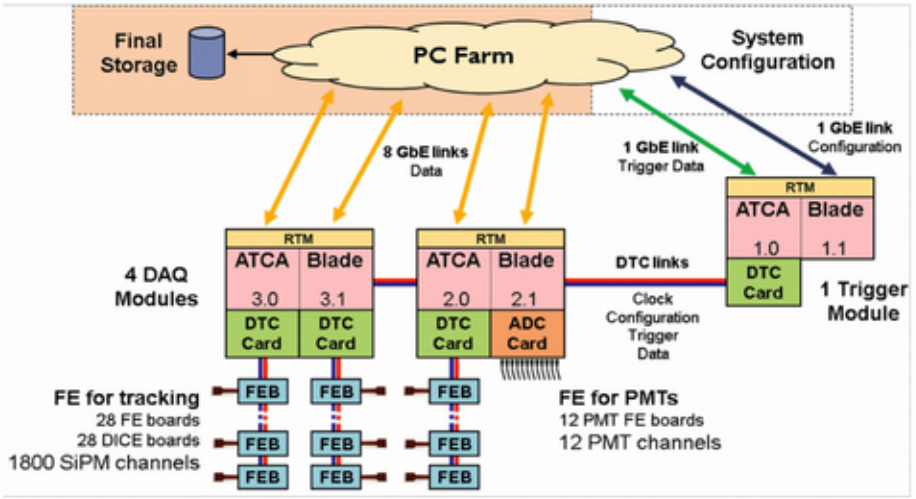
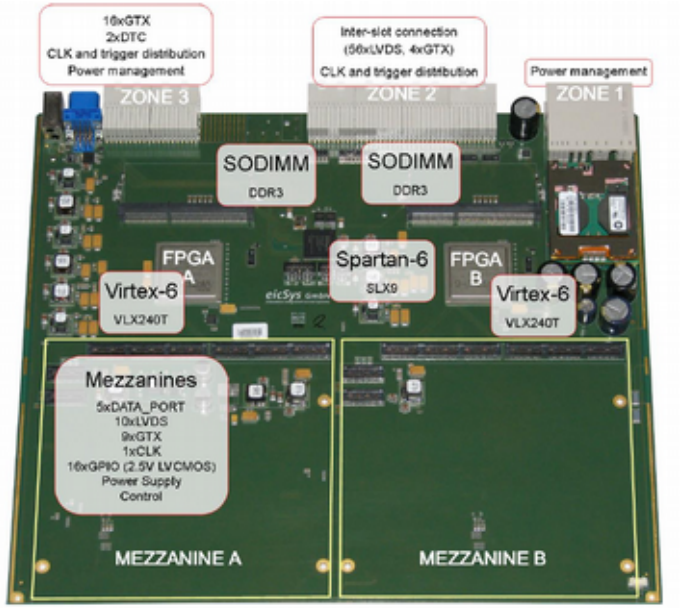
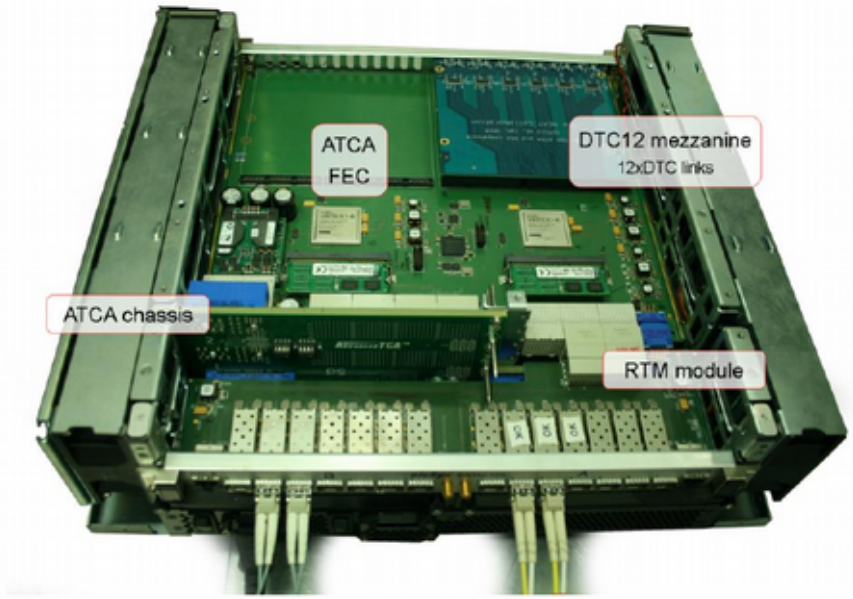


Figure 4.10: *NEW DAQ and trigger system architecture.*





F. Monrabal et al., The Next White (NEW) detector, arXiv preprint arXiv:1804.02409 (2018), subitted to JINST.

Other readout systems in HEP (fraction)

Silicon pixel specific:

The University of Bonn has developed a test bench for the FE-I3 ASIC called the **USBpix** , which has found application in the whole silicon pixel R&D community. Over 100 systems have been produced. An FPGA board called Mulit-IO with custom firmware is controlled via a USB micro controller. It connects to an adapter board, that can connect different front-end versions like the FE-I4 on a DUT (Device Under Test) board or multi-chip boards. A DAQ (Data AcQuisition) and testing framework (basil) that also contains libraries with FPGA firmware blocks and lab equipment drivers was developed alongside as well as a readout and analysis software (PyBar). The system was and is continuously upgraded with new versions of boards and adapter cards for new ASICs. Using the libraries and know-how. The same group currently develops a test system for the RD53A ASIC on basis of the USBPix system . The Multi-IO board (MIO3) is again custom design, but the FPGA (Kintex-7) on this board can be mounted as a commercial module. The data transmission to the computer is realised by SFP+ 10 Gb/s Ethernet.

YARR (Yet Another Rapid Readout) is another system designed for the test of the FE-I4 based on a commercial PCIe (Peripheral Component Interconnect express) card with FPGA, that can be directly inserted into a computer. The card can connect daughter boards via an FMC (FPGA Mezzanine Card) connector with up to 16 pixel modules. The connection to the computer can theoretically reach 1 Gb/s per lane on up to 16 lanes in PCIe 3.0 (latest version PCIe 5.0: 4 Gb/s lane rate, standardisation expected 2019) . A hardware upgrade for the RD53A ASIC is foreseen. The philosophy of this system is to pipe all data from the front-end into the PCs memory as fast as possible and rely on modern multi-core CPU architectures for data processing. This is due to the fact that despite the power of FPGAs in data processing, the firmware development and maintenance is time- and manpower consuming, while software design is more common and flexible. This approach is different to a traditional readout system where the data is preprocessed by an FPGA-based readout card first and the data is then sent to a computer through a cable link.

RCE (Reconfigurable Cluster Element) is a modular larger scale readout system developed at SLAC for the ATLAS upgrade. It was used in the first generation for R&D and testing of the ATLAS pixel IBL. The latest version became the readout of the ATLAS CSCs (Cathode Strip Chambers) when they were upgraded in LS1, the new AFP (ATLAS Forward Proton Detector) in the 2016 run and other experiments outside CERN. The system is designed for ATCA (Advanced Telecommunication Computing Architecture, a shelf standard with several slots for cards, powering and bus system for interconnection) as host platform with a main carrier board that can host several RCE mezzanine cards, which makes the system modular. An embedded 10 Gb/s Ethernet switch provides communication between the different RCEs and interconnects. On one side of the board an internal interface can connect to an application specific RTM (Rear Transition Module) which provide the physical interface to the detector, while the other side is the external interface with 8 x 10 Gb/s Ethnernet SFP+ links. The RCE holds one of the first Xilinx Zynq SoC, DDR3 memory and connectors to the main board. Each slot of an ATCA crate can be equipped with a main board/RTM combination such that the system can be scaled up. For smaller table-top test systems, a version of the main board for a single RCE mezzanine card called HSIO II with an Artix-7 FPGA exists, which does not require an ATCA crate. the data acquisition computer farm. The reference clock, time stamping and slow control would be transmitted in the direction from the Backend towards the FE.

Other readout systems in HEP (fraction)

In the framework of the development of the vertex detector readout chip (*CLICpix)* for the CLIC experiment, a versatile and modular readout system named **CaRIBOu** (Control and Readout Inner tracking Board) is developed by the CLICdp collaboration. It aims to support a wide range of current and future ASICs due to minimal integration effort, should be flexible and provide the performance to be used for laboratory measurements and test beams and relies on the maintenance of the collective effort community simplified by open source hardware, firmware and software. The hardware consists of three modules: An application specific chip board, a common interface board (CaR) and a common SoC board. Chip boards with minimal functionality are available for ClicPix2, FE-I4 and two other ASICs. The interface board provides power, communication standards, ADCs (Analogue to Digital Converters) for monitoring and is connected to the chip boards by a 320 pin connector on one side and to the SoC board with an FMC connector on the other side. Optionally, the FMC connection can be achieved via cables up to about 50 cm length, such that the SoC can be placed outside irradiated areas. The SoC board is a commercial Xilinx Zynq evaluation kit (upgrade to Zynq Ultrascale+ kit foreseen) with 10 Gb/s SPF+ output, which can host two interface boards. The data acquisition software runs directly on the Linux operating system of the SoC processors and is controlled via SSH (Secure Shell) through a 1 Gb/s link to a computer. The hardware comes with a firmware and software framework with user friendly abstraction levels.

SPIDR (Speedy PIxel Detector Readout) is a flexible general-purpose system developed at NIKHEF (Dutch National Institute for Subatomic Physics) for the Timeix3 and Medipix3 originally to characterise and test those ASICs. It was first implemented on a Virtex-7 Evaluation kit. Later, a custom board called Compact-SPIDR with an ARTIX-7 FPGA. Both boards have a 10 Gb/s SFP+ output and connect to a chip carrier mezzanine card via an FMC connector. The FPGA firmware consists of firmware blocks like the the UDP (User Datagram Protocol) offload block for the Ethernet communication, an open source soft core processor called LEON3 and a ASIC specific control and trigger block. On the software side, an API (Application Programming Interface) was developed to control the SPIDR from a PC. This modular firmware and software structure simplifies the implementation of other ASICs, which is foreseen for the future. SPIDR became a test system for the LHCb VeloPix and is the readout of a Timepix3 beam telescope which is used for the characterisation of other ASICs.

Kartherine, the Ethernet Embedded Readout Interface for Timepix3 is developed by the Institute of Experimental and Applied Physics of the Czech Technical University in Prague and the Faculty of Electrical Engineering of the University of West Bohemia in Pilsen in the tradition of previous USB based Timepix readout device. The USB link has been dropped for reasons of link bandwidth, scalability and cable length. Katherine is a compact box of 10 cm x 8 cm x 2.8 cm that connects to a single chip carrier board via 68-pin VHDCI (Very Hight Density Cable Interface) directly or by an extension cable. The readout rate of the TImepix3 is limited by the 1 Gb/s Ethernet, which was selected as it is still dominantly used in network architectures. The design goal of the device is not readout speed, but compactness and simple remote control, such that it can be used without maintenance in areas without human access like intensely radiated areas in a reactor. The PCB inside the box holds an Altera SoC FPGA with a dual core embedded processor, DDR3 memory, ADCs and voltage regulators. The device is supported by the Pixelman Software package that evolved with the developments of these groups.

Other readout systems in HEP (fraction)

Large experiments

For the upgrade of the ATLAS readout system, **FELIX** (Front End LInk eXchange) aims to integrate all sub-detectors in LHC Run 4 after LS3 in 2025. It should be the interface between the custom links and commercial network standards. After LS2, it will already be used for the NSW and Lar (Liquid Argon Calorimeter) and now serves as a test system for the pixel and Tile Calorimeter R&D. The goal is to bring the readout, clock distribution, slow control and triggering system, which was designed with the capabilities of electronics of around 2005, to the current state of the art. The main hardware component will be a custom PCIe card with a powerful FPGA, of which several can be placed in a host PC with large processing and memory resources and custom software that connects to a high bandwidth network via another PCIe card. The global ALTAS clock, time, trigger and control will be induced a the FELIX PCIe card FMC mezzanine. The sub-detector electronics will be connected via GBT. The current prototype FLX has 24 such input ports and uses a 16 lane PCIe 3 (a total of 128 Gb/s) as output with a Kintex Ultrascale as FPGA. There is a mini Felix for laboratory tests on a Virtex-7 development kit and the system has attacked interest outside the ATLAS community, among others by the ProtoDUNE collaboration.

The LHCb experiment will change its readout philosophy in LS2 from a hardware trigger to full and live readout of all data from the detectors into a computer-baed online event builder with high level software trigger. The InfiniBand network technology will be used to transfer a total of about 32 Tb/s of data. The network will consists of about 500 nodes, each realised by a computer with 100 Gb/s output, two CPUs and a custom PCIe board called **PCIe40** . One of the CPUs manages direct memory access for the PCIe40 card, while the other one builds events. The PCIe boards host one of the most powerful FPGAs on the marked, an Altera Arria10 to treat about 480 Gb/s of data.

For the **ESS** (European Spallation Source), which is currently constructed in Lund to become the worlds brightest neutron source, a **new readout system** will be designed as one of the In-Kind contributions from the United Kingdom, which should be generically usable for all detectors of the different instruments and beam monitors . A large fraction of those will employ the VMM readout ASIC. The current design foresees to use commercial development boards in a three level hardware architecture with FE (Front End), master FE and Backend. The FE is the detector interface and holds the ASIC, ADC or other digitiser elements, an FPGA and an interface for up to 6.25 Gb/s connected to a master FE or another FE in a ring network. The master FE is a commercial Evaluation board like a Xilinx Kintex Ultrascale kit with 10 Gb/s SFP+-. Several of those boards would be connected to the Backend, which could be a Xilinx Virtex-7 Ultrascale+ evaluation board with 100 Gb/s QSFP+ interface to

Other readout systems in HEP (fraction)

Small and medium size experiments with dedicated readout:

In the framework of generic R&D for a X-ray polarimeter TPC (Time Projection Chamber) in China, a special sampling ASIC called **CASCA** (Charge Amplifier and Switch Capacitor Array) and a dedicated **readout system** are developed. The system consists of three parts: The ASIC card with the 32 channel readout chip, an edge-mounted adapter card that digitises the data and transmits it via SRIO (Serial Rapid IO) at 6.25 Gb/s on multiple lines through an HDMI cable to the master controller card. This card holds a powerful Xilinx Kintex Ultrascale FPGA, can connect up to eight adapter cards and transmits the data via 10 Gb/s SPF+ to the computer.

The **Mu3e** experiment will search for lepton flavour violation in the rare decay of the muon to three electrons. The detectors will employ HV-MAPS (High Voltages Monolithic Active Pixel Sensors) and a dedicated readout system to evaluate those in the laboratory and test beams was designed. The ASIC is mounted or bonded on a carrier card that provides stable power supply, test pulses and transmits and receives data through several serial links, each at 1.25 Gb/s to a commercial Altera Stratix IV development kit that is PCIe mounted into a computer and can connect at most two ASIC cards. The system can be scaled for a total of eight ASICs for a beam telescope.

AGATA (Advanced GAmma Tracking Array) is a European gamma-ray spectrometer used to study the structure of atomic nuclei. For the second phase of this experiment, new electronics will be designed that should be backward compatible, cost effective, modular to allow for further upgrades and use modern commercial components .The current electronics is already based on digitisation of waveforms from HPGe (High Purity Germanium) crystals with a 100 Msamples/s ADC for pulse shape analysis, a 2 Gb/s link per channel and a trigger system to select valid events. Recent FPGA technology allows for preprocessing of several channels, while high bandwidth Ethernet provides higher readout rates which results in less electronic components and cost reduction. The design is based on a main board with a Xilinx Kintex Ultrascale FPGA and several mezzanine cards all connected via FMC. That way, for further upgrades each component can be replaced individually. There is one type of card for receiving data from the current 2 Gb/s links, one for receiving the global trigger, one for sending data through a 40 Gb/s to 100 Gb/s Ethernet link.

Other readout systems in HEP (fraction)

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