ToASt : Torino Amplifier for Strip detectors

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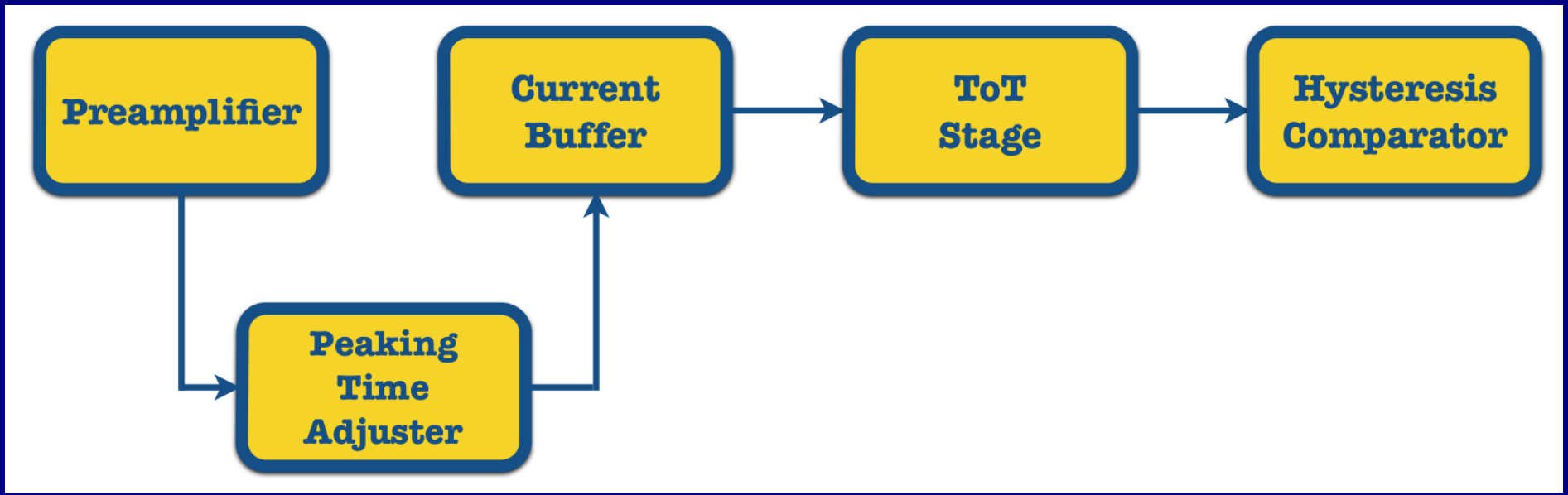
ToASt development background

- Developed for the PANDA MVD strip detector readout
- Possible use in COMPASS under investigation
- Analogue front-end from the PASTA ASIC
- Digital back-end derived from the ToPiX ASIC
- Technology : CMOS 0.11 μm

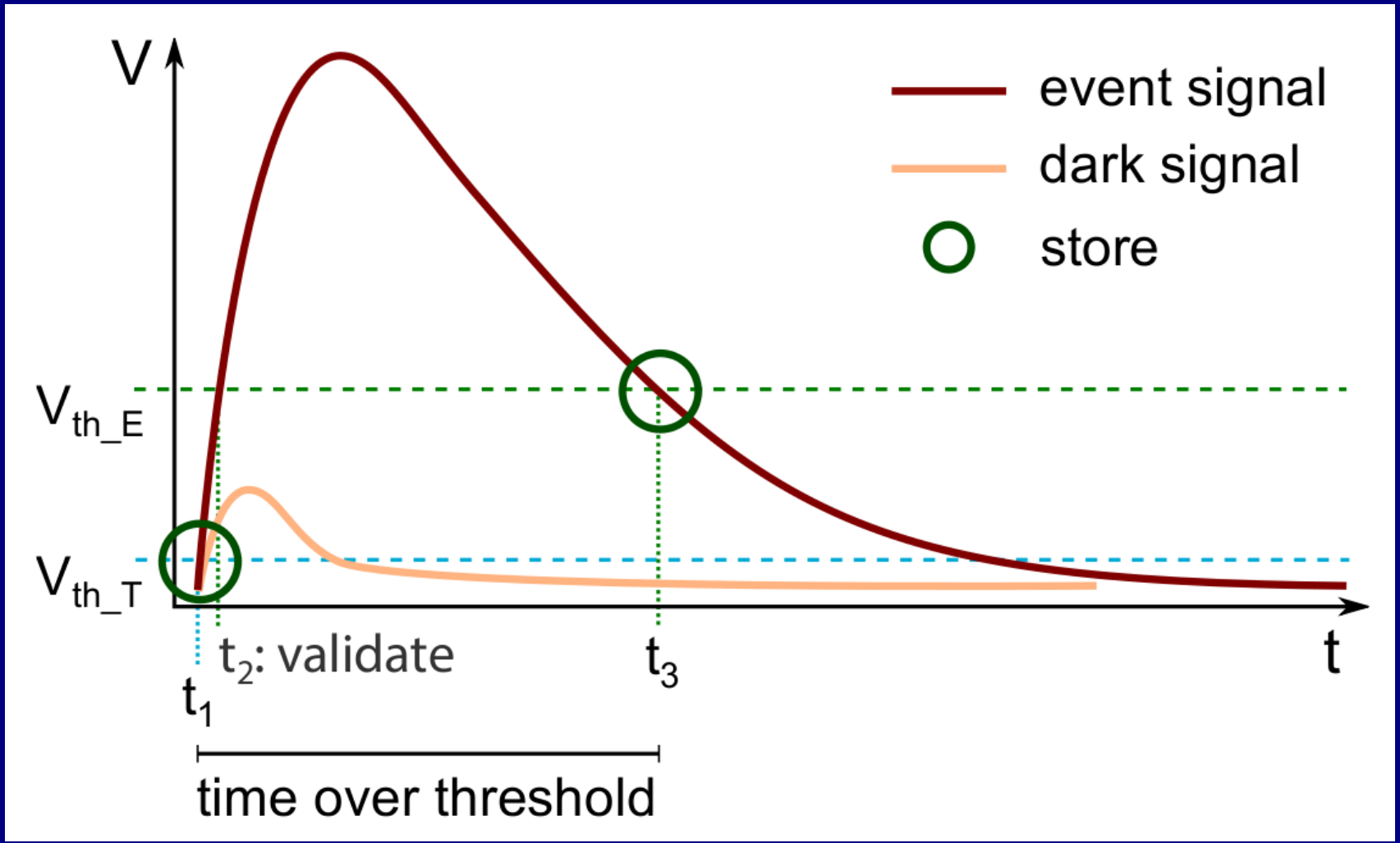
Specifications

Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	100 (?)	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.2×3.5		mm^2
Pads position	On two sides only		

ToASt analog FE



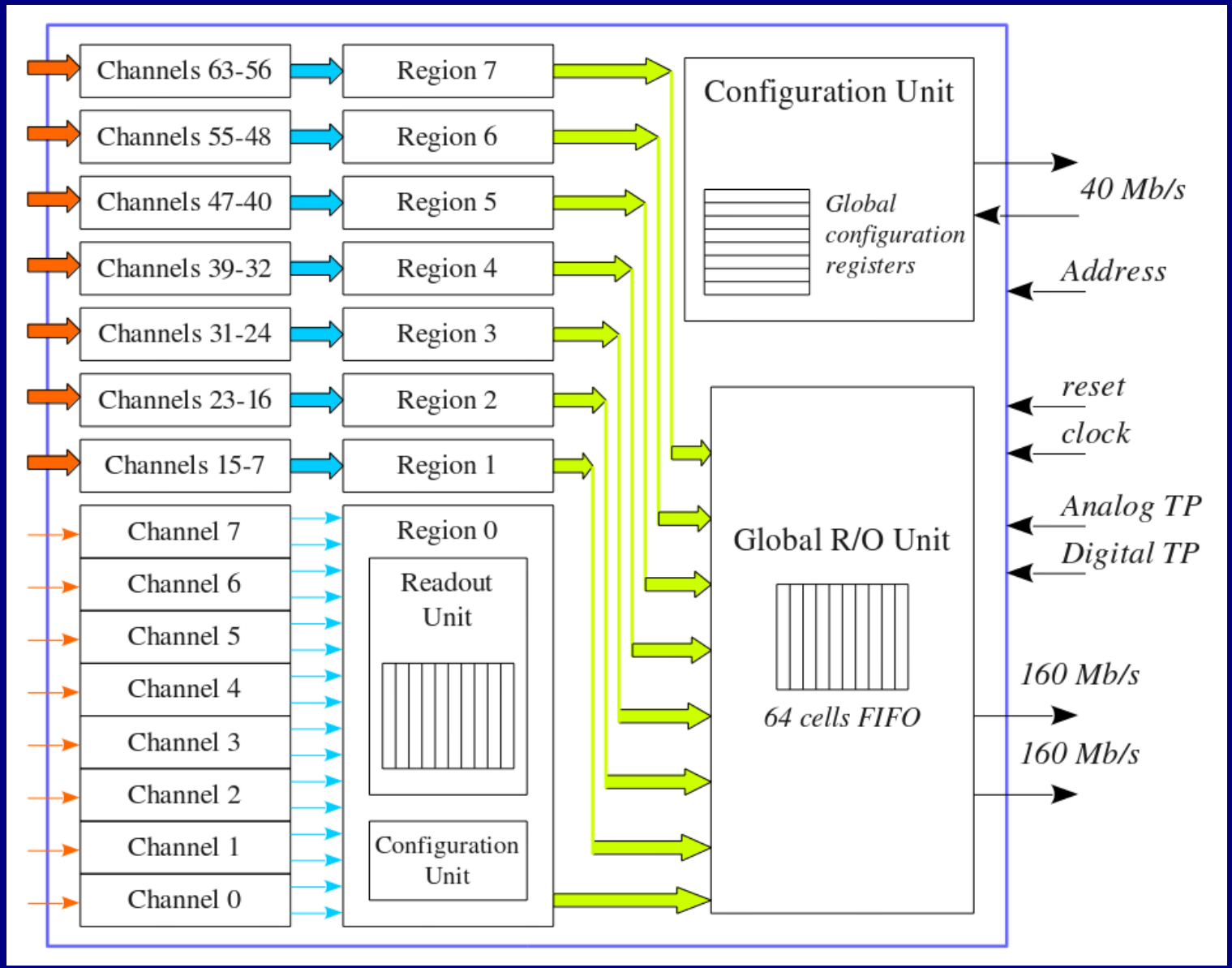
Double threshold logic



ToASt main characteristics

- 64 input channel channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 40 Mb/s
- SEU protection for registers and FSM
- CMOS 0.11 μm technology

ToASt architecture



ToASt preliminary pinout

Pin name	Direction	Description
in[63:0]	In	Analog inputs
SyncReset	Rx	Synchronous reset
ChipAddr[6:0]	In	Chip address
TestPulse	In	Digital test pulse
CfgRx	Rx	Configuration receiver
CfgTx	Tx	Configuration transmitter
TxOut_0	Tx	Data serial output 0
TxOut_1	Tx	Data serial output 1

Channel configuration - *Preliminary*

Register	Bits	Function
0	11:8	*Reserved for future use*
0	7	Channel mask
0	6	Delay enable
0	5	Calibration enable
0	4:0	ToT discharge current calibration DAC
1	11:10	*Reserved for future use*
1	9:5	Energy threshold calibration DAC
1	4:0	Time threshold calibration DAC

WARNING ! This is not the final assignment - Work in progress...

Global configuration - *Preliminary*

Register	Name	Function
0	11	*Reserved for future use*
0	10	detector polarity
0	9	leading edge-only mode
0	8	single threshold mode
0	7:6	*Reserved for future use*
0	5	Tx 1 enable
0	4	Tx 0 enable
0	3:2	*Reserved for future use*
0	1	Time stamp counter Gray mode
0	0	Time stamp counter enable
1	11:8	*Reserved for future use*
1	7:0	Region disable

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Project status

Task	Status
Analogue FE optimization	ongoing
HDL code of the channel logic	done
HDL code of the region logic	done
HDL code of the chip readout logic	done
HDL code of the chip configuration logic	done
HDL code of the TMR protected serializers	done
SEU protection of registers, counters and FIFOs	done
SEU protection for FSM	to be done
Header and trailer insertion with CRC calculation	done
Synthesis	ongoing
P&R	to be done

Summary

- Development for the PANDA MVD strip detector :
  - 64 channel ASIC
  - Configurable for both input signal polarities.
  - Time of Arrival measurement with system clock resolution
  - Charge measurement via Time over Threshold
  - Local FIFOs for data de-randomization
  - 2$\times$160 Mb/s serial outputs
- FE and BE design in advanced status
- Submission foreseen for April 2019
  to be confirmed - delays in CAD license renewal are delaying the design.