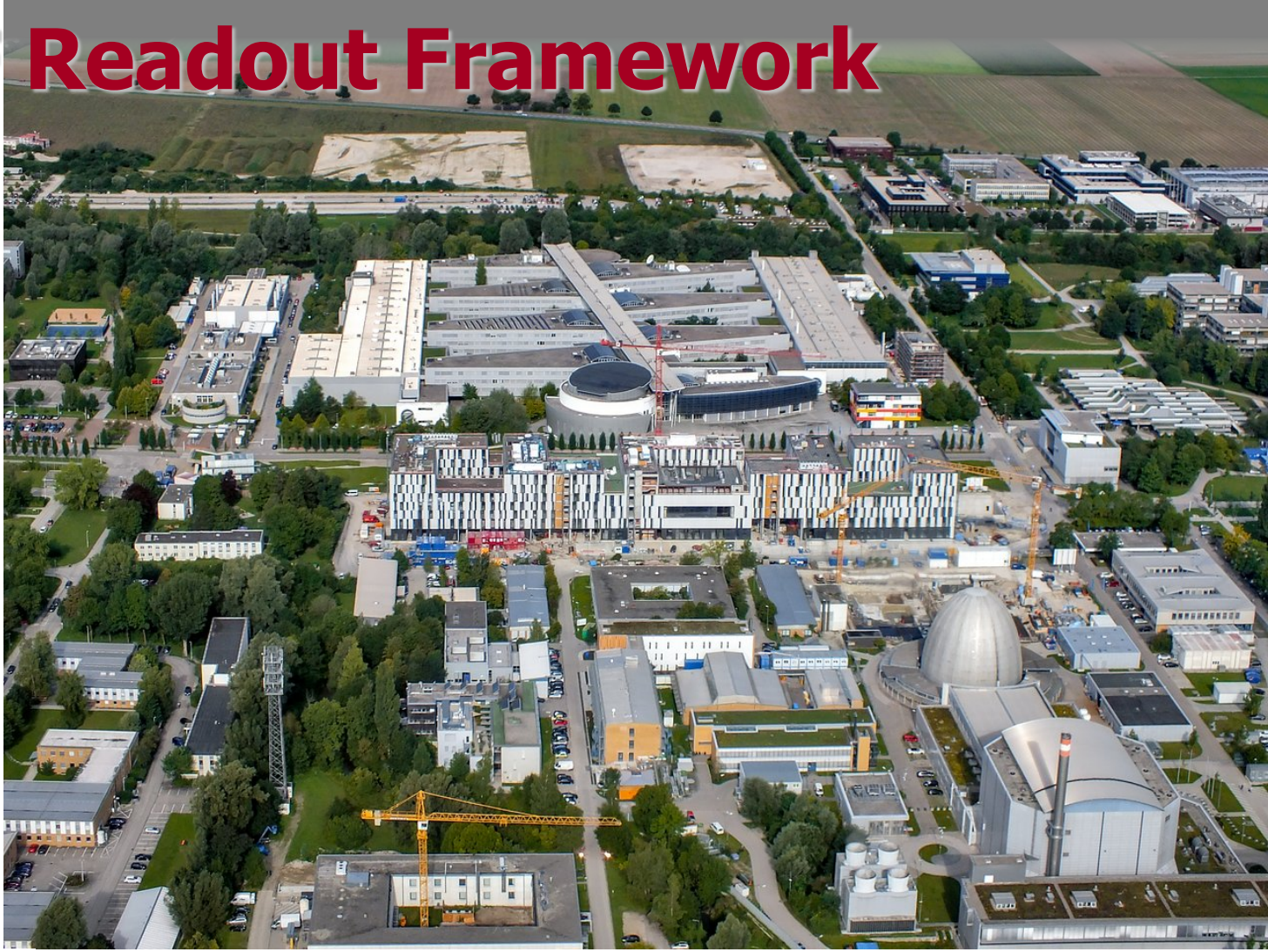
GANDALF Readout Framework



Bundesministerium
für Bildung
und Forschung

Masse und Symmetrien nach der
GRK 2044
Entdeckung des Higgs-Teilchens am LHC

UNI FREIBURG

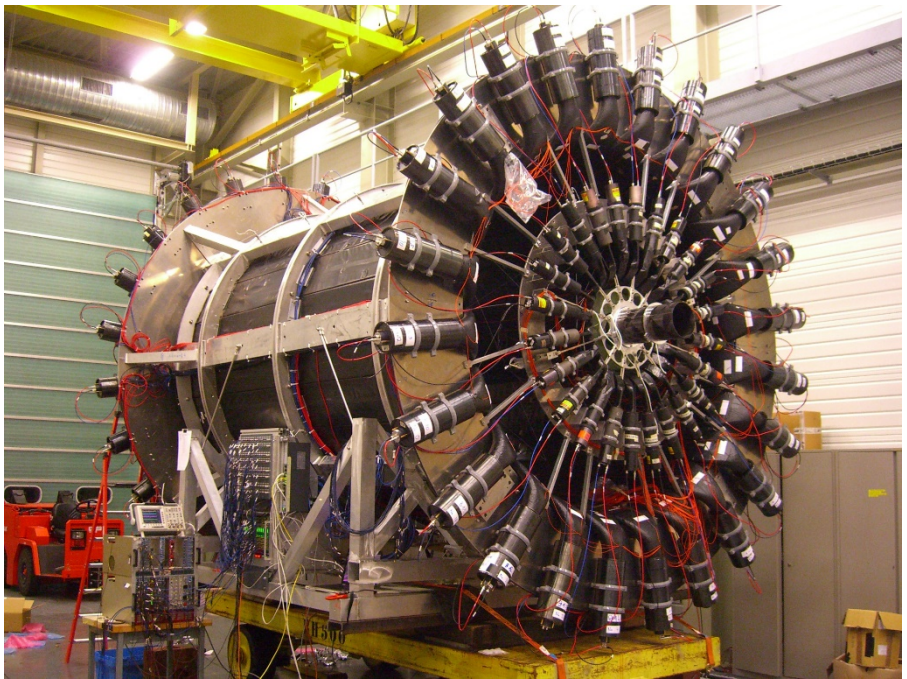
Horst Fischer / Matthias Gorzellik

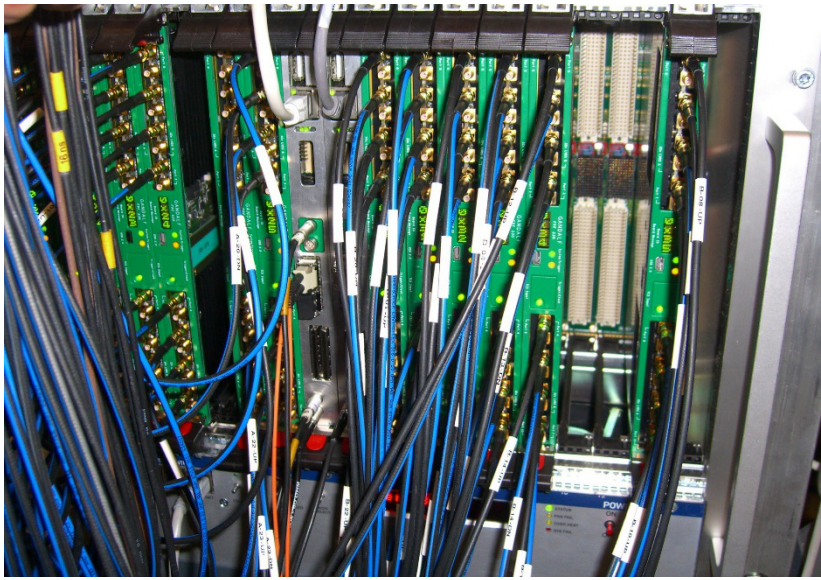
DAQFeet Munich, 10.2.-12.2.2019

Readout

Objectives: (defined 2009)

- digitization of analog signals from 96 PMs for TOF recoil proton detection for COMPASS DVCS measurement
- Two measurements on rising edge (single PE rise time 3.5ns)
- Double pulse separation
- 10 ENOB dynamic range, V_{max} = 2V or V_{max}= 4V
- Trigger generation based on pattern, time and energy loss
- Later, CATCH-F1 TDC replacements complemented the shopping list





- **Details: https://gandalf-framework.web.cern.ch/**

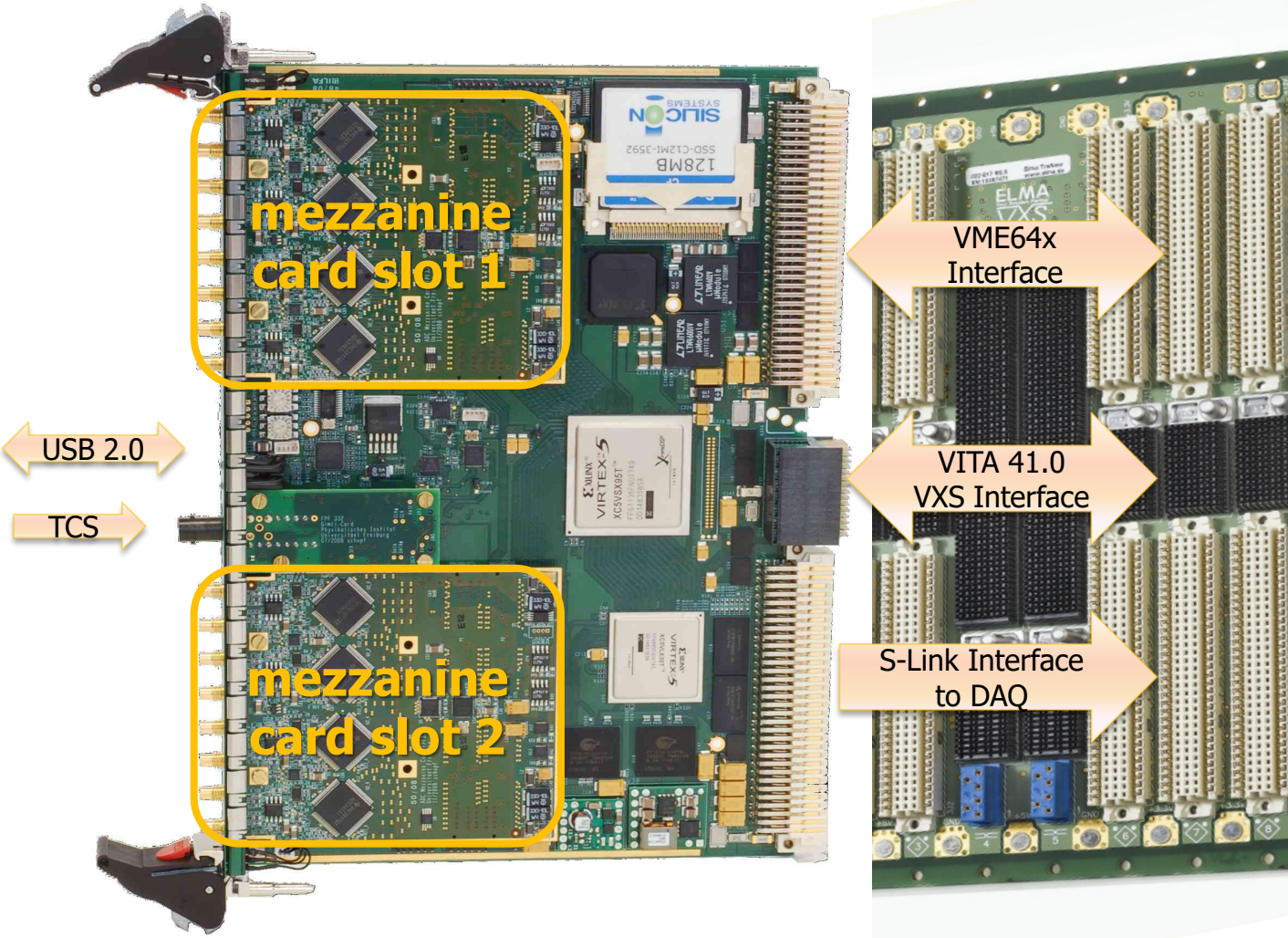
The GANDALF module

Generic **A**dvanced **N**umerical **D**evice for **A**nalog and **L**ogic **F**unctions

Virtex-5 SX95T FPGA for Data Processing:
60k CLB flip-flops,
8 Mbit Block RAM,
640 DSP Slices,
500 MHz

Virtex-5 LX30T FPGA for Memory Control & Data Output:
20k CLB flip-flops,
1.2 Mbit Block RAM,
500 MHz

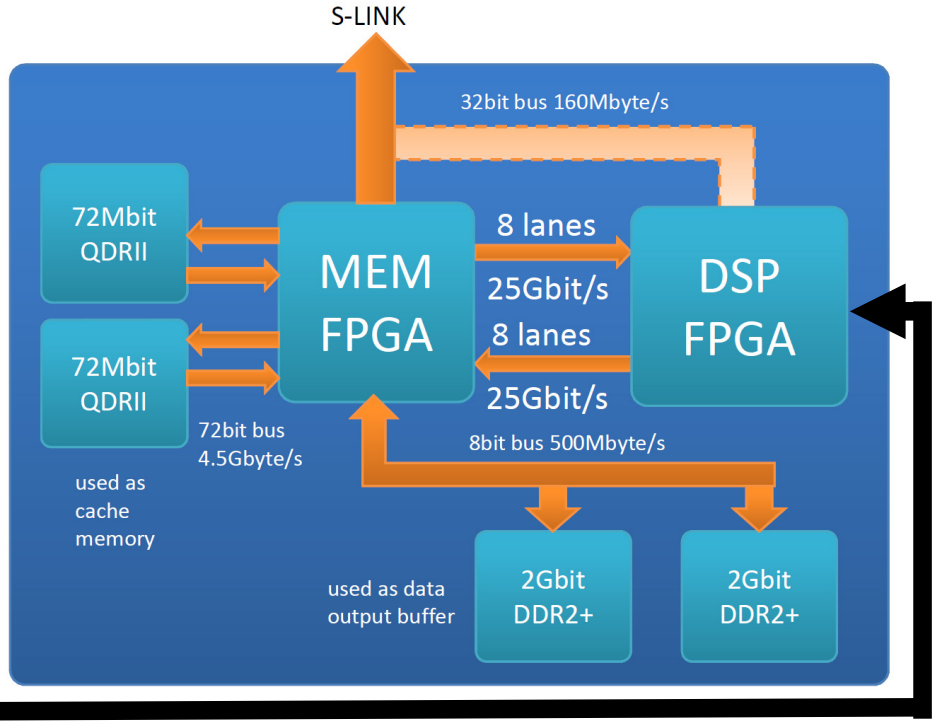
Memory:
144 Mbit QDRII+,
4 Gbit DDR2

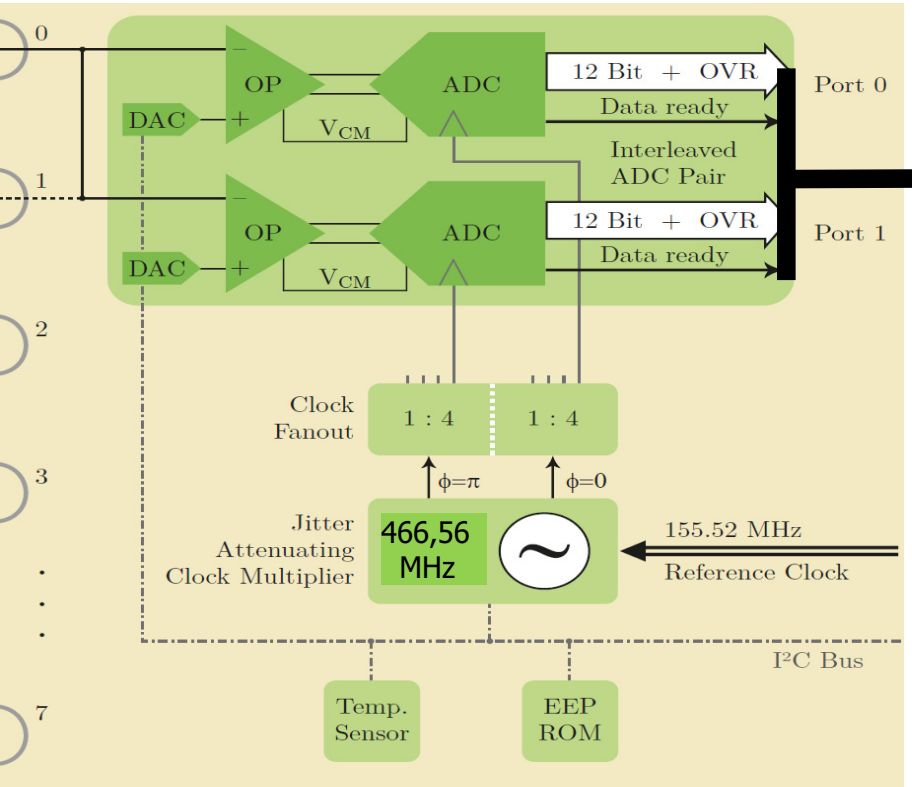


GANDALF - Sampling ADC

DSP FPGA:

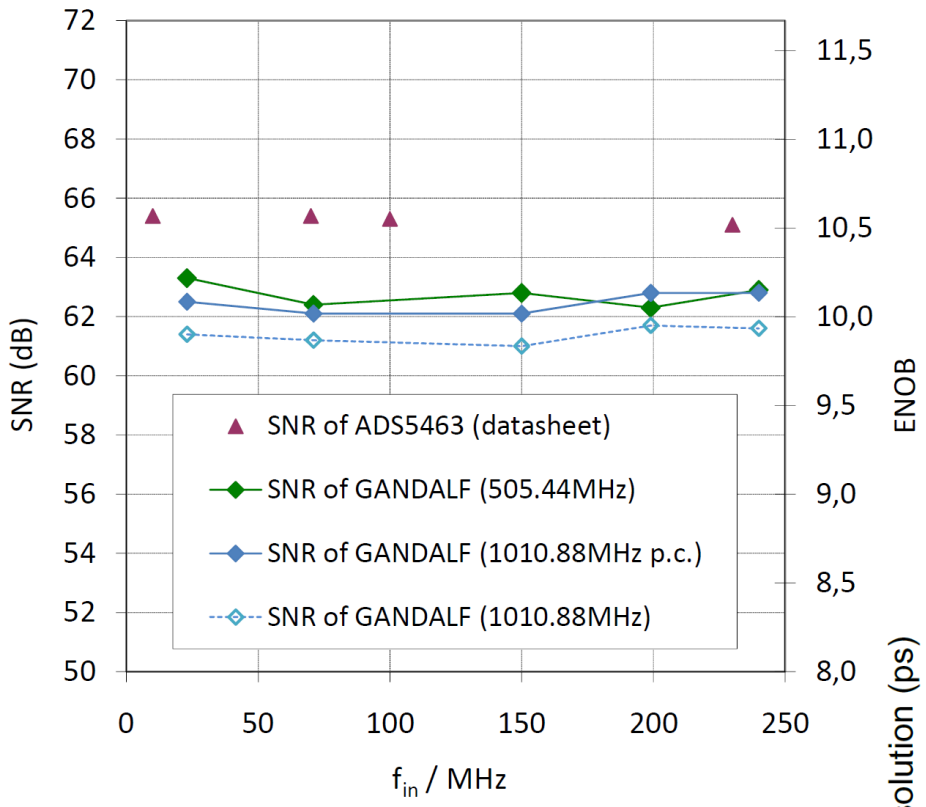
- Zero suppression
- Feature extraction (time & amplitude)
- Event selection
- 2017: Firmware for MEM FPGA

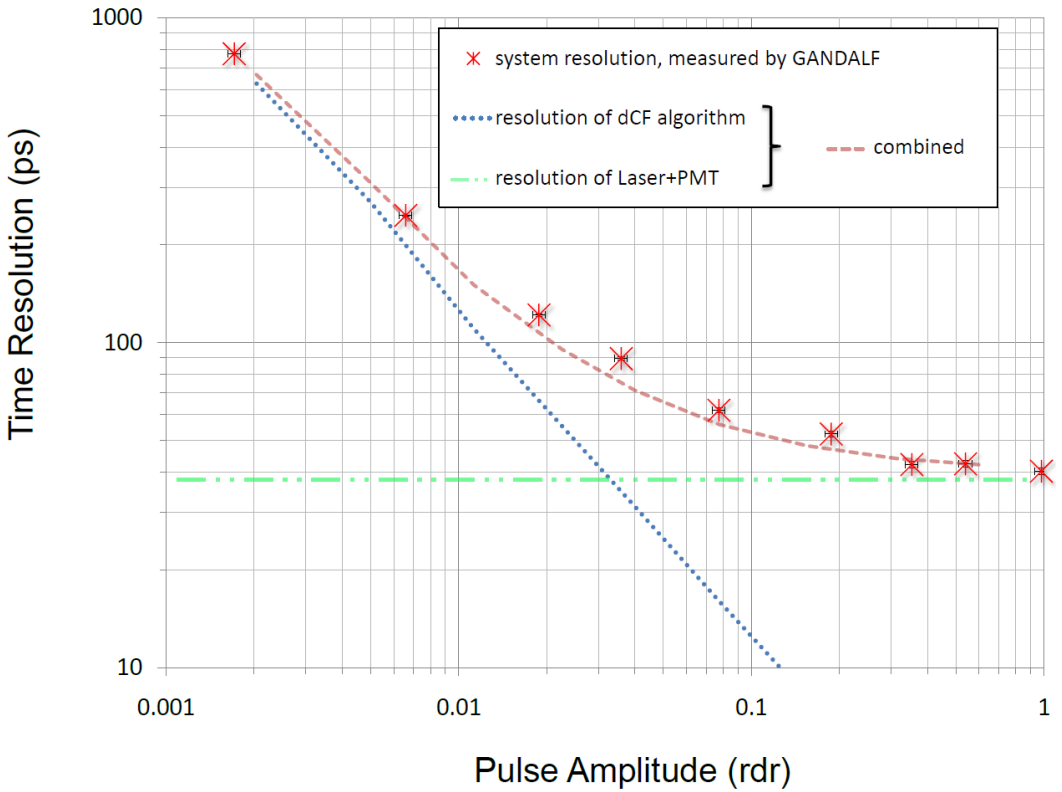




- 2012 Problem: phase recovery of Jitter attenuator (SI5326)
- 2015: major rework of Firmware
- Beamtimes 2016 & 2017 VERY stable data takings
- Event selection in MEM FPGA

Performance





Recent Firmware: Self Triggered Sampling Mode

- Self-trigger via ToT /external triggers allowed (monitoring)
- Configurable "trigger condition", i.e. # samples needed for ToT,
  # samples recorded before and after trigger
- Individual configuration of thresholds and baselines for each channel

- on-board or external reference clock (currently 20 MHz – 50 MHz)

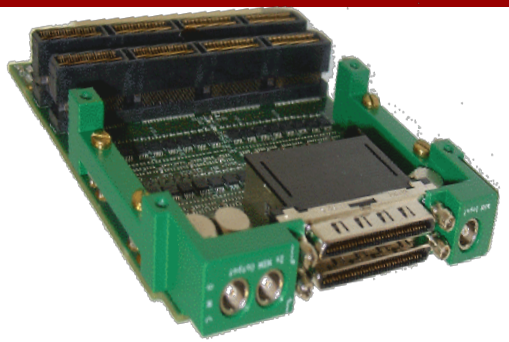
- 8 / 16 independent channels,
- 12 bit amplitude resolution, 10.5 ENOB
- 932 MS/s / 466 MS/s
- 16K samples channel-buffer (corresponds to ~16 µs / 32 µs)

- Common readout-buffer: 128K samples (round-robin collection of channels)

- configuration and readout via USB (data rate ~20 MB/s) or VME
- combination of multiple GANDALF-modules using USB3 (5GBit/s, optical) switch;

GANDALF – 128 channel TDC

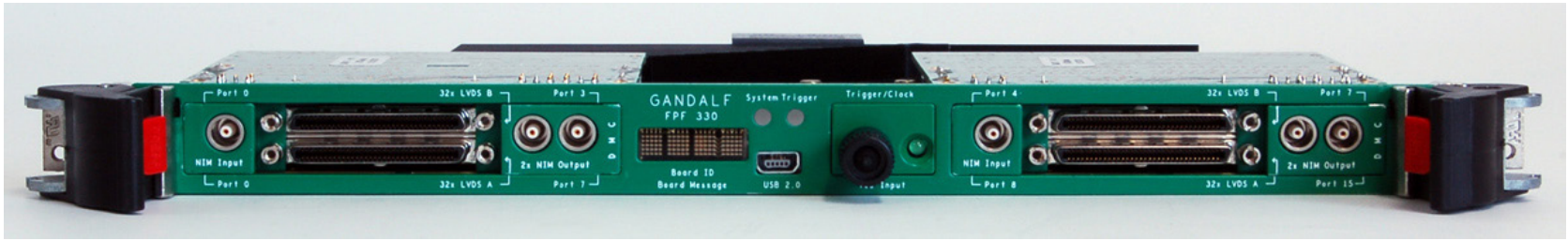
GANDALF with digital I/O



- 128 differential inputs or outputs

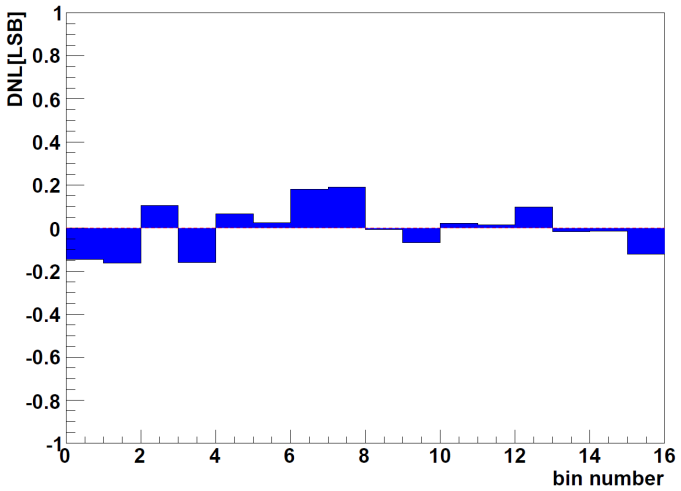
- module functionality is free programmable in the FPGA
- e.g. time-to-digital converter, scaler, mean-timer, coincidence matrix, pattern generator

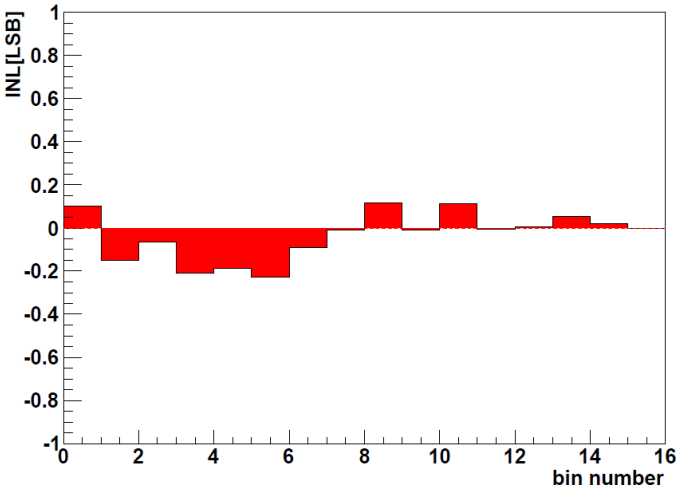
- **combinations of these functionalities are possible for cost efficient design**



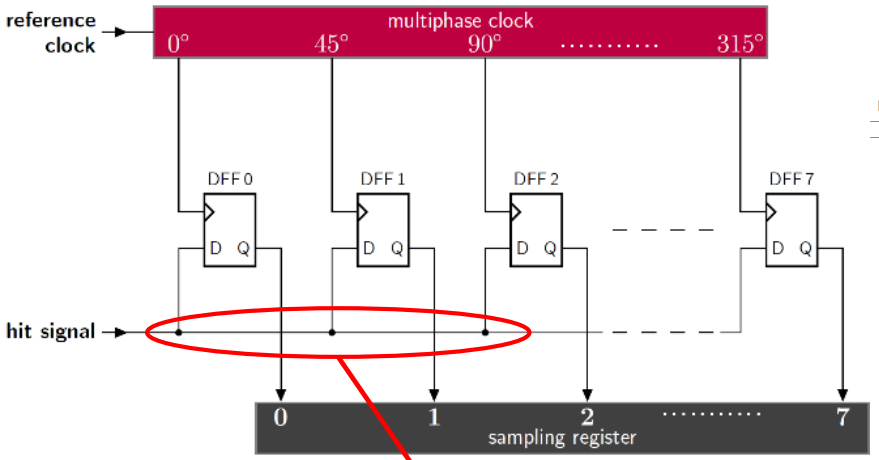
M1-TDC Firmware

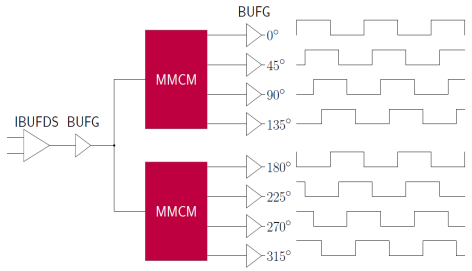
- 128 channels TDC
- Digitization step 160ps
- 16 Flip-Flop stages





TDC Implementation





- phase shift

$$\Delta\phi = \frac{360^\circ}{8} = 45^\circ$$

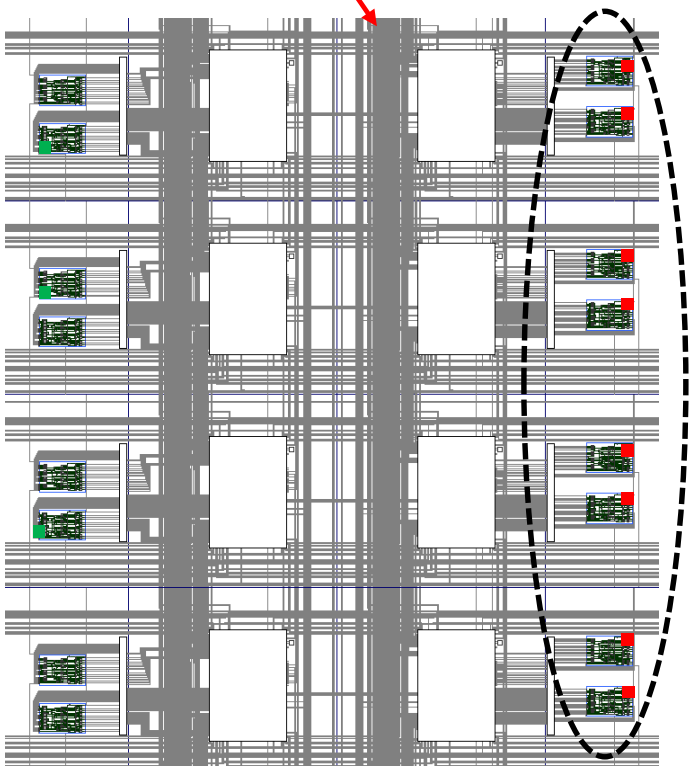
- $f_{TDC} = 311.04\ \text{MHz}$
- $t_{\text{LSB}} = \frac{1}{311.04\ \text{MHz}} \approx 402\text{ps}$

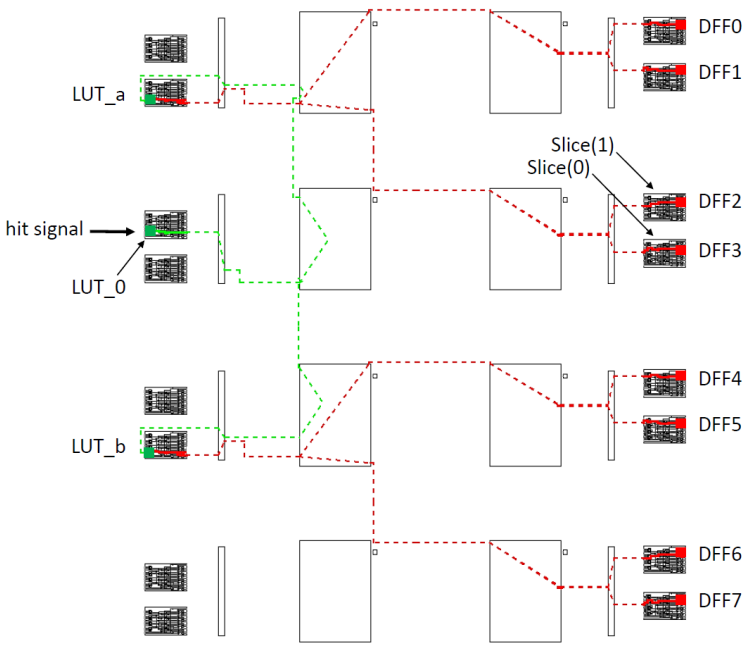
optimized by interactive routing!

- routing skew < 20ps
- clock skew < 35ps

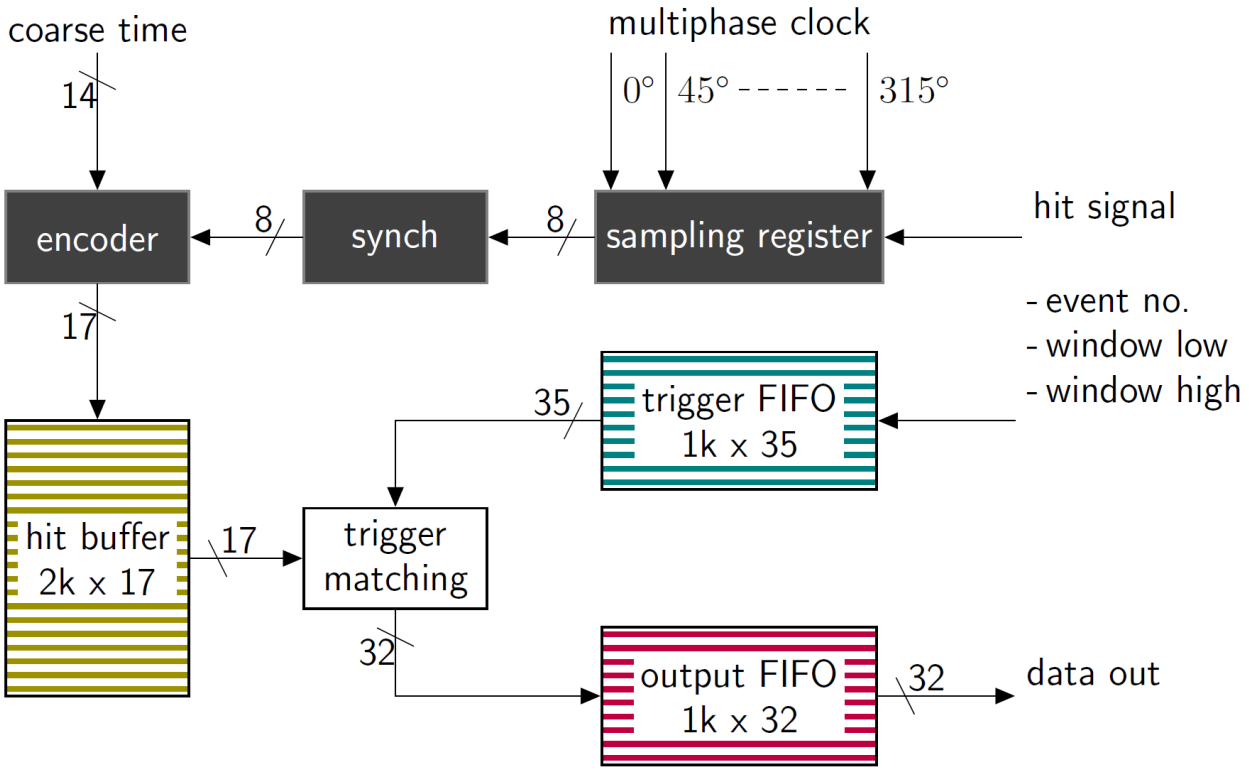
$\Big\} \ll t_{\text{LSB}}$

8 TDC flip-flops

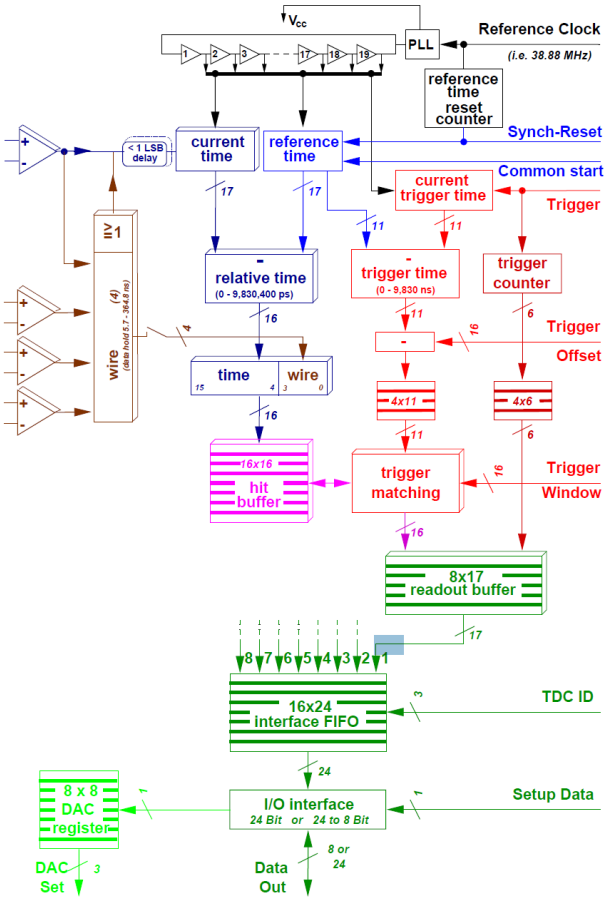




Sketch of a Single M1-TDC Channel



F1 TDC design:



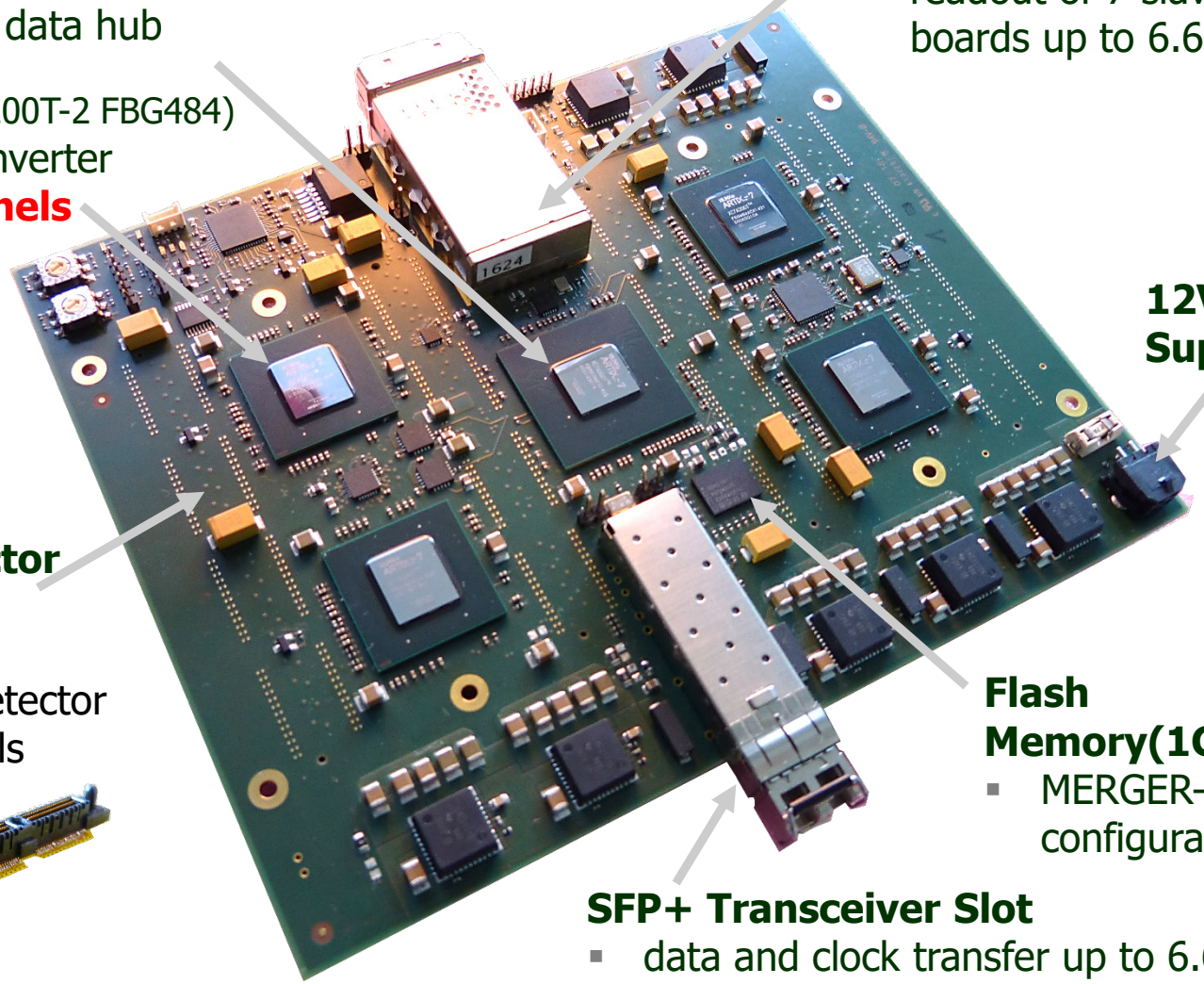
- M1 TDC core → CATCH-F1 compatible design
- Identical data format to F1 → simplified decoding
- Probably trigger-less R/O possible?

The ARAGORN Front-End

MERGER-FPGA (XC7A200T-2 FBG676)
- interface to optical modules
- local event builder
- data hub

CXP Transceiver Slot
- readout of 7 slave boards up to 6.6 Gb/s

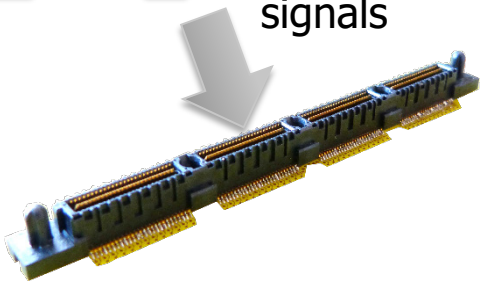
4x TDC-FPGA (XC7A200T-2 FBG484)
- Time-to-Digital Converter
- 4x96 = **384 channels** per board



12V Power Supply

4x 208-pin connector (on solder side)

96 detector signals



Flash Memory(1Gb)
- MERGER-FPGA configuration

SFP+ Transceiver Slot
- data and clock transfer up to 6.6 Gb/s

ARAGORN Implementation

ARAGORN Master

Fiber-Optic Fanout Cable

CXP Transceiver Module
- hot pluggable
- 850 nm VCSEL array technology

7x ARAGORN Slave

interconnect 8 boards through star topology
- identical board layout
- master/slave role
- readout **3072 channels**

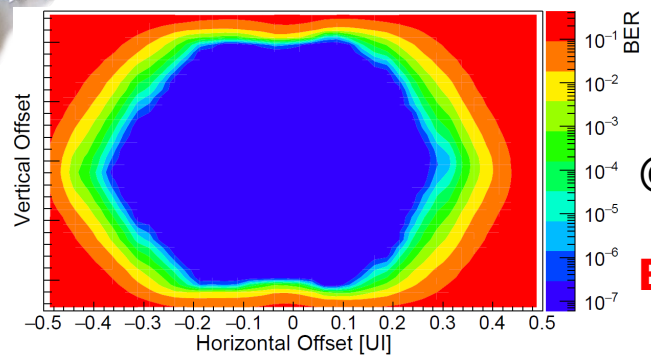
ARWEN (4x SFP+)

VME64x

VXS

S-LINK

GANDALF VXS/VME64x



@ 6.2208 Gb/s:
~20 hours without errors
Bit Error Rate $<10^{-14}$ at 99% *CL*

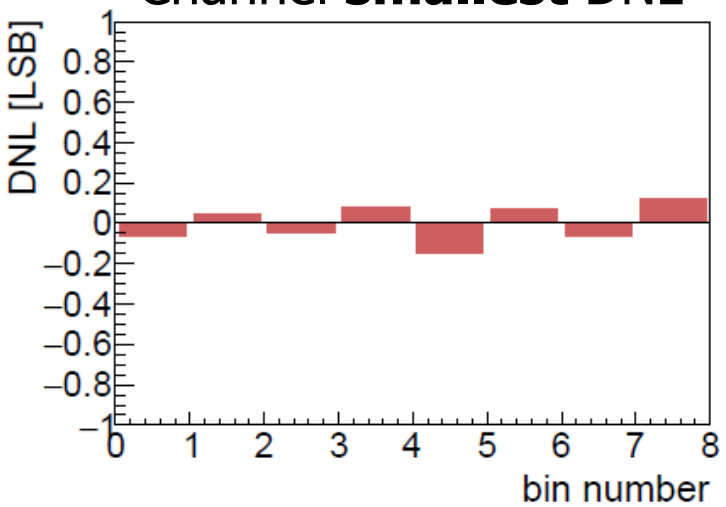
ARAGORN Specs

- ✓ Channels / board: 384
- ✓ $t_{\mathrm{LSB}} = \frac{1/311.04\ \mathrm{MHz}}{8} \approx 402\mathrm{ps}$
- ✓ Double hit resolution: 3.2ns
- ✓ Rate capability: 34MHz
- ✓ Sensitivity: rising/falling/both edge
- ✓ Dead time: none

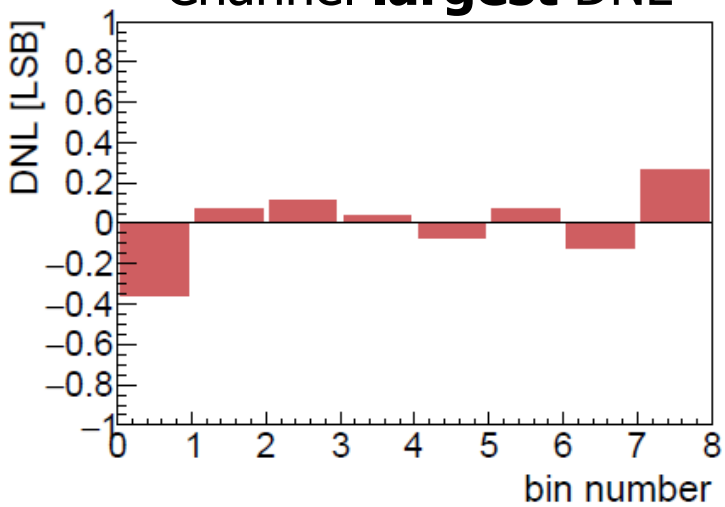
Systematics from fixed latency link:

System initializations	16.4 ps peak-to-peak
Long-term stability	10.5 ps RMS
Temperature stability	0.21 ps/℃

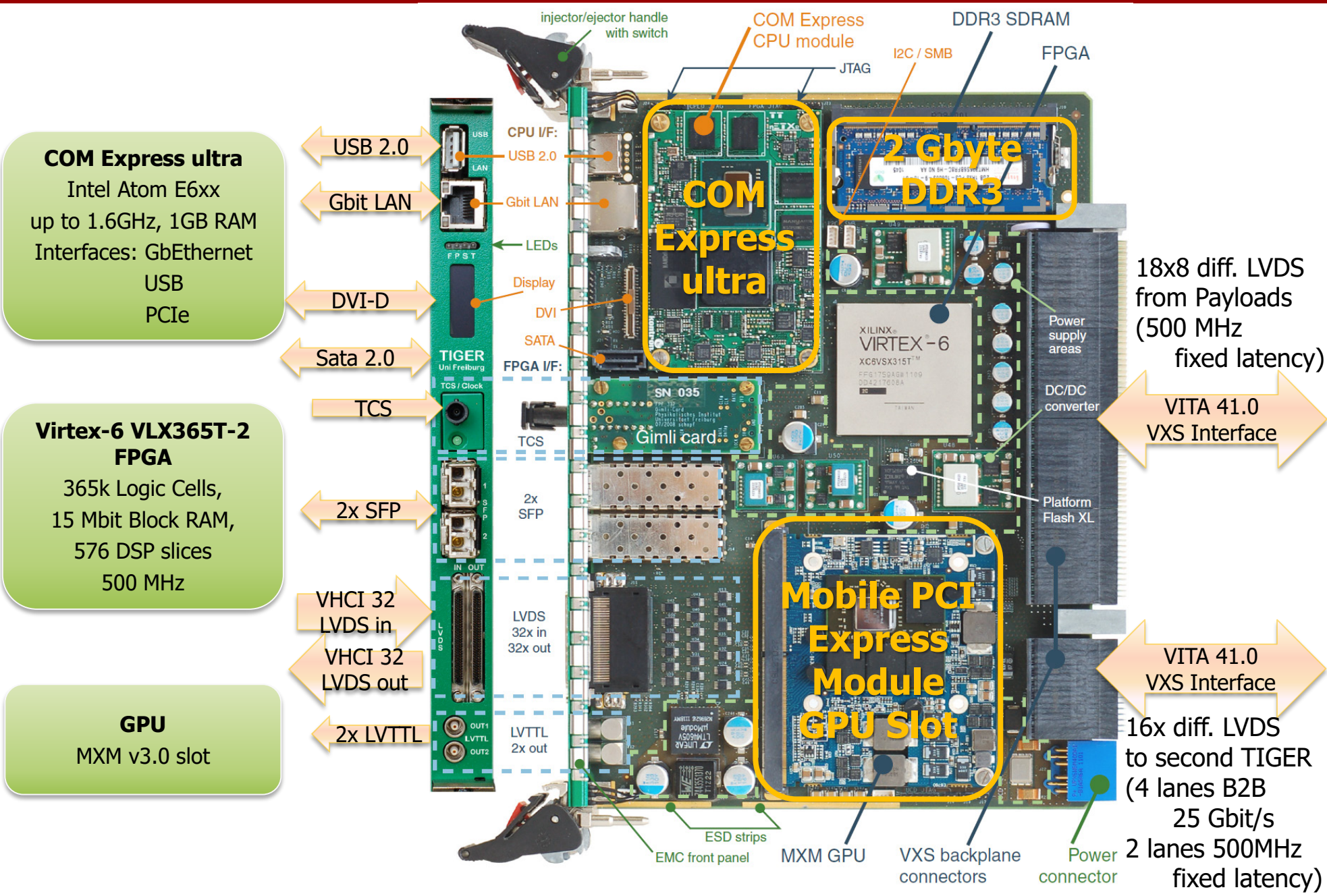
Channel **smallest** DNL



Channel **largest** DNL



TIGER – (Trigger Implementation for GANDALF Electronics Readout)

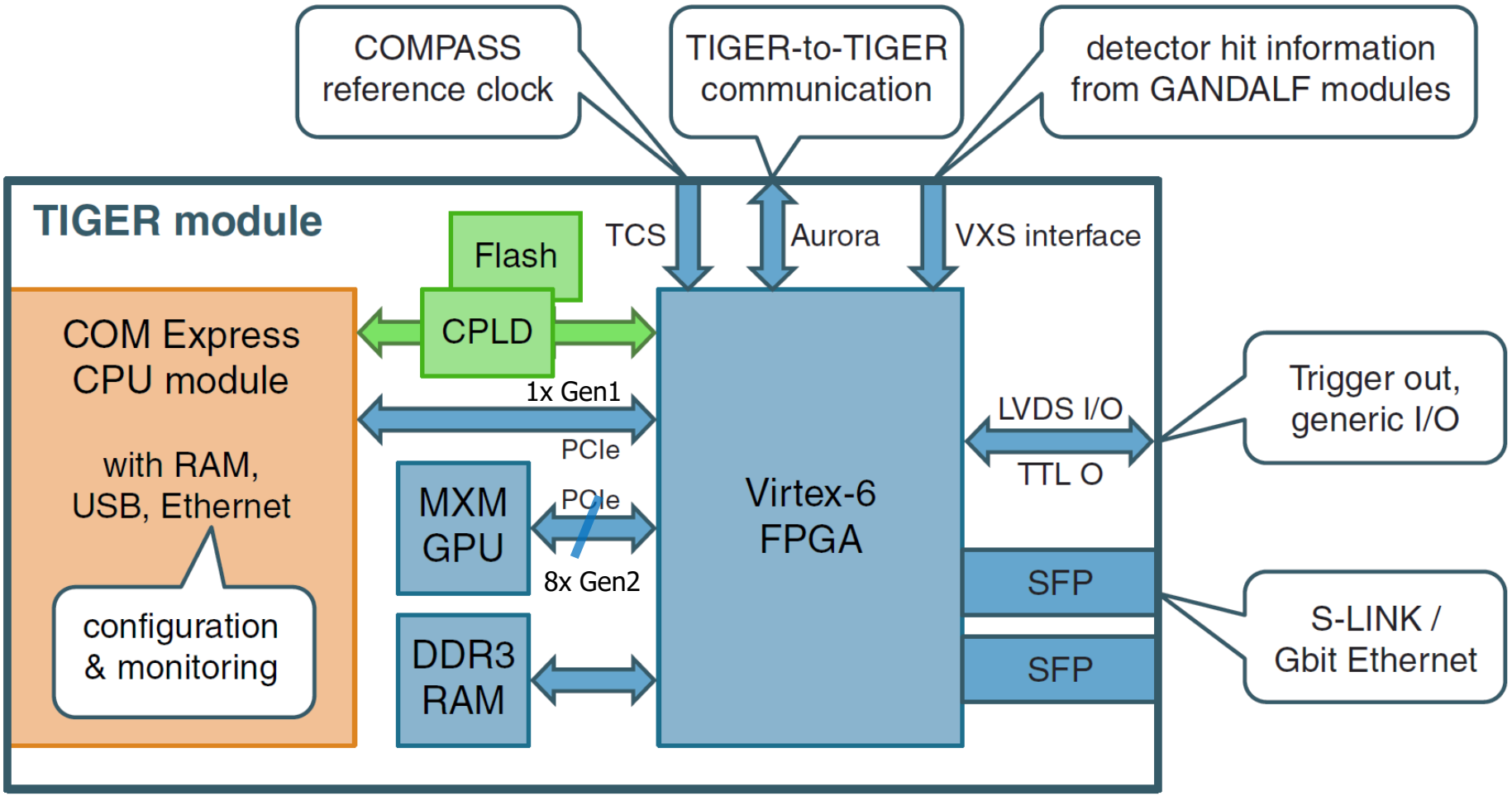


COM Express ultra
Intel Atom E6xx
up to 1.6GHz, 1GB RAM
Interfaces: GbEthernet
USB
PCIe

Virtex-6 VLX365T-2 FPGA
365k Logic Cells,
15 Mbit Block RAM,
576 DSP slices
500 MHz

GPU
MXM v3.0 slot

TIGER: Simplified Diagram



- TIGER has no connection to VME bus
- Communication to outside World by Ethernet only

GPU and CPU Modules

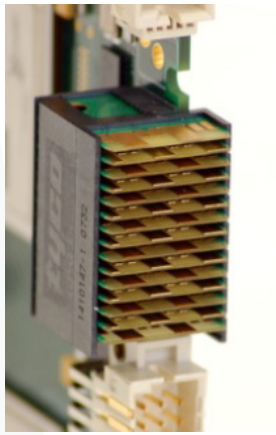
kontron

- AMD HD6770M
- nVidia GTS 250M

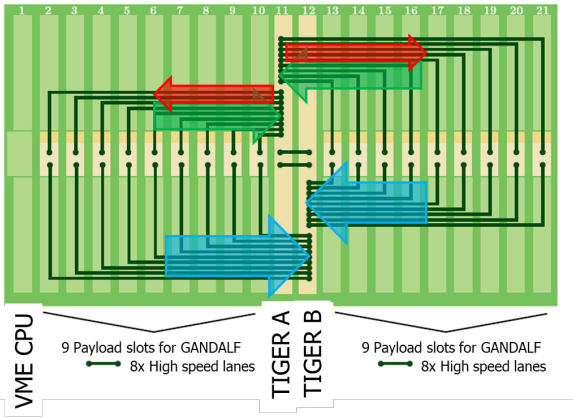
Kontron nanoETXexpress-TT:
COMe-mTTi10 E680T

- size: 55mm x 84 mm
- 1GB DDR2 memory
- 4GB onboard SSD
- 4x PCI Express x1 Lanes
- 10/100/1000 Mbit LAN

TIGER in COMPASS II



Backplane:



GANDALF (up to18 Modules)

Vita 41.1 VXS Backplane

18*8 fixed latency (time stamps, Amplitudes)

18x S-Link

18x Trigger & Clock (TCS)

TIGER 1 Trigger Processor (Trigger Generator)

TIGER 2 Readout Concentrator

TCS

USER defined

Trigger

Experiment Trigger

Trigger & Clock via TCS to Frontends

1x /2x Serial Readout Link (presently HOLA or ODIN S-Link to ROB)

DAQ

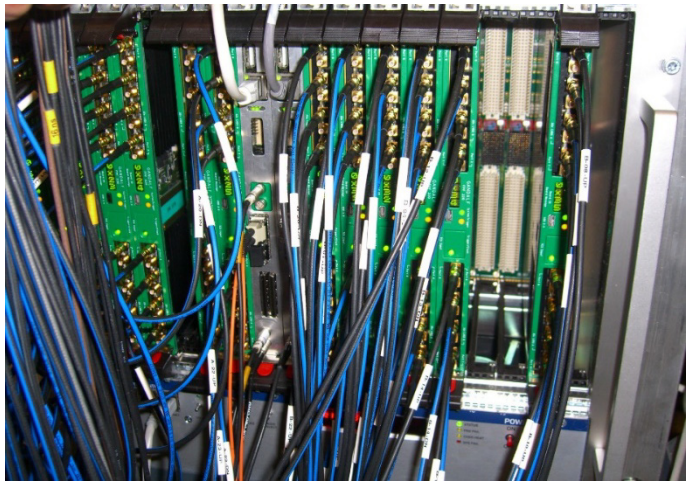
Concluding Remarks

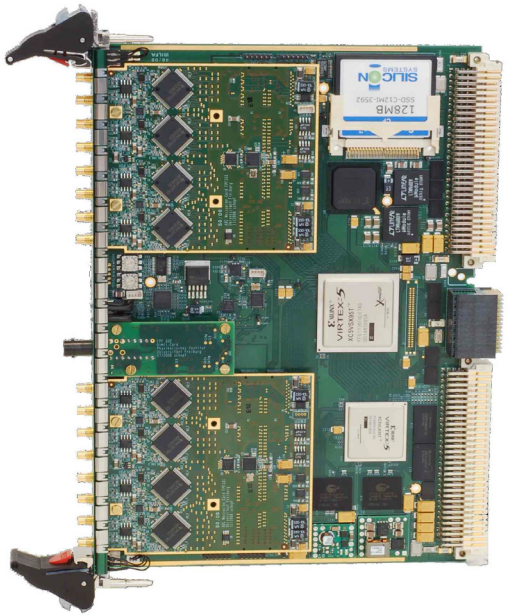
Presently …

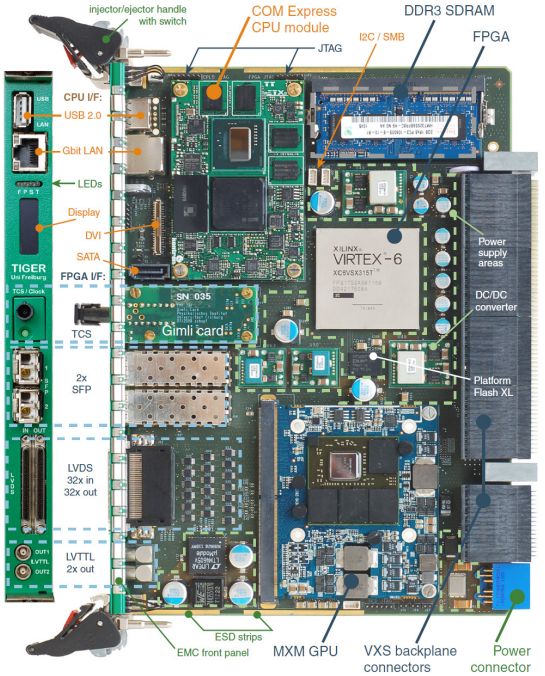
… COMPASS related hardware projects completed,

… we are eager to start something new …

… either new TDC based on PicoTDC
or firmware contribution to digital trigger







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