COMPASS++ Trigger-Less DAQ

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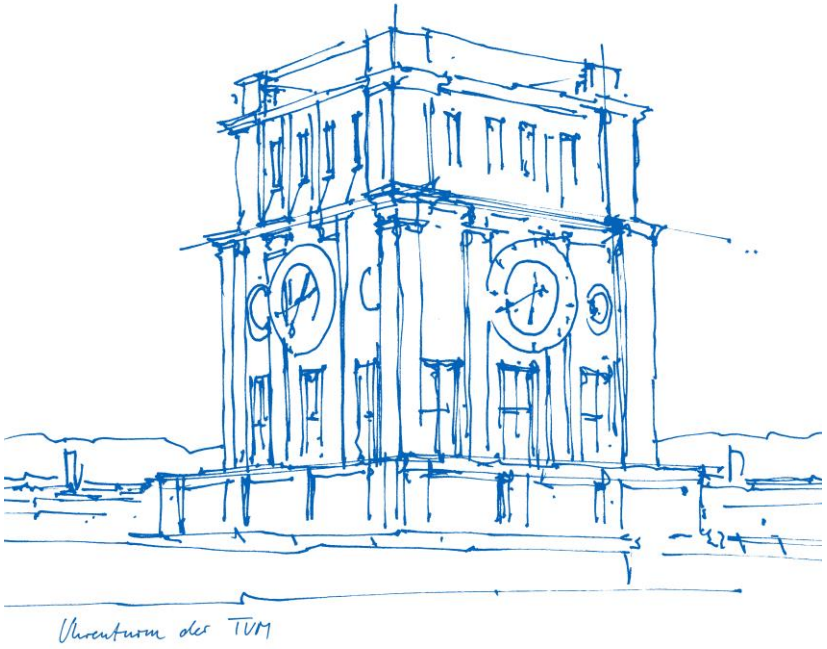


Limits of FEE

F1 TDC Limitations

- Trigger latency - 2us
- Trigger rate 40-50kHz
- No further improvements possible

Plan : substitution of F1

APV25 : Silicon, Gem, PGEM, PMM, RICH

- Trigger latency 4 us
- Trigger rate 40kHz by interface bandwidth, absolute maximum 90kHz

Plan : new front-end electronics based on SAMPA or/and VMM ASICs

Limits of Current System : SADC and MSADC

HCAL1, HCAL2, ECAL1 – SADC 10bit 80MSPS

- Highly inefficient zero suppression algorithm
- One channel provides 32 samples or 44 bytes of data
- Trigger latency 5us
- 100 kHz @10% occupancy

ECAL0, ECAL2 – MSADC 12bit 80MSPS

- One channel provides 32 samples or 68 bytes of data
- Trigger latency 5 us
- Maximum trigger rate limited by interface bandwidth of 20MB/s/64 channels
- 45 kHz @10% occupancy

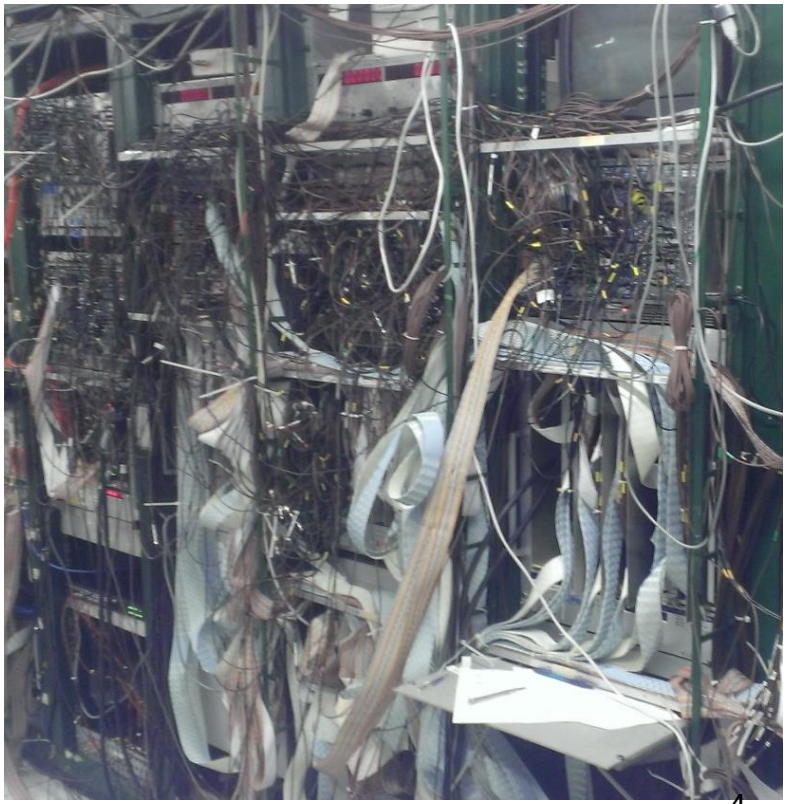
To be done :

- **Implement feature extraction algorithm and transmit Amplitude and Time => 4 Bytes/channel**
- **Waveform compression**
- **Develop new carrier card to convert MSADC system to trigger less capable**

Trigger Logic

NIM logical modules

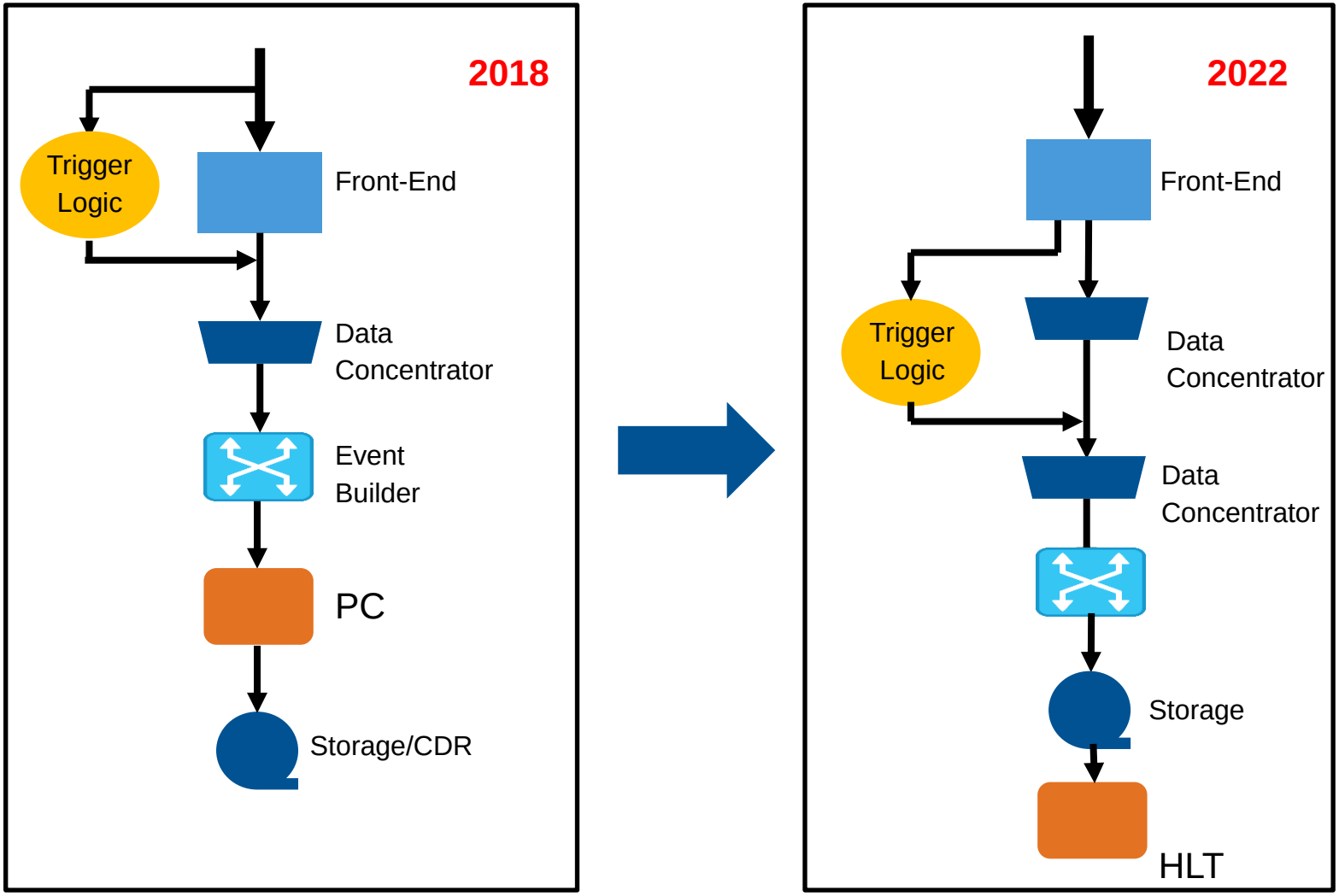
- Programmable, analogue coincidence matrix for target pointing trigger
- Simple trigger functions
- Limited programmable features
- Limited debugging capabilities



Plan :

- Develop FPGA based trigger processor
  - Programmable latency
  - Programmable logic
  - Built-in monitoring

Evolution of COMPASS DAQ Architecture



PRM Data Rate

Beam rate	#planes	5 10^7 /s
Silicon	8+8	13 GB/s
SciFi	8+4	10 GB/s
TPC	66 ch@10MSPS	2 GB/s
Sustained		7 GB/s

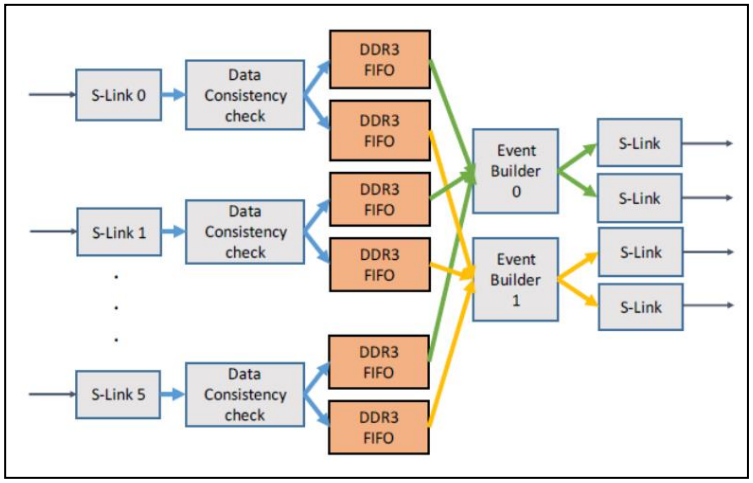
DY Data Rate Projected to TL ReadOut

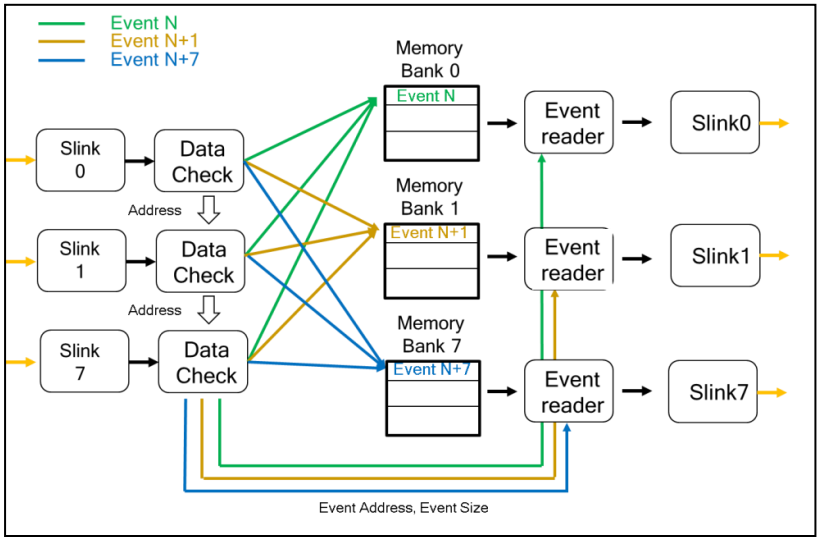
Detector	Gate	DY 2018	
		RND	Phy.
MWPC	250 ns	0.8 GB/s	2.4 GB/s
DC1-4	320 ns	3.2 GB/s	6.8 GB/s
SciFi	90 ns	6.6 GB/s	11 GB/s
W45	640 ns	0.5 GB/s	0.8 GB/s
Straw	200 ns	1.2 GB/s	2.5 GB/s
PMM	300 ns	5.5 GB/s	14.6 GB/s
RW	250 ns	0.7 GB/s	1.5 GB/s
RICH	120 ns	1 GB/s	1.5 GB/s
MW1,2	250 ns/900 ns	0.3 GB/s	0.5 GB/s
GEM	300 ns	6.6 GB/s	10 GB/s
CEDAR	80 ns	3.2 GB/s	5 GB/s
Rate within spill		29.6 GB/s	56.6 GB/s
Averaged rate		10 GB/s	19 GB/s

iFDAQ Limits

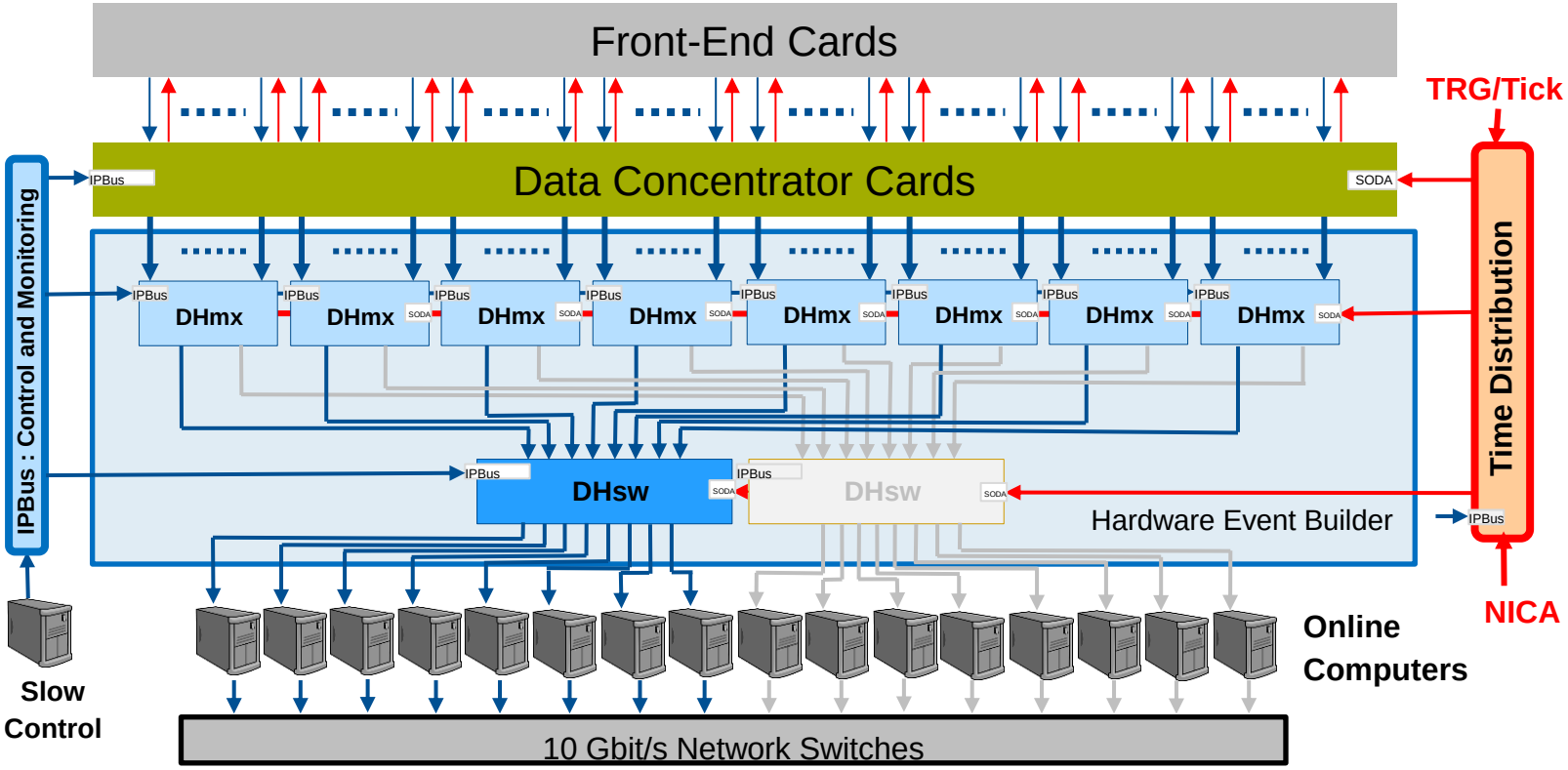
DAQ performance is limited by Switch bandwidth:

- current firmware bandwidth 400 MB/s
- new firmware architecture 2.5 GB/s
- expected performance with new FPGA card 10GB/s





iFDAQ Architecture



Data Flow in Trigger-less DAQ

Data divided to time slices

How big slice has to be ?

- Detector time resolution
- Event size

If event occurs on a border between two slices?

1. Long time slices of 1 ms
   - Ignore events on border between two slices
   - Copy data at boundaries to both slices
   - How to apply trigger?
2. Small time slices
   - Event is two consecutive time slices
   - TPC special case
3. Long time slices with sub-slices of different length according to detector time resolution
   - Event is collection of two consecutive sub-slices from each detector

New Developments

UCF (Unified Communication Framework)

- Universal protocol for all types of communications between FPGAs
- Single link for trigger, slow control(IPBUS) and data
- Supports different topologies : point-to-point and start like

FPGA TDC - iFTDC

Digital Trigger Processor

- Process TDC information instead of analogue information
- Provision of AND, OR , VETO processor units
- Build entire trigger logic out of these units within FPGA

Feature extraction algorithm for calorimeters

- Develop FIR filter to extract TIME and AMPLITUDE down to SNR = 4

Develop trigger less FEEs and DAQ for future COMPASS like experiment

PRM Work Packages

Hardware

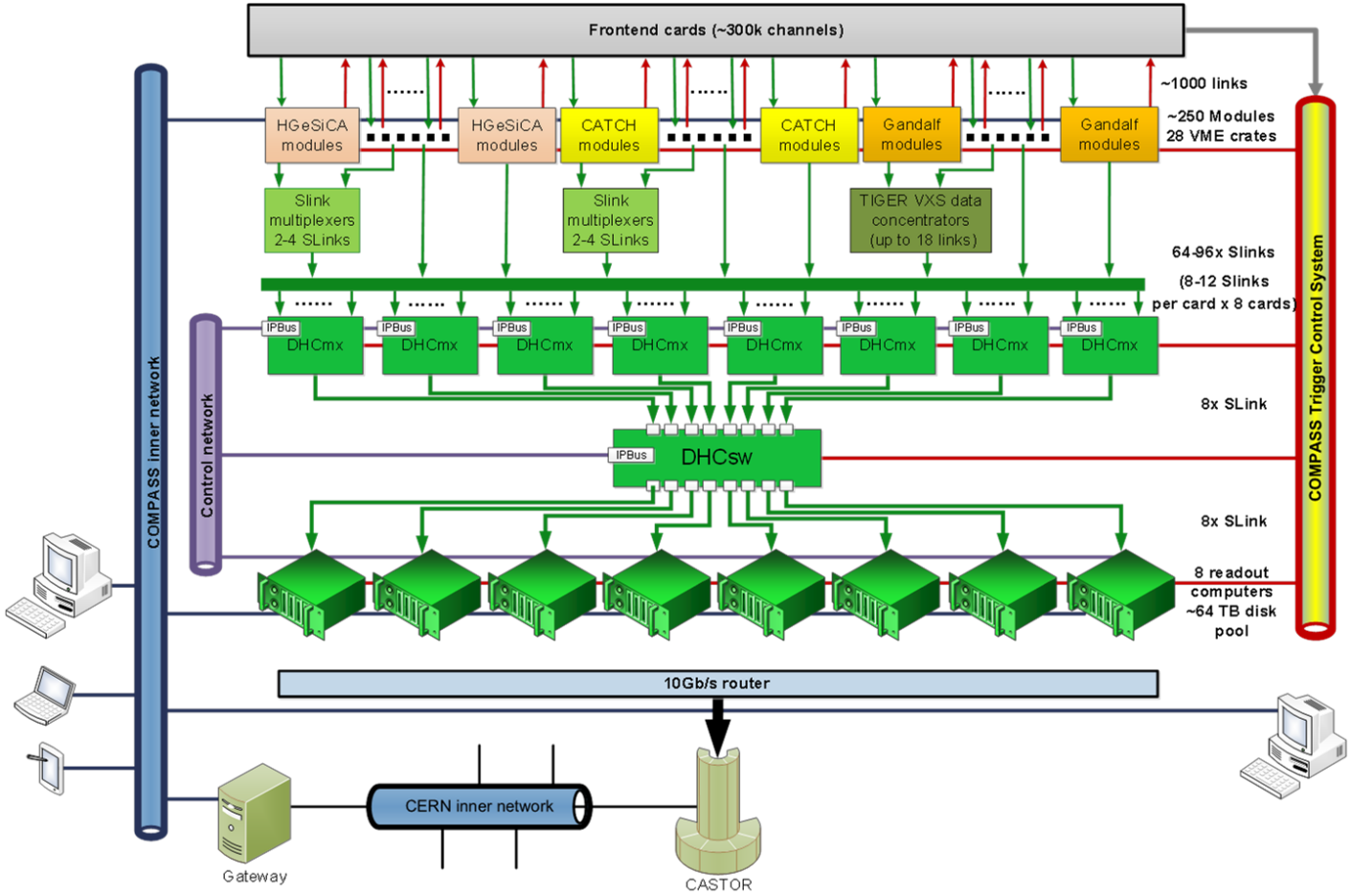
- New FPGA Card
- iFTDC
- Silcion read out
- Trigger processor
- High speed interface to PC : PCIe or Ethernet
- Trigger-less MSADC read out (?)

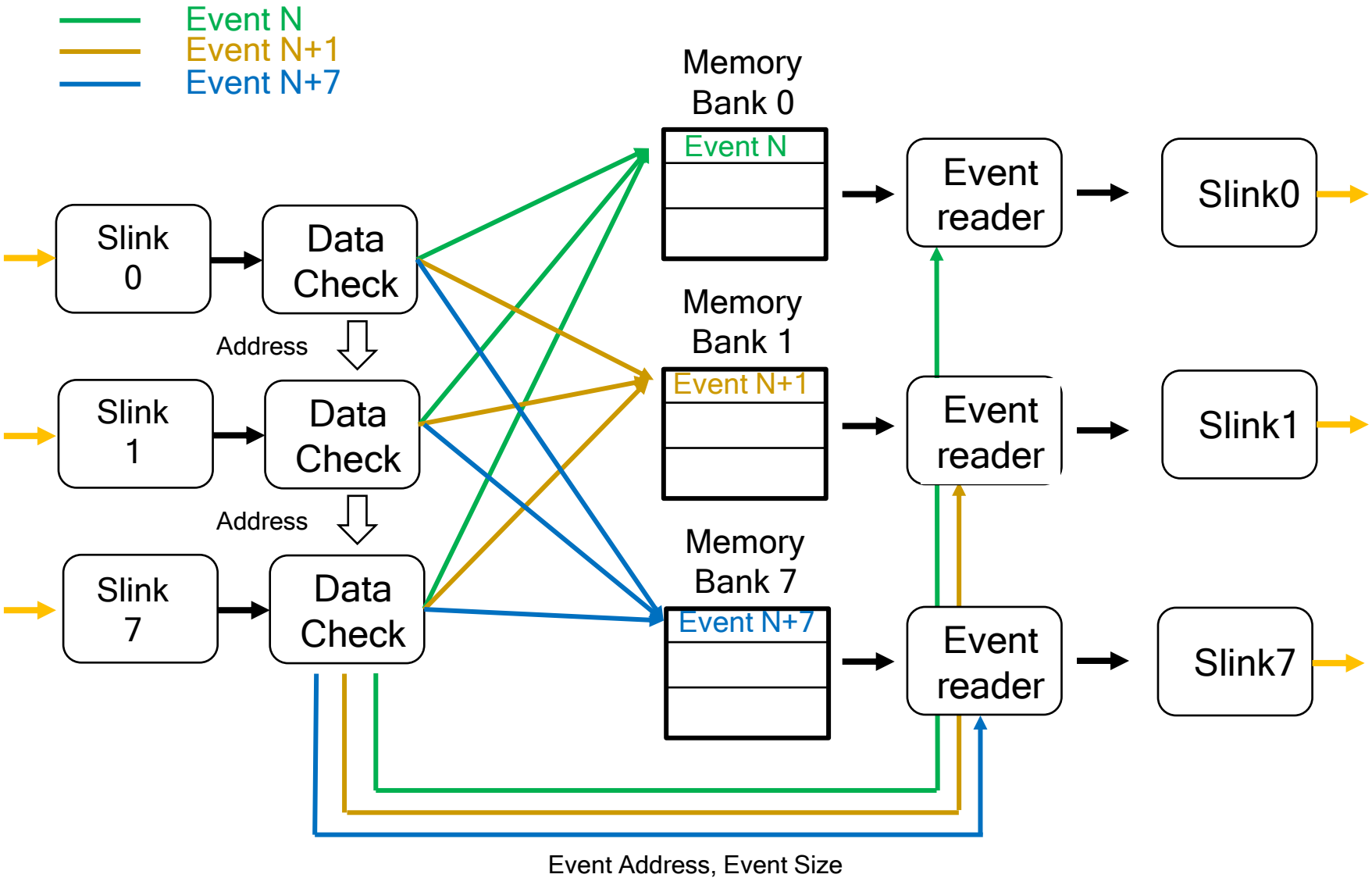
Software

- High performance read out process – 1GB/s/PC
- Support of two level trigger scheme
- Offline software

THANK YOU

iFDAQ Limits




Event N
Event N+1
Event N+7
Memory
Bank 0
Event N
Memory
Bank 1
Event N+1
Memory
Bank 7
Event N+7
Slink
0
Slink
1
Slink
7
Data
Check
Data
Check
Data
Check
Address
Address
Event
reader
Event
reader
Event
reader
Slink0
Slink1
Slink7
Event Address, Event Size

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