The CMS
High Granularity
Calorimeter Upgrade

Vito Palladino on behalf of the CMS Collaboration
CepC 15-17 April 2019
Overview

- HL-LHC step-up in instantaneous luminosity: from $\sim 2 \times 10^{34}$ to $5-7 \times 10^{34}$ cm$^{-2}$ s$^{-1}$
- Average pileup (PU) increases from $\sim 50$ up to 200 interactions per bunch crossing.
- Integrated radiation dose over the lifespan of some detectors increases by one order of magnitude.
- New design and/or electronics for sub-detectors needed to meet the new maximum L1 trigger rate (from 100 to 750 kHz) and latency (from 4 to 12.5 μs).
HGCAL Design

- The radiation dose in the current endcap calorimeters will exceed the design limit.
- The increase in PU will stress the background rejection performance.
- The solution to those issues has been chosen to be the new High Granular Calorimeter.

Fluence $10^{16}$ n$_{eq}$ cm$^{-2}$

Radiation Dose $10^6$ Gy
HGCAL Design

- Radiation tolerance:
  - Si-only planes in the high radiation region,
  - Scint+SiPM in the low radiation region ➔
    hybrid planes in downstream half of HGCAL,
  - Active cooling at -30 °C (~100kW/endcap).
- Lateral shower confinement: dense calorimeter (CuW+Cu+Pb absorber).
- Adjacent shower separation: fine lateral granularity (two cell sizes 0.52 and 1.18 cm²).
- PU rejection, PID and energy resolution: fine longitudinal granularity (52 layers).
- PU energy rejection: good time resolution (25 ps).
HGCAL Design

- Calorimeter Endcap Electromagnetic (CE-E):
  - 28 layers (Si-only)
  - CuW+Cu+Pb absorber
  - $25.4 \times \lambda_0$
  - $1.5 \lambda_0$

- Calorimeter Endcap Hadronic (CE-H):
  - 24 layers (Si-only + Si-Scint)
  - Stainless Steel absorber
  - $8.9 \lambda_0$
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Silicon Modules

- Basic hexagonal blocks from 8” diameter silicon wafers.
- Sensor’s thickness and active cell size are $\eta$ dependent: radiation damage minimization, better shower separation in the high occupancy region.

PCB (hexaboard)
Sensor
Kapton-Au bias plane
Baseplate ($^{\text{Cu/W}}_{\text{PCB}}$ for CE-E, $^{\text{Cu}}_{\text{PCB}}$ for CE-H)

192 cells 1.18 cm$^2$
432 cells 0.52 cm$^2$

Colored regions: coarse granularity for trigger purposes.
Silicon Modules

- Preparation for full scale production undergoing at the Module Assembly Centres:
  - China (Beijing IHEP),
  - India (Mumbai BARC),
  - Taiwan (Chungli NCU/Taipei NTU),
  - USA (Carnegie-Mellon, Texas Tech., UCSB).
  - ~100 modules produced for test beam purposes.

- Sensors wire bonded to PCB through large holes.

- Thermo-mechanical studies are performed in order to ensure robustness during repeated thermal cycles (-30 to +40 °C).
Scintillator Modules

- Plastic scintillator tiles arranged in r-\(\phi\) grid.
- Tile surface varies from 4 to 32 cm\(^2\) (from small to large \(r\)).
- Readout is performed by on-tile SiPM.
- Tiles grouped in tileboards with max dimension of 45\(\times\)41 cm\(^2\).
- Tile Assembly Centres:
  - US (FNAL)
  - Germany (DESY)
On-detector Electronics

- Bunch Crossing synchronous data from hexaboards are sent to concentrator ASICs, mounted on ‘motherboard’ PCB, through up to 36 e-links at 1.28 Gbps.
- ECON-T will select trigger data before transmitting to the Back-End.
- ECON-D will send zero suppressed fine granularity data to DAQ.
- DAQ path sent via lpGBT link at 10.24 Gpbs.
- lpGBT, VTRX+ and SCA are common developments.
Motherboard

- Motherboards will host the ECONs and the transceivers to the off-detector electronics.
- Bandwidth to off-detector electronics is highly cost constrained.
- Up to 4×10 Gbps links to the off-detector electronics:
  - 1 for DAQ
  - Up to 3 for Trigger
- Geometry needs optimization to minimise link count.

Average Bandwidth for data and trigger (in Gbs)
Front End Electronics: HGCROC ASIC

- Two different input stages for Si and Scint.
- Final version of the final HGROC chip expected in early-2021.
- High dynamic range: from 0.2 fC to 10 pC.
- 10-bit ADC + ToT (12-bit TDC).
- ToA:
  - Available for deposits above 10-15 fC,
  - 10-bit TDC, step < 25ps range up to 25 ns,
  - Precision for hit ≤100 ps, and ~30 ps for showers.
- Low power: ≤ 15 mW/channel.
- High radiation environment: up to 2 MGy and a fluence of $10^{16}$.
- Technology: CMOS 130 nm.
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Cassettes

- Detector is divided in 60° sectors.
- **CE-E:**
  - Silicon only cassettes.
  - Absorber included in the cassette.
  - Double sided around the cooling plate.
- **CE-H:**
  - Silicon only planes have similar design as CE-E cassette, differences: single sided, absorber not included, build out of 2×30° sectors.
  - From layer 9 hybrid Si+Scint cassette.
Cooling

- To reduce silicon radiation damage silicon temperature -30°C with 1-3°C gradient.
- Electronics power dissipation main source of heat in the cold volume (~70%), total ~100kW/endcap.
- Scheme based on the AMS cooling system, also adopted by LHCb and current CMS pixel.
- Coolant choice: CO₂
  - Low viscosity ➔ small pipes.
  - High radiation tolerance.
  - Environmentally friendly.
- Baseline:
  - Dual phase CO₂ close-loop.
  - Cooling power 300kW for both endcaps.
  - Minimum design temperature -35°C.
  - Divided in 30° sectors.
Services

- Many different services are required:
  - CO2 cooling.
  - Low-voltage for the electronics.
  - Bias voltages for silicon detectors and SiPM.
  - Optical fibres for data and trigger information.
  - Dry gas system.
  - Detector Control System (DCS).
  - Detector Safety System (DSS).
- Services routed under and adjacent to cooling distribution pipes (purple volume in the top drawing).
- Services exit the cold volume through feedthroughs placed on the back of the HGCAL endcaps.
Off-detector Trigger Electronics

- Two distinct stages based on ‘coarse’ information (trigger cells) from detector available (4 or 9 times the full granularity).
- Baseline:
  - Stage 1: builds and selects 2D clusters, implements Time Multiplex (TMUX),
  - Stage 2: generates the trigger primitives (TP) in forms of 3D clusters.
- ‘Direct 3D’ approach considered:
  - Stage 1: multiplexes data to Stage 2 and implements the TMUX,
  - Stage 2: builds TP using full depth information with no loss of raw information.
Generic ATCA Board: Serenity

- Generic motherboard common to several subsystems.
  - Exchangeable FPGAs on daughterboards: versatile.
  - DAQ and TPG will use different kind of FPGAs ➔ cost reduction and tailored resources.
  - Up to 72 in and 72 out links at 25 Gbps (Xilinx VU7P FPGA).
- Baseline firmware for TPG Stage 1 developed, needs to be ported on target FPGA.
  - Alternative TPG algorithms are under study.
- Clock distribution node: channel-to-channel RMS jitter has been measure to be 2.8 ps (input jitter 1.3 ps).
  - HGCAL clock distribution jitter requirement: <10 ps.
Test Beam

Test beam setup

Energy Resolution (Electromagnetic)

Energy Resolution (Hadronic)
Machine Learning for HGCAL

- In parallel to developing a more conventional reconstruction (structured to allow the possibility to run on GPUs), a machine learning approach is also being investigated.
- Exploiting lateral and longitudinal high granularity.
- Image processing approach.
- Wide spectrum of options:
  - Convolutional Neural Network (NN) for denoising
  - Graph NN Irregular geometry
  - Reconstruction
  - ...

Example of de-noising in HGCAL.
Conclusions

- Physics simulation is teaching us how to exploit the full capability of the High Granularity Calorimeter.

- The HGCAL project is moving fast towards the start of production in 2021.
- Many design choices have been frozen but many more need optimization.
- EDR foreseen for Q1 2021.
Backup
The HGCAL Roadmap

- HGCAL adopted by CMS in 2015.
- First prototype modules produced and tested in 2016.
- Mass construction due to start ~2021.
- Installation foreseen during LS3 (2024-2025), for operation in Run4 (starting in 2026).
Dummy Cassette for Cooling tests

Dummy cassette for heat exchange at FNAL.

- Stainless-steel clad Pb absorber 2.1mm Stainless-steel clad
- PCB motherboard
- ASICs etc. PCB sensor board
- Silicon CuW baseplate
- Cu cooling plate

- Inlet temp -24C, outlet temp -27C
- Pressure difference 1bar
- Cooling plate -24C, ambient -9C
Sensor Thickness

Sensor thickness tuned on the expected neutron fluence after 3 ab⁻¹
Luminosity at CMS

CMS Peak Luminosity Per Day, pp, 2018, $\sqrt{s} = 13$ TeV

Data included from 2018-04-17 10:54 to 2018-10-26 08:23 UTC

Max. inst. lumi.: 21.40 Hz/nb

CMS Preliminary
Time Based PU Discrimination

Before Time cut

After Time cut $\Delta t < 90$ ps

VBF event ($H \rightarrow \gamma\gamma$) with one photon and one jet in the same quadrant.

- Reminder: ToA available only for a deposited charge of $\sim 12$ fC.
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Cassette
Test Beam 2018

Configurations:

- **Config1:**
  - 28 layers in EE + 9×7 + 3×1 in FH

- **Config2:**
  - 28 layers in EE + 2×1 + 9×7 in FH

- **Config3:**
  - 8 layers in EE + 12×7 in FH
dowlink @ 2.56 Gb/s
uplink @ 10.24 Gb/s

dowlink @ 2.56 Gb/s
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CLK & Fast Timing
I2C, temp, etc.

CLK, Fast Timing, I2C

HGCROCs