Test and Design for Testability of Analog and Mixed-Signal Circuits

ACEOLE - PH-ESE Electronics Seminars
4-5 February 2010

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Test is critical

- Semiconductor industry is extremely competitive and is asking for the best quality and reliability levels at the lowest cost.
- Nanoscale devices in combination with gigascale complexity
- Increasing complexity (e.g., more than 100 microcontrollers in one car)
- Test is becoming a dominant factor in overall manufacturing cost.
- Long product life times, typically from 10 to 25 years (!), which require zero reliability defect
Test is critical

- Harsh and/or variable environment (e.g., in a car or in a human body)
- Heterogeneous systems (MEMS, RF, digital, etc.) in miniaturized packages
- Mandatory secure communication links (data integrity, protection against attacks)
- Complex diagnosis and very high costs or risks of maintenance/repair (e.g. implanted devices)
- Test is the last chance to deliver quality and reliability to the end customer!
Outline

• Basic concepts on testing and design for testability
• Defect, fault modeling and test metrics
• Design for testability and built-in self-test
  – structural and functional test
• Standard test infrastructures
• Digital signal processing based testing
Basic concepts on Testing and Design for Testability

• “Our reason for living”

- Bad design or specifications
- Manufacturing errors
- External disturbance
- Bad materials or components

  Software defects

  Hardware defects

  Faults
Basic concepts on Testing and Design for Testability

Product life-cycle (value chain)

The test of an IC can occur in different stages:

- at the wafer level 
  \textit{(probing the wafer)}
- after packaging 
- after insertion in a board 
- as part of a system 
- as part of a system operating in the field

Specifications: functional, structural, technological process, manufacturing characterization

- Design
- Prototyping
- First production
- Manufacturing
- Production test
- Client
- Operation

Prototype characterization test
Evaluation of the manufacturing process
Intermediate test
Final production test
Reception test
Maintenance test
### Basic concepts on Testing and Design for Testability

#### Types of test

<table>
<thead>
<tr>
<th>Type of Test</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Production: Wafer Sort /Probe Final / Package</td>
<td>Tests of manufactured parts to sort out those that are faulty; Test of each die on the wafer; Test of packaged chips and separation into bins (military, commercial, industrial)</td>
</tr>
<tr>
<td>Design verification</td>
<td>Verification of design correctness</td>
</tr>
<tr>
<td>Characterization or Engineering</td>
<td>Determine actual values of devices' Ac and Dc parameters and interaction of parameters: Set final specifications and identification of possible process yield improvement.</td>
</tr>
<tr>
<td>Quality / Sample</td>
<td>Test a sample of each lot of manufactured parts.</td>
</tr>
<tr>
<td>Go / No Go</td>
<td>Determine whether devices meet specifications</td>
</tr>
<tr>
<td>Stress Screening (ESS/Burn-in)</td>
<td>Test under high temperature, temperature cycling, vibration, .., to eliminate short life parts</td>
</tr>
<tr>
<td>Reliability (Accelerated life)</td>
<td>Estimate time to failure in normal operation after operation under high temperature</td>
</tr>
<tr>
<td>Diagnostic / Repair</td>
<td>Identify failures and locate defects</td>
</tr>
<tr>
<td>Acceptance</td>
<td>Demonstrate / verify degree of compliance with specified requirements</td>
</tr>
<tr>
<td>On-line / checking</td>
<td>Verification of operation correctness during normal operation</td>
</tr>
</tbody>
</table>
Basic concepts on Testing and Design for Testability

Test Complexity

Test development and application time may become prohibitive
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New packaging types

- BGA (Ball Grid Array)
  - Small solder balls to connect to board
  - Small
  - High pin count
  - Cheap
  - Low inductance
- CSP (Chip scale Packaging)
  - Similar to BGA
  - Very small packages

Package inductance:
1 - 5 nH
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- “AMS circuits account for 70% of SOC-test cost and 45% of test-development time, even though they make up a small fraction of the chip complexity,”
  Karim Arabi, Qualcomm

- Test pattern generation can account for 40% of an ASIC design time
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• Testing – process of screening/detecting defective parts (in a manufacturing line)

Production Yield ($Y$): $Y = \frac{N_{\text{PassedDevices}}}{\#\text{TotalDevices}} \times 100\%$

Defect Level (DL): $\frac{\text{Faulty devices}}{\text{Total}} \times 100\%$

Failed devices

Rejected devices
(Defective devices + actually good devices)
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**Yield** — production efficiency: measures the percentage of good components in the overall production volume – a statistical parameter.

\[ Y = e^{-DD.SA} \]

\[ N_{PassedDies} = N_{Dies/Wafer} \cdot N_{Wafers/Lot} \cdot Y \]

\[ N_{FailedDies} = N_{Dies/Wafer} \cdot N_{Wafers/Lot} \cdot (1-Y) \]
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Production yield \( Y = e^{-Area \cdot DefectDensity} \)

Typical defect density \( \sim 0.005 - 0.02 \) defects/mm\(^2\)

- Low production volume technology: \( D = 0.02 \)
- Very high production volume technology: \( D = 0.005 \)
- Typical ASIC technology: \( D = 0.01 \)

Price of 100 mm\(^2\) chip compared to 50 mm\(^2\) chip:
- \( 100 \text{ mm}^2 / 50 \text{ mm}^2 \times 0.61 / 0.37 = 3.4 \) (\( D = 0.01 \))
- \( 100 \text{ mm}^2 / 50 \text{ mm}^2 \times 0.36 / 0.14 = 5.3 \) (\( D = 0.02 \))
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Testing time

\[
T_{\text{test\_chip}} = \frac{T_{\text{setup}} + T_{\text{wafer\_loading}} \times NWL + T_{\text{die\_stepping}} \times NDW \times NWL + T_{\text{pass}} \times NPD + T_{\text{fail}} \times NFD}{NDW \times NWL}
\]

Cost\_test = \(T_{\text{test\_chip}} \times \text{Test\_Cost\_Rate}\)

\[
\text{Test\_Cost\_Rate} = \left( D_{\text{Tester}} + D_{\text{Handler}} + C_{\text{Fixed}} \right) \left( \frac{T_{\text{test\_allchips}} + T_{\text{Handler}}}{T_{\text{test\_allchips}}} \right) \left( \frac{T_{\text{Tester\_Used}} + T_{\text{Down}} + T_{\text{Idle}}}{T_{\text{Tester\_Used}}} \right)
\]

Throughput = \(\frac{N_{\text{good\_devices}}}{T_{\text{Total}}}\)
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Classes of IC Electrical Tests

• Functional
  – Detection of failures by verification of correct operation rather than by verifying the absence of specific faults
  – Verification that circuits operate correctly and meet specifications (design verification)

• Structural (DC parametric tests) – test for the occurrence of faulty behaviours; interconnections; presence of protection circuits

• AC, parametric tests
  – Measure of time parameters, leakage currents, power consumption
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Test Cost

NRE Costs
- DfT design and validation cost
- Test generation cost

Device costs
- Die area
- Yield loss

Capital equipment
Depreciation of:
- Test equipment cost
- Handler/Prober

Equipment cost
Room costs
- Staff
- Consumables
- Test jig …

Untested devices → Testing operations → Shipment to market → Rejected devices

€ Yield loss

Cost of returned parts

Goal: optimum product cost

Test TWG – 2007 ITRS December Conference – Makuhari, Japan
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• Costs
  – $C_{dftde}$: DfT design effort
  – $C_{dftt}$: DfT tools
  – $C_{atpg}$: ATPG development
  – $C_{ap}$: Test application
  – $C_{esc}$: Test escapes
  – $C_{ohd}$: Silicon overhead
  – $C_{pr}$: Performance loss
  – $C_{yl}$: Yield loss

• Benefits
  – $C_{tm}$: Time to market
  – $C_{va}$: Verification ability
  – $C_{ned}$-$C_{ed}$: Test escape diagnosis
Basic concepts
on Testing and Design for Testability

\[ \text{ROI} = \frac{\text{Benefit}}{\text{Cost} + C_{esc}} \]

\[ \text{Benefit} = \frac{C_t}{N_{gd}} + \frac{C_{va}}{N_{gd}} + (C_{ned} - C_{ed}) \]

\[ \text{Cost} = \frac{C_{atpg}}{N_{gd}} + C_{ap} + C_{esc} + C_{ohd} + C_{pl} + \frac{C_{yl}}{N_{gd}} \]

\[ C_{esc} = C_{bd} + C_{sd} + C_{fs} \]

\[ C_{bd} = K_{loop} \times T_{bd} \times C_{labor} \times N_{icb} \times P_{bd} \]

\[ C_{sd} = T_{sys} \times C_{labor} \times N_{sys} \times P_{sys} \]

\[ C_{fs} = \left( T_{fs} \times C_{labor} + C_{spare} + C_{travel} + C_{downtime} \right) \times N_{sys} \times P_{fs} \]

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Aspects affecting test cost

- Changing technology/products
- Lack of structural tests
- High quality
- High fault coverage
- Shorter time-to-market
- Maintenance
- Need to leverage investment in product life cycle
- Test errors
- Less in-circuit; more functional
- Complex circuits
- Expensive ATE
- Longer test development

High test cost
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• Manufacturer A (MA)
  • 150000 boards/year; 28 $/ board
  • 800 components; 4000 solder joints / board
  • Board repair yield: 85%, up to 5 repair cycles; scrap rate: 0,0076%
  • Electrical defect rate: 250 defects per million (DPM); average 0,2 defects/board
  • Structural defect rate: 400 DPM; average 1,6 defects/board
### Basic concepts on Testing and Design for Testability

- **Current field return rate**: 0.02%
- **Field failures/returns cost**: $2
- **Retest cost**
- **Repair cost per defect**
- **Debug/diagnosis cost per defect**
- **Repair time per defect**
- **Diagnostics/verification time per defect**

<table>
<thead>
<tr>
<th></th>
<th>ICT</th>
<th>FT</th>
<th>ESS</th>
<th>System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Labor cost of Verification/Diagnosis [$/h]</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
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<tr>
<td>Repair labor cost [$]</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Diagnostics/verification time per defect [min]</td>
<td>5</td>
<td>10</td>
<td>60</td>
<td>120</td>
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<tr>
<td>Repair time per defect [min]</td>
<td>15</td>
<td>30</td>
<td>50</td>
<td>50</td>
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<tr>
<td>Debug/diagnosis cost per defect [$]</td>
<td>0.17</td>
<td>0.33</td>
<td>2</td>
<td>4</td>
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<tr>
<td>Repair cost per defect [$]</td>
<td>0.5</td>
<td>1</td>
<td>1.67</td>
<td>1.67</td>
</tr>
<tr>
<td>Retest cost [$]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Field failures/returns cost - $2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current field return rate - 0.02%</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
## Basic concepts on Testing and Design for Testability

<table>
<thead>
<tr>
<th>Test Coverage Assumptions</th>
<th>ICT 1</th>
<th>ICT 2</th>
<th>FT</th>
<th>ESS</th>
<th>System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test access [%]</td>
<td>95</td>
<td>95</td>
<td>50</td>
<td>70</td>
<td>80</td>
</tr>
<tr>
<td>Fault coverage structural [%]</td>
<td>80</td>
<td>85</td>
<td>60</td>
<td>90</td>
<td>60</td>
</tr>
<tr>
<td>Fault coverage electrical [%]</td>
<td>90</td>
<td>95</td>
<td>85</td>
<td>95</td>
<td>99</td>
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<tr>
<td>Test coverage [%]</td>
<td>78</td>
<td>82</td>
<td>32</td>
<td>64</td>
<td>53</td>
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<tr>
<td>False fail rate [ppm]</td>
<td>50</td>
<td>25</td>
<td>10</td>
<td>5</td>
<td>2</td>
</tr>
</tbody>
</table>
### Basic concepts on Testing and Design for Testability

#### Total test costs, ICT 1

<table>
<thead>
<tr>
<th></th>
<th>ICT 1</th>
<th>FT</th>
<th>ESS</th>
<th>System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structural defects before test [per board]</td>
<td>1,600</td>
<td>0,384</td>
<td>0,26880</td>
<td>0,09946</td>
</tr>
<tr>
<td>Structural defects after test [per board]</td>
<td>0,384</td>
<td>0,2688</td>
<td>0,09945</td>
<td>0,05172</td>
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<tr>
<td>Electrical defects before test [per board]</td>
<td>0,200</td>
<td>0,0290</td>
<td>0,01668</td>
<td>0,00559</td>
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<tr>
<td>Electrical defects after test [per board]</td>
<td>0,029</td>
<td>0,01668</td>
<td>0,00559</td>
<td>0,00116</td>
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<tr>
<td>Structural defects found [per board]</td>
<td>1,216</td>
<td>0,1152</td>
<td>0,16930</td>
<td>0,04770</td>
</tr>
<tr>
<td>Electrical defects found [per board]</td>
<td>0,171</td>
<td>0,0123</td>
<td>0,01110</td>
<td>0,00440</td>
</tr>
<tr>
<td>Total defects found [per board]</td>
<td>1,387</td>
<td>0,1275</td>
<td>0,18040</td>
<td>0,05220</td>
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<tr>
<td>First pass yield [%]</td>
<td>25</td>
<td>88</td>
<td>83,5</td>
<td>94,9</td>
</tr>
<tr>
<td>Overall test effectiveness [%]</td>
<td>77</td>
<td>31</td>
<td>63</td>
<td>50</td>
</tr>
<tr>
<td>DPM remaining on board after test</td>
<td>86</td>
<td>59,5</td>
<td>21,9</td>
<td>11</td>
</tr>
<tr>
<td>Annual verification costs [$]</td>
<td>34,675</td>
<td>6,376</td>
<td>54,13</td>
<td>31,298</td>
</tr>
<tr>
<td>Annual repair costs [$]</td>
<td>104,025</td>
<td>19,129</td>
<td>45,108</td>
<td>13,041</td>
</tr>
<tr>
<td>Annual scrap costs [$]</td>
<td>741</td>
<td>80</td>
<td>93</td>
<td>28</td>
</tr>
<tr>
<td>Annual retest cost [$]</td>
<td>56,263</td>
<td>17,959</td>
<td>49,527</td>
<td>15,248</td>
</tr>
<tr>
<td>Annual field failure/return costs [$]</td>
<td></td>
<td></td>
<td></td>
<td>6000</td>
</tr>
<tr>
<td><strong>Total [$]</strong></td>
<td>139,441</td>
<td>25,585</td>
<td>99,331</td>
<td>44,367</td>
</tr>
</tbody>
</table>

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Test and DfT of Analog and Mixed-Signal Circuits
Basic concepts on Testing and Design for Testability

<table>
<thead>
<tr>
<th>Total test costs, ICT 2</th>
<th>ICT 2</th>
<th>FT</th>
<th>ESS</th>
<th>System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structural defects before test [per board]</td>
<td>1,600</td>
<td>0,3090</td>
<td>0,21560</td>
<td>0,07980</td>
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<tr>
<td>Structural defects after test [per board]</td>
<td>0,308</td>
<td>0,2156</td>
<td>0,07980</td>
<td>0,04150</td>
</tr>
<tr>
<td>Electrical defects before test [per board]</td>
<td>0,200</td>
<td>0,0195</td>
<td>0,01120</td>
<td>0,00376</td>
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<tr>
<td>Electrical defects after test [per board]</td>
<td>0,020</td>
<td>0,01120</td>
<td>0,00376</td>
<td>0,00078</td>
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<tr>
<td>Structural defects found [per board]</td>
<td>1,292</td>
<td>0,0924</td>
<td>0,13580</td>
<td>0,03830</td>
</tr>
<tr>
<td>Electrical defects found [per board]</td>
<td>0,171</td>
<td>0,0123</td>
<td>0,01110</td>
<td>0,00440</td>
</tr>
<tr>
<td>Total defects found [per board]</td>
<td>1,473</td>
<td>0,1007</td>
<td>0,14330</td>
<td>0,04130</td>
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<tr>
<td>First pass yield [%]</td>
<td>22,9</td>
<td>90,4</td>
<td>86,7</td>
<td>96</td>
</tr>
<tr>
<td>Overall test effectiveness [%]</td>
<td>82</td>
<td>31</td>
<td>63</td>
<td>49</td>
</tr>
<tr>
<td>DPM remaining on board after test</td>
<td>68,2</td>
<td>47,3</td>
<td>17,4</td>
<td>8,8</td>
</tr>
<tr>
<td>Annual verification costs [$]</td>
<td>36.813</td>
<td>5.034</td>
<td>42.985</td>
<td>24.759</td>
</tr>
<tr>
<td>Annual repair costs [$]</td>
<td>110.438</td>
<td>15.103</td>
<td>35.821</td>
<td>10.316</td>
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<tr>
<td>Annual scrap costs [$]</td>
<td>726</td>
<td>68</td>
<td>76</td>
<td>23</td>
</tr>
<tr>
<td>Annual retest cost [$]</td>
<td>57.799</td>
<td>14.368</td>
<td>40.048</td>
<td>12.128</td>
</tr>
<tr>
<td>Annual field failure/return costs [$]</td>
<td>4.795</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total [$]</td>
<td>147.976</td>
<td>20.205</td>
<td>78.883</td>
<td>35.099</td>
</tr>
</tbody>
</table>

Savings $42,423

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Basic concepts on Testing and Design for Testability

The 1:10:100 Rule:

- The cost to fix a defect increases exponentially the later in the development lifecycle that it is identified.
- A defect caught in requirements phase costs a factor of 1 (1x) to fix.
- A defect caught in construction costs 10 times as much as in requirements.
- A defect caught in production costs up to 100 times as much as in requirements.
Basic concepts on Testing and Design for Testability

- Test metrics

\[
D_{\text{efectLevel}} = \frac{\text{Pass}/\text{Ok}}{\text{Pass}/\text{Ok} + \text{PassOk}}
\]

Prototype test
- Pass, Ok
- Pass,/OK
- Fail, OK
- Fail,/OK

Production test
- Pass, Ok
- Pass,/OK
- Fail, OK
- Fail,/OK

Reception test
- Pass, Ok
- Pass,/OK
- Fail, OK
- Fail,/OK

Diagnostics, fault analysis, repair

Client
Defect, fault modeling and test metrics

Typical defects

- Open circuits, high contact resistance and short-circuits in and among different layers
- Threshold voltage, transconductance, aspect ratio deviations
- Gate-oxide shorts, metallization failures or corrosion
- High leakage currents
- Defective bonding or packaging, geometry deviations
- Parasitic transistors
- Hot electrons, cosmic radiation, α particles
- Electromigration
Defect, fault modeling and test metrics

- Nvidia Corp 40 nm graphics processor has 3.2 billion transistors and 7200 million vias (> world population)
- via deposition is a major reliability concern.
- leakage power has "become almost intolerable“, “DC power has exceeded AC power for the first time;"
- the needs for zero defects and zero variability have become paramount.

John Chen, Nvidia Corp
Defect, fault modeling and test metrics

• **Electromigration**

Aggravated by:

– Reduction of the metallic interconnection width
– Reduction of contact area
– Higher current densities

![Diagram of interconnect](image)

**Conduction resistance**

- R
- R+10%
- R+20%

- T1
- T2
- T3
Defect, fault modeling and test metrics

In terms of duration defects can be:

- Permanent – their effect remains after the first occurrence
- Intermittent – their effect occur in intervals
- Transient – their occurrence is triggered by a particular event and whose effect is temporary (e.g., cross-talk)

Physical defects are not manageable with common simulation tools. That requires their representation with fault models.
Defect, fault modeling and test metrics

Fault model

- The translation of a defect into the electrical or logic level.
- A formal representation of the mode how the physical defect affects/changes a circuit’s behaviour in a certain level of abstraction.
- Knowing the physical mechanisms behind the occurrence of a defect, and how these manifest electrically is fundamental to develop realistic fault models. These are required for test stimuli generation and to evaluate tests quality.
Defect, fault modeling and test metrics

The same defect can be represented by different fault models according to the level of abstraction being used.

Attributes of a good fault model

- **Simplicity**, to allow efficient test vector generation and fault simulation procedures
- **Defect coverage**, to guarantee that the percentage of defective components escaping detection is acceptably low
Defect, fault modeling and test metrics

Reliability

- Failing parts within first 1000 hours: 1 - 5 %
- Burn-in testing: Heating up chips to 125 deg. accelerates 1000 hours period to approx. 24 hours.
  - Static: power supply connected
  - Dynamic: Power + stimulation patterns.
- Temperature cycling: continuous temperature cycling of chips to provoke temperature gradient induced faults. (Non matching thermal expansion coefficients).
- Electrical stress: Operation at elevated supply voltage
- \( I_{DDQ} \)

<table>
<thead>
<tr>
<th>Failure rate</th>
<th>Badly designed component (electron migration, hot electron, corrosion, etc.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Infant mortality</td>
<td></td>
</tr>
<tr>
<td>Time</td>
<td></td>
</tr>
<tr>
<td>1000 hours</td>
<td></td>
</tr>
<tr>
<td>10 years</td>
<td></td>
</tr>
</tbody>
</table>
Defect, fault modeling and test metrics

**I\textsubscript{DDQ} Test - Improved Process Control**

Set CMOS devices into static state and measure tiny current leaking from power to ground

- Certain defects are easily detected after the observation of the quiet current - $I_{\text{DDQ}}$.

- A resistive defect which may fail in the customers device
  - Excessive $I_{\text{DDQ}}$ signals the presence of leakage currents which are an indicator of process problems and reliability issues on medium/long term.

![Diagram](image-url)
Defect, fault modeling and test metrics

- $I_{\text{DDQ}}$ testing can only be performed if the device design is compatible, i.e. designed for test
- main requirements:
  - stable current at the moment of measurement
  - repeatable test conditions (substrate bias, temperature, VDD, …)

Shorter channel transistors exponentially contribute more to $I_{\text{DDQ}}$

An Effective Design-for-Idqq-Testing Approach for Embedded Cores Based System-on-Chip
John Sunwoo, Jonathan Harris
VLSI-TESTING, Spring/2004
José Machado da Silva
Test and DfT of Analog and Mixed-Signal Circuits
Defect, fault modeling and test metrics

Fault models

Catastrophic

Short-circuits

Opens

Fault models:

- Short-circuits (sc)
- Opens (oc)

Values:

- Short-circuits: 1 fF
- Opens: 1 GΩ

Source Drain

Gate

Open

Short

Test and DfT of Analog and Mixed-Signal Circuits
Defect, fault modeling and test metrics

• Gate Oxide Shorts
Defect, fault modeling and test metrics

Fault models

Parametric faults are simulated by affecting components’ parameters (passive and active) with deviations of their nominal values. E.g. ±5% to ±20% in the values of L, C, R and in the aspect ratio, VTO, KP, of MOS transistors.
Defect, fault modeling and test metrics

Defect Level

- The ultimate objective is to minimize the number of defective parts reaching the market.
  - Ideal value: 0 ppm
  - Typical: < 100ppm

\[ DL = 1 - Y^{(1-FC)} \]

- This equation provides an estimation of the defect level as a function of the production yield (Y) and testing fault coverage (FC). Faults are considered equiprobable.
Defect, fault modeling and test metrics

Inductive fault analysis
Considering non equally probable faults, 
 expresses a weighted measure of fault coverage.

Each fault weighted by a factor

which reflects its occurrence probability

\[ DL = 1 - Y^{(1-Z)} \]

J.T. Sousa, F.M. Gonçalves, J.P. Teixeira, T.W. Williams
"Fault Modeling and Defect Projections in Digital ICs"
Defect, fault modeling and test metrics

Extraction of realistic faults and Inductive fault analysis

Extraction of shorts in tracks.  
Critical area for shorts in two specified tracks.

“A Tool for Fault Extraction in PCBs”,  
L.C. Laranjeira, J. Machado da Silva, J.S. Matos  
IEEE European Test Workshop 2000
Defect, fault modeling and test metrics

When is a deviation considered a fault?
When is a fault considered detectable?

Signature analysis in amplitude and time domains
Defect, fault modeling and test metrics

Test errors

The cost of validation escapes are enormous (the Pentium FPDIV bug cost Intel $475 million)

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Defect, fault modeling and test metrics

Undetectable fault - no test exists for that fault

Redundant fault - undetectable fault but whose occurrence does not affect circuit operation

Testability = (#detectable faults) / #faults

Effective faults = faults - redundant faults

(These are the ones we must detect if we want to completely test the chip. Since redundant faults cause no harm, they should not be counted against us.)

\[ FC = \frac{DetectableFaults}{DefectiveFaults} = 1 - \frac{\int \int f_{MT}(m,t)dsdt - P_{PassTest}}{1 - P_{CircuitGood}} \]

(This is a better measure of how well a circuit is tested by a specific test method.)
DfT and BIST
Design for Testability and Built-in Self-Test

IC manufacturers have demanded high performance Automatic Test Equipment

Costly:
- 1 million $

Memory:
- Very high amount of data. Represents 40% of improvements in testers

Mixed-Signal Instrumentation:
- Higher bandwidth, higher sampling rates, higher accuracy, lower noise, etc.
- RF and audio circuits a major challenge, more when noisy digital circuitry is also present.

DUT to ATE interface:
- Higher pin-counts, high frequency & performance probes and sockets.
- No degradation of tester accuracy and noise.
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Design for Testability and Built-in Self-Test

Design for Testability

Set of techniques/methodologies aiming to improve the capability of generating, applying, and evaluating tests in order to comply with the required fault coverage objectives, subject to time and cost restrictions.

Key concepts:

• Accessibility
• Controllability - capability to activate internal nodes
• Observability - capability to observe internal nodes
• Partitioning
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Test difficulties – accessibility, observability

Plated through hole technology, 200 pin PGA

5 cm

Surface mount technology, 200 pin QFP

3 cm

Multichip module, 200 pad Bare Die

1 cm
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Subtle Forms of DfT

• Robust Circuits
  – Tighter statistical distributions centered between upper and lower test limits.
  – Robust circuits are much less expensive to test

• Design Margin
  – Generous design margins allow devices to be tested on less expensive testers
  – Doubling design margin reduces measurement sampling time by a factor of four
  – Designers often make margin decisions based purely on silicon area without consideration of test impact
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Subtle Forms of DfT

- **Avoiding over-specification**
  - Question the need for too tight specifications

- **Predictability of failure mechanisms**
  - Use circuits with simple, “predictable” failure modes even if they require more silicon area

- **Tester performance reduction**
  - In general, a low frequency tester is much less expensive than a high frequency tester
  - Tester with fewer digital pins is much less expensive
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Advantages of DfT

• Lower test cost
• Ease in test program development
• Higher test efficiency = product and process quality
• DfT observability and controllability provide means for enhanced diagnostic capabilities (through life-cycle) and processing problems
• Lower cycle time = increased profit
• Test resources available along the whole product life-cycle
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Test auxiliary circuitry

Disadvantages:

- Performance degradation
- Increased power consumption
- Area overhead
- Increased silicon increases development and manufacturing costs
- Increased defect occurrence probability
- Test engineers and design engineers must work as a team to determine the overall cycle time and cost impact of each DfT choice
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Economics of DfT

• Difficult to quantify cost savings
  – Can estimate test cost savings
  – Can’t calculate how much cycle time is reduced by a particular DfT choice
  – Lower cycle time results in higher profit margins, but how much higher?
  – How much business would be lost if DfT were not used to improve quality?

• Nevertheless, experience shows that DfT advantages outweigh the disadvantages
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Ad-hoc DfT hints

- Partition the circuit into functionally independent individual blocks
- Choose test nodes with similar electrical characteristics
- Avoid the necessity for multiple test instruments
- Explore as much as possible the resources already available in the circuit
- Choose the test sequence which allows for the best efficiency/test time relationship
- Use as much as simple test schemes as they can be
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Built-In Self Test (BIST)

– BIST is a subset of DfT
– BIST circuits provide the stimulus and response verification capabilities for testing on-chip
– Allows the DUT to evaluate its own quality with minimum ATE support
– Widely used in digital circuits, but not in analog and mixed-signal circuits
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Accessibility - physical vs. electronic access
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The need for hierarchical access

Problems with known good die:
- Single chip fault coverage: 95%
- MCM yield with 10 chips: $(0.95)^{10} = 60\%$

Primary access nodes

Test pad

Opens (48%)

Bad / Wrong part (7%)

Shorts (22%)

Missing / Misaligned part (19%)

<650µm

Damaged part (4%)
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Tester timing errors

Source: SIA Roadmap

Bandwidth gap between ATE and on-chip signals!

Device Period (nS)
Tester OTA (nS)
Projected Yield Loss (%)

Devices 30% per year

ATE: +12% per year approx.
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Analogue testing difficulties

• Different functional characteristics of the various blocks embedded in a circuit
• Diversity of amplitude and time characteristics of the different signals present in the same circuit
• Higher volume and accuracy of data to be processed
• Test methods and instruments are often inadequate to test the new circuit’s functionalities
• Lack of fast and generic tools to develop and evaluate test methods (test generation, simulation, stimuli generation)
• Higher sensitivity to process variations and measurement inaccuracy
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• There is no other way to cope with the cost and complexity of future ICs.
• Do not try to emulate a complete external testing - this is not practical in most cases. Functional testing must be reduced.
• Reduce costly or non-practical on-chip tests
  – Structural test is a clear powerful complement to functional testing
  – Structural test related to the I/O functional behavior
• Accessing: Yes, but non-intrusive
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The BIST Solution

• On-chip resources can run at the same speed than the CUT
• Avoid the need of external accessing
• Reduce interface to low bandwidth (control, low freq. signals, etc.)
• Customized test
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Design for Testability and Built-in Self-Test

Key aspects

• Re-usable and structured DfT & BIST techniques
  » Reduce I/O data rate requirements,
  » Enable low pin count testing, and
  » Reduce the dependence on expensive instruments.

• Structured Test planning
  » Enable hierarchical testing
  » Enable the re-use of on-chip resources (DSP, uP, etc.)
  » Facilitate parallel testing
  » etc.

• Standardized Test Access Mechanism
A generic test system model

Noise

$u'$ $u$ $\Sigma$

Circuit under test

$\Sigma$ $y'$$y$

Stimuli generator

Sensor / Observer

Time control

Response evaluation

Diagnostics

Test bus

Measurement uncertainty

External Tester

Interface

Faults

Modelling errors

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Test and DfT of Analog and Mixed-Signal Circuits
DfT and BIST
Design for Testability and Built-in Self-Test

- Testing embedded macros - Test what?
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Design for Testability and Built-in Self-Test

Approaches
- Infrastructures to access internal test nodes
- Inclusion of observation and evaluation blocks
- Local test stimuli generation
- Functional reconfiguration based schemes
- Built-in self-test
Infrastructures to access internal test nodes

- Multiplexing test nodes
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Infrastructures to access internal test nodes

- Analogue scan (observation)

Built-in self-test (BIST) structure for analog fault diagnosis
DfT and BIST

Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes

- PLL internal test

Motivations towards BIST and DfT for embedded charge-pump phase-locked loop frequency synthesizers. M.J. Burbidge, A. Lechner, G. Bell and A.M.D. Richardson

IEE Proc.-Circuits Devices Syst., Vol. 151, No. 4, August 2004

\[ K_{VCO} = \frac{f_2 - f_1}{V_{t2} - V_{t1}} \]
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Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes
• Design Diagnostics

Analog Test Input Bus

Mux | PGA | Filter | ADC

Analog Test Output Bus
DfT and BIST
Design for Testability and Built-in Self-Test

Infrastructures to access internal test nodes

- IEEE 1149.4 — Standard for a Mixed-Signal Test Bus

http://grouper.ieee.org/groups/1149/4/
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Insertion of observation and evaluation blocks

\[ S(t) = -\frac{1}{C} \int \sum_{i=1}^{n} \frac{v_i(t)}{R_i} dt \]

On-chip Analog Output Response Compaction
M. Renovell, F. Azais, Y. Bertrand
European Design & Test Conference, 1997
DfT and BIST
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Insertion of observation and evaluation blocks
- Multi-mode signature analyser

A multi-mode signature analyzer for analog and mixed circuits
M. Renovell, M. Lubaszewski, S. Mir, F. Azais, Y. Bertrand

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Insertion of observation and evaluation blocks
- Use of a Programmable Biquad

Improving the Testability of Switched-capacitor Filters
J.L.Huertas, A. Rueda, D.Vázquez
Journal of Electronic Testing, November 1993
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Insertion of observation

- ABSINT

"Control and observation of analog test nodes",
IEEE ITC, 1993
"An Approach to Testability Improvement of Mixed-Signal Boards",
IEEE ISCAS, 1994
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Local test stimuli generation

- $\Sigma \Delta$ modulated signals

![Diagram of ΣΔ modulated signals]

Characteristics
- Bit-Stream obtained from a 3rd order $\Sigma \Delta$ Modulator
- 804 bit length
- $f_{IN}$ at 5 kHz
- Clocked at $f_{CK}/2$

A BIST Scheme for SNDR Testing of $\Sigma \Delta$ ADCs Using Sine-Wave Fitting
Luis Rolindez, Salvador Mir, Ahcene Bounceur and Jean-Louis Carbonero
Proceedings of the 24th IEEE VLSI Test Symposium (VTS’06)
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Local test stimuli generation

- Multi-mode stimuli generator

A built-in multi-mode stimuli generator for analogue and mixed-signal testing
Lubaszewski M., Renovell M. Mir, S. Azans, F. Bertrand, Y.

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Local test stimuli generation
• Generation of pseudo-random signals

![Diagram of PRBS generator]

### Parameters
- \( m, n \): Lengths
- \( 2^m - 1 \): Total length

<table>
<thead>
<tr>
<th>( m )</th>
<th>( n )</th>
<th>Length (2^m - 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>3</td>
<td>15</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>63</td>
</tr>
<tr>
<td>8</td>
<td>4,5,6</td>
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<td>10</td>
<td>7</td>
<td>1023</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>32767</td>
</tr>
</tbody>
</table>

### Power Spectrum
- \( f_k = \frac{k}{M\Delta t} \)
- \( A(f_k) = \sqrt{\frac{M+1}{M}} \frac{k\pi}{M} \sin \frac{k\pi}{M} \) for \( k=1,2,3, \ldots \)
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Local test stimuli generation

- Discrete sinewave generation

For correctly weighted resistors
the 1st harmonic is of order $2^{m-1}$
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- Sinewave oscillator

\[ v_i(t) \rightarrow \Sigma \rightarrow 1/s \rightarrow v_o(t) \]
\[ \frac{v_o(t)}{v_i(t)} = \frac{s}{s^2 + s/Q + 1} \]

\[ v_i(n) \rightarrow \Sigma \rightarrow Z^{-1} \rightarrow v_o(n) \]
\[ v_o(n) = 2\cos(\omega_o) \cdot v_o[n-1] - v_o[n-2] \]
\[ v_o[-1] = 0; \quad v_o[-2] = -A_0 \sin(\omega_o); \quad \omega_o = 2\pi f_S \]

\[ \frac{V_o(z)}{V_i(z)} = \frac{z^{-1}}{1 - A_1z^{-1} - A_0z^{-2}} \]

\[ Zp_{1,2} = \frac{A_1/2 \pm j\sqrt{-A_1^2 - 4A_0}}{2} \]
\[ Zp_{1,2} = \cos(\omega_0 T_s) \pm j \sin(\omega_0 T_s) \]
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Functional reconfiguration based schemes

- Reconfiguration of universal biquadratic sections

\[ H_{UBSj}(s) = k_j \]
\[ H(s) = \prod_{j=1}^{m} k_j = k \]

A New Strategy for Testing Analog Filters
D. Vázquez, A. Rueda, J.L. Huertas
12th VLSI test Symposium, 1994

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Functional reconfiguration based schemes

- Oscillation test mode

<table>
<thead>
<tr>
<th>Normal mode</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>Test out</th>
<th>Components tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test mode f1</td>
<td>0</td>
<td>0</td>
<td>on</td>
<td>off</td>
<td>on</td>
<td>2</td>
<td>all</td>
</tr>
<tr>
<td>Test mode f2</td>
<td>1</td>
<td>2</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>2</td>
<td>all, but C1</td>
</tr>
<tr>
<td>Test mode f3</td>
<td>1</td>
<td>1</td>
<td>on</td>
<td>off</td>
<td>on</td>
<td>1</td>
<td>R1,R2,R3,C1,OA1</td>
</tr>
<tr>
<td>Test mode f4</td>
<td>1</td>
<td>1</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>1</td>
<td>R1,R2,R3,OA1</td>
</tr>
<tr>
<td>Test mode f5</td>
<td>1</td>
<td>0</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>2</td>
<td>R3,R4,R5,C1,C2,OA1,OA2</td>
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<tr>
<td>Test mode f6</td>
<td>1</td>
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<td>off</td>
<td>on</td>
<td>off</td>
<td>1</td>
<td>R1,R2,R3,OA1</td>
</tr>
</tbody>
</table>

Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method
K. Arabi, B. Kaminska
IEEE Transactions on CADICS, vol.16, no.7, July 1997

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Functional reconfiguration based schemes

- Oscillation test mode

A Low-Power Oscillation Based LNA BIST Scheme
José Machado da Silva, Proceedings DTIS, 2006

The extra transistors’ area overhead is smaller than 25%.
### DfT and BIST

**Design for Testability and Built-in Self-Test**

**Catastrophic faults**

<table>
<thead>
<tr>
<th>Par.</th>
<th>S11</th>
<th>S12</th>
<th>S21</th>
<th>S22</th>
<th>P1dB</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tol.</td>
<td>-15→-20</td>
<td>-47→-41</td>
<td>19.5→21.7</td>
<td>-22→-15</td>
<td>-18.5→-13</td>
<td>0.57→0.61</td>
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<tr>
<td>1-M$_{1gs}$</td>
<td>-1</td>
<td>-175</td>
<td>-147</td>
<td>-24</td>
<td>-40</td>
<td>147</td>
</tr>
<tr>
<td>2-M$_{1gds}$</td>
<td>-1</td>
<td>2</td>
<td>-4</td>
<td>3.8</td>
<td>14.6</td>
<td></td>
</tr>
<tr>
<td>3-L$_{gs}$</td>
<td>-1</td>
<td>-54</td>
<td>7.2</td>
<td>-18</td>
<td>-7.6</td>
<td>6</td>
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<tr>
<td>4-L$_{ss}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>5-M$_{2gss}$</td>
<td>-10</td>
<td>-214</td>
<td>-144</td>
<td>-24</td>
<td>-37</td>
<td>144</td>
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<tr>
<td>6-M$_{2dss}$</td>
<td>-7</td>
<td>-29.3</td>
<td>5.5</td>
<td>-5</td>
<td>&gt;5</td>
<td>0.87</td>
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<td>7-M$_{2gds}$</td>
<td>-7</td>
<td>-51</td>
<td>10.8</td>
<td>-5</td>
<td>&gt;5</td>
<td>0.82</td>
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<tr>
<td>8-M$_{1go}$</td>
<td>-1</td>
<td>-108</td>
<td>-47</td>
<td>&gt;5</td>
<td>54</td>
<td></td>
</tr>
<tr>
<td>9-R$_{bo}$</td>
<td></td>
<td></td>
<td>18</td>
<td>-20.6</td>
<td>0.56</td>
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<tr>
<td>10-L$_{so}$</td>
<td>-0</td>
<td>-139</td>
<td>-127</td>
<td>-11</td>
<td>-26</td>
<td>127</td>
</tr>
</tbody>
</table>

Observing a single parameter does not ensure a reliable fault detection.
DfT and BIST
Design for Testability and Built-in Self-Test
Catastrophic faults

<table>
<thead>
<tr>
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<th>Tol.</th>
<th>$R_{\text{out}}^F \frac{i^F}{D D}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-M$_{1gss}$</td>
<td>3.3</td>
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<tr>
<td>2-M$_{1gds}$</td>
<td>3.3</td>
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<tr>
<td>3-L$_{gs}$</td>
<td>3.3</td>
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<tr>
<td>4-L$_{ss}$</td>
<td>1.2</td>
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<td>5-M$_{2gss}$</td>
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### DfT and BIST

**Design for Testability and Built-in Self-Test**

**Parametric faults**

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<th>P1dB</th>
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</tr>
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<tbody>
<tr>
<td>11-Lg+20</td>
<td>-8</td>
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<td></td>
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<tr>
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<td></td>
<td>-10.7</td>
<td>0.55</td>
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<td>15-Ls+20</td>
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<td>16-Ls+10</td>
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<td>20-Lt+10</td>
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<td>23-Ct+20</td>
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# DfT and BIST

Design for Testability and Built-in Self-Test

## Parametric faults

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- Functional reconfiguration based schemes
**DfT and BIST**

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**Functional reconfiguration based schemes**
- ADC transfer characteristic observation

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**Flash A/D Converters – Design for Testability**
R. Ramadoss, M.L. Bushnell

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Functional reconfiguration based schemes
- Double-loop $\Sigma\Delta$ modulator

A BIST Technique for Sigma-Delta Modulators Based on Circuit Reconfiguration
S. Mir, A. Rueda, J. L. Huertas, and V. Liberali
3rd International Mixed-Signal Testing Workshop

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Functional reconfiguration based schemes
• Hybrid BIST

Hybrid Built-in self-test (HBIST) for mixed analogue/digital integrated circuits

Hybrid BIST

Digital core
A/D
D/A

MISR
BILB01
BILB02

A/D

Test control

A/D

Digital core

A/D

Test control
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Built-in Logic Block Observer

Parallel Inputs

EXOR Feedback Network

Scan-in

C1  C2  Mode
0   0  Scan
0   1  Clear
1   0  MISR
1   1  Normal

Parallel Output (Signature in Test Mode)

Built-in logic block techniques
B. Koenemann, J. Mucha, G. Zwiehof
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Functional reconfiguration based schemes
• MADBIST

1 - fully digital test
2 - convert D/A to oscillator
   (without smoothing filter)
3 - close Mux1
4 - test ADC
5 - DAC set to normal operation
6 - DAC can be tested after
   closing Mux2
7 - use DSP computational
   resources to implement a
   narrow band digital filter
   which allows computing
   parameters such as SNR
   and IMD

A BIST Scheme for an SNR test of a Sigma-Delta ADC
M.F. Toner, and G.W. Roberts
Proceedings of International Test Conference, 1993

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1. MADBIST
2. MADBIST
3. MADBIST
4. MADBIST
5. MADBIST
6. MADBIST
7. MADBIST
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• Mixed-signal BIST hurdles
  – Lack of robust traceability to central standards such as NIST
  – Designs are very close to specification limits requiring great accuracy in measurements
  – The use of on-chip stimulus and measurement circuits throws doubt into the accuracy of measurements, since there is a question about the quality of the signals generated and measured on a given DUT
DfT and BIST
Design for Testability and Built-in Self-Test

- BIST instrumentation is often inferior to ATE equipment
  - ATE is calibrated, traceable to NIST
  - ATE digitizers & sources include anti-aliasing and anti-imaging circuits
  - Circuit overhead to implement BIST is overwhelming unless circuits are already present in design (microprocessor, DSP, ADC, DAC etc)
  - Problems are not insurmountable, but mixed-signal BIST can’t be applied blindly
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Re-use of existing resources


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Glitch

Time [ms]
Output Voltage [V]

Power Supply Current [mA]

16-bit shift register

13-bit counter

13-bit counter

13-bit counter

Data out

Correlation Index
Normalised Polarity Correlation

Glitch

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Test and DfT of Analog and Mixed-Signal Circuits
DfT and BIST
Design for Testability and Built-in Self-Test

- Estimation of the amplifier’s nonlinearity.
- Automatic gain control
- Correction of eye diagrams’ opening

“An Adaptive Scheme for Estimating and Correcting RF Amplifiers’ Non-Linearities”
Pedro Mota, José Machado da Silva
APCCAS, 2008
Test and Design for Testability of Analog and Mixed-Signal Circuits

ACEOLE - PH-ESE Electronics Seminars
4-5 February 2010
José Machado da Silva

U.Porto – Faculdade de Engenharia
INESC Porto