The development and application of digital BPM signal processors at SSRF

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BI, SSRF
Outline

• Introduction
• Applications on SSRF
• Applications on FEL
• New processors for SHINE
SSRF introduction

- SSRF synchrotron radiation facility @ phase II
- soft x-ray FEL @ user facility
- hard x-ray FEL: SHINE @ tunnel construction

**e-beam:** 8 GeV
Photon energy: 0.4-25 keV
Pulse duration: 1-100fs
Repetition: 1MHz
Total length: 3.1km
ca. 38m underground

Longwei Lai, BI, SSRF
BPM Signal Processor Milestones

- **2009.9** Project Start
- **2010.12** Principle Prototype: RF front-end and Digital Signal Processing
  - Lai Longwei, Leng Yongbin*, Yi Xing, et al. DBPM signal processing with field programmable gate arrays[J], *NST* 22(2011), 129-133.
  - 赖龙伟，冷用斌*，阎映炳，杨桂森等，数字BPM信号处理算法研究，核技术，2010年，第33卷第10期，734-739
- **2011.6** Version-I and Beam Tests
  - 易星，冷用斌*，赖龙伟等. 基于软件无线电的新型数字束流位置处理器[J]，核技术，2012年，第35卷第5期
  - X. D. Sun, Y. B. Leng*, An DBPM Calibration Method Implemented on FPGA, IBIC 2012, Tsukuba, Japan
  - Leng Yongbin, Yi Xin, Lai Longwei, et al. Online Evaluation of New DBPM Processor at SINAP[C]// Prof of ICALEPCS2011,
  - 冷用斌，易星，赖龙伟等. 新型数字BPM信号处理器研制进展[J]，核技术，2011年，第33卷第5期，326-330
  - X.D. Sun, Y.B. Leng. Implementation and integration of a systematic DBPM calibration [J], *NST* 25(2014), 020401-1-6.
  - 赖龙伟，冷用斌，易星等. 数字束流位置信号处理算法优化[J]，强激光与粒子束,2013年，第25卷第1期，109-113
- **2014.6** Small amount(5) tests
- **2015.6** Optimization, Intelligent Trigger Application Development
  - L.W. Lai, Y.B. Leng, AN INTELLIGENT TRIGGER ABNORMAL BEAM OPERATION MONITORING PROCESSOR AT THE SSRF, IPAC2015
  - L.W. Lai, Y.B. Leng, THE APPLICATION OF DIRECT RF SAMPLING SYSTEM ON CAVITY BPM SIGNAL PROCESSING, IBIC2017
- **2016.6** Version-II, Volume Application on SXFEL, DCLS and Sirius LINAC
  - L.W. Lai, Y.B. Leng, BATCH APPLICATIONS OF DIGITAL BPM PROCESSORS FROM THE SINAP, IBIC2016
  - L.W. Lai, Y.B. Leng, DESIGN AND PERFORMANCE OF DIGITAL BPM PROCESSOR FOR DCLS AND SXFEL, IPAC2017
- **2017.12** Firmware and software upgrade for SXFEL
  - L.W.Lai, et.al, UPGRADE OF DIGITAL BPM PROCESSOR AT DCLS AND SXFEL, IBIC2018
- **2017 Ideas on direct RF sampling BPM processor for C band cavity BPM**
  - L.W.Lai, et.al, THE APPLICATION OF DIRECT RF SAMPLING SYSTEM ON CAVITY BPM SIGNAL PROCESSING, IBIC2017
- **2018.1** Firmware and software upgrade for SSRF
  - L.W.Lai, et.al, THE DEVELOPMENT AND APPLICATIONS OF DIGITAL BPM SIGNAL PROCESSOR ON SSRF, IBIC2018
- **2019.4** 10 units on-line operation on SSRF
- **2019** Start new processor design for SHINE
Processor Overview

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>Channels</td>
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<tr>
<td>Central Frequency</td>
<td>500MHz/wideband</td>
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<tr>
<td>Bandwidth</td>
<td>~20MHz/wideband</td>
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<tr>
<td>Dynamic range</td>
<td>31dB/NA</td>
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<tr>
<td>ADC bits</td>
<td>16</td>
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<tr>
<td>ADC bandwidth</td>
<td>650MHz</td>
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<tr>
<td>Max ADC rate</td>
<td>125MSPS</td>
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<tr>
<td>FPGA</td>
<td>Xilinx xc5vsx50t</td>
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<tr>
<td>Clock</td>
<td>Ext./Int.</td>
</tr>
<tr>
<td>Trigger</td>
<td>Ext./Self/Period</td>
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<tr>
<td>Software</td>
<td>Arm-Linux/EPICS</td>
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</table>

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Applications on SSRF
Applications on SSRF

Small amount of processors are installed on SSRF:
- LINAC 1/3
- LTB 1/3
- Booster 3/30
- BTS 4/5
- Storage ring 1/140

More will be installed gradually…
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Version-II DBPM Beam Tests on SR@Jan. 2018

K=10mm, Turn-by-turn resolution:0.34μm
Control panel and data

ADC data

Turn-by-turn data during injection

Turn-by-turn data

SA data

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SSRF Beam Test—Check With Brilliance

Assuming the Brilliance results are correct. Data spectrums show they fit quite well.
BPM pickup sum signal is divided into 8 channels and put into DBPM and Brilliance, similar to beam passing through BPM center. The output position value should be stable.

The DBPM output is **drifting** when beam current decays from 260mA to 200mA. Brilliance output is stable when crossbars are switched off. The main reason is the **inconsistency** between the four channels.

Fit polynomial to data.

\[ P = \text{POLYFIT}(X,Y,N), \quad N=3 \]

\[ X: \text{SA channel read out} \]

\[ Y: \text{current, mA} \]

\[ Y=P(1)\times X^3 + P(2)\times X^2 + P(3)\times X + P(4) \]

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SSRF Beam Test—Correction

X fits well after correction.
Y not very good.
Correction effect is obvious during injection.
Beam test on booster

Streaming data or capture data for:
- ADC raw data
- turn-by-turn data
- 7.9kHz data (TBT/210), cover ramping period within 2000 points

TBT data spectrum during one injection

x/y/sum of one top-up period (five injections)
SSRF Operation Monitor

Monitoring beam status and capture data when injection is detected.


TBT data waveform and spectrum during injecting. (Hor.)

Normalized frequency

Tune monitoring.
Bunch Charge Monitor

4 ADCs on wideband RF board make bunch-by-bunch charge measurement with **interleaved sampling**. Optimization is ongoing.
Applications on FEL/LINAC

Stripline BPM Processor
Cavity BPM Processor
BAM processor

DCLS
SXFEL
Sirius LINAC

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Mass Application on SXFEL/DCLS
SBPM Evaluation

Vertical displacement is getting larger along the beam direction.

Charge measurement accuracy is getting worse when the beam moving from center.
Phase and k Calibration

Phase calibration tests.

X phase distribution is wider than Y, caused by beam tilt in X direction.

Kx = 0.37

Ky = 0.34

K calibration tests.
Processor for SHINE

Cold button BPM processor
Stripline BPM processor
Cavity BPM processor

......

➤ ADC+FPGA
Processor Overview

- standalone structure based on Xilinx SOC
- common platform for beam signal processing...
- FMC ADC and timing mezzanine cards
- IF sampling / RF sampling ADC card, 1MHz repetition rate
Hardware

- Refer to the design of Xilinx ZCU102 evaluation board
- Zynq Ultrascale SOC FPGA ZU19EG
- $\geq 500\text{MSPS}$, $\geq 14$ bits IF sampling processor (AC&DC), also can be used as BxB processor on synchrotron facility
- RF direct sampling technique (bandwidth $> 5\text{GHz}$) is also studied for C band cavity BPM signal processor, $\geq 14$ bits
**Table 1: Virtex-5 FPGA Family Members**

<table>
<thead>
<tr>
<th>Device</th>
<th>Configurable Logic Blocks (CLBs)</th>
<th>Block RAM Blocks</th>
<th>PowerPC Processor Blocks</th>
<th>Endpoint Blocks for PCI Express</th>
<th>Ethernet MACs&lt;sup&gt;(5)&lt;/sup&gt;</th>
<th>Max RocketIO Transceivers&lt;sup&gt;(6)&lt;/sup&gt;</th>
<th>Total I/O Banks&lt;sup&gt;(6)&lt;/sup&gt;</th>
<th>Max User I/O&lt;sup&gt;(7)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC5VSX50T</td>
<td>120 x 34&lt;br&gt;8,160&lt;br&gt;780&lt;br&gt;288</td>
<td>18 Kb&lt;sup&gt;(3)&lt;/sup&gt; 36 Kb&lt;br&gt;132&lt;br&gt;4,752</td>
<td>6&lt;br&gt;N/A</td>
<td>1&lt;br&gt;4</td>
<td>12&lt;br&gt;N/A</td>
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<tr>
<td>XC5VSX95T</td>
<td>160 x 46&lt;br&gt;14,720&lt;br&gt;1,520&lt;br&gt;640</td>
<td>488&lt;br&gt;244&lt;br&gt;8,784</td>
<td>6&lt;br&gt;N/A</td>
<td>1&lt;br&gt;4</td>
<td>16&lt;br&gt;N/A</td>
<td>19&lt;br&gt;640</td>
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**Zynq UltraScale+ MPSoC: EG Device Feature Summary**

**Table 13: Zynq UltraScale+ MPSoC: EG Device Feature Summary**

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<thead>
<tr>
<th>ZU2EG</th>
<th>ZU3EG</th>
<th>ZU4EG</th>
<th>ZU5EG</th>
<th>ZU6EG</th>
<th>ZU7EG</th>
<th>ZU9EG</th>
<th>ZU18EG</th>
<th>ZU19EG</th>
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<tbody>
<tr>
<td>Application Processing Unit</td>
<td>Quad-core Arm Cortex-A53 MPcore with CoreSight; NEON 8 Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB 2 Cache</td>
<td>Quad-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM</td>
<td>256KB On-Chip Memory w/ ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPi; NAND; eMMC</td>
<td>214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters</td>
<td>4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMMI</td>
<td>Arm Mali-400 MP2; 64KB L2 Cache</td>
<td>1,152,450</td>
<td>1,045,440</td>
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<tr>
<td>CLB Flip-Flips</td>
<td>103,320&lt;br&gt;154,350&lt;br&gt;192,150&lt;br&gt;256,200</td>
<td>256,200&lt;br&gt;469,466&lt;br&gt;504,000&lt;br&gt;599,550</td>
<td>653,100&lt;br&gt;746,550&lt;br&gt;926,194</td>
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<td>CLB LUTs</td>
<td>94,464&lt;br&gt;141,120&lt;br&gt;175,680&lt;br&gt;234,240</td>
<td>234,240&lt;br&gt;429,208&lt;br&gt;460,800&lt;br&gt;548,160</td>
<td>597,120&lt;br&gt;682,560&lt;br&gt;846,806</td>
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<td>Distributed RAM (Mb)</td>
<td>47,232&lt;br&gt;70,560&lt;br&gt;87,840&lt;br&gt;117,120</td>
<td>117,120&lt;br&gt;214,604&lt;br&gt;234,400&lt;br&gt;274,080</td>
<td>298,560&lt;br&gt;341,280&lt;br&gt;423,463</td>
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<td>Block RAM Blocks</td>
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<td>144&lt;br&gt;714&lt;br&gt;312&lt;br&gt;600</td>
<td>744&lt;br&gt;796&lt;br&gt;796&lt;br&gt;796</td>
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<td>DSP Slices</td>
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<td>1,248&lt;br&gt;1,973&lt;br&gt;1,728&lt;br&gt;2,520</td>
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<td>Max. HP I/O&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>156&lt;br&gt;208&lt;br&gt;416&lt;br&gt;416</td>
<td>416&lt;br&gt;208&lt;br&gt;416&lt;br&gt;416</td>
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<td>System Monitor</td>
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<td>GTH Transceivers 16.3Gb/s&lt;sup&gt;(3)&lt;/sup&gt;</td>
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<td>100G Interlaken</td>
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<td>100G Ethernet w/ RS-FC</td>
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**Notes:**
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SPVC784 package support data rates up to 12.5Gb/s. See Table 14.

**Longwei Lai, BI, SSRF**
FPGA design overview

- ADC Interface
- Signal Processing Module (algorithm config.)
- Data Flow Control Manager
- Timing Interface
- Clock Config.
- SFP Interface
- DMA
- SDRAM Interface
- Trigger Config. (delay control, mode config.)
- System Monitor
- Register Control Manager
- Interlock Module
- User IO & LED
- PS-PL Interface
- APP
- SD
- QSPI
- UART
- ETH
- USB
- HDMI
- Driver
- OS

Longwei Lai, BI, SSRF
BxB DBPM / PT Acc. DBPM / TBF Processor

SP Device PXI board.

BPM Processor on Proton Therapy Accelerator. On-line.

Bunch-by-bunch transverse feedback processor. Tested on SSRF.

Longwei Lai, BI, SSRF

500M bunch-by-bunch BPM processor Tested on SSRF.
<table>
<thead>
<tr>
<th>Facility</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brazil Sirius LINAC</td>
<td>2+</td>
</tr>
<tr>
<td>DCLS</td>
<td>19+</td>
</tr>
<tr>
<td>SXFEL test facility</td>
<td>60</td>
</tr>
<tr>
<td>SXFEL user facility</td>
<td>50</td>
</tr>
<tr>
<td>SSRF</td>
<td>10+</td>
</tr>
<tr>
<td>SHINE</td>
<td>300+</td>
</tr>
</tbody>
</table>
Thanks for your attention