The development and application of digital BPM signal processors at SSRF

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BI, SSRF

DEELS2019 ESRF

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Outline

- Introduction
- Applications on SSRF
- Applications on FEL
- New processors for SHINE

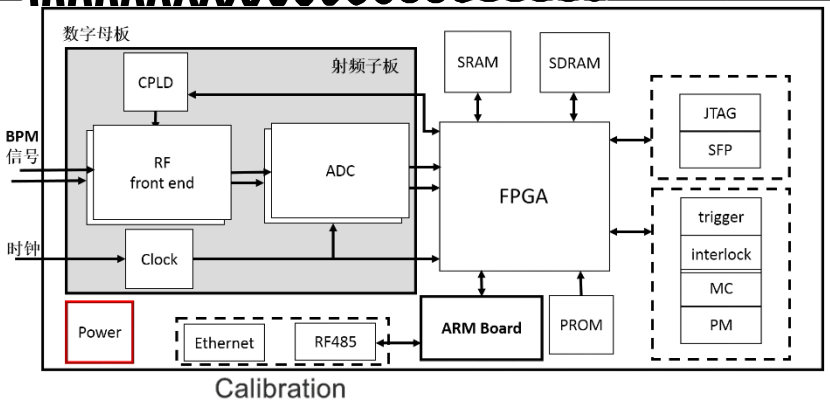
SSRF introduction

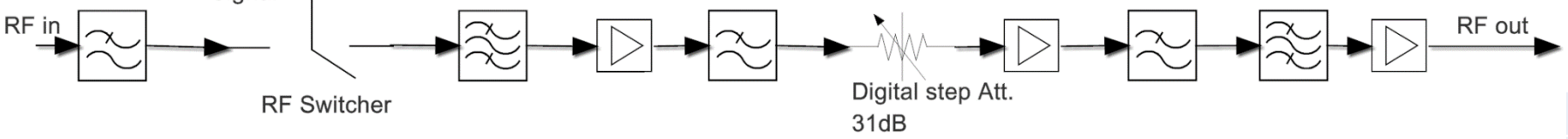
- SSRF synchrotron radiation facility @ phase II
- soft x-ray FEL @ user facility
- hard x-ray FEL: SHINE @ tunnel construction

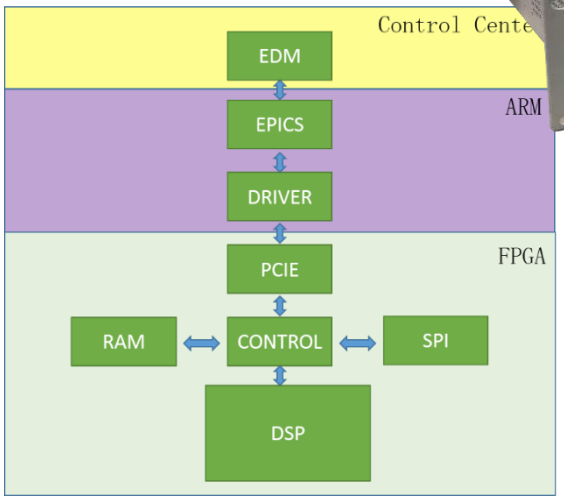
BPM Signal Processor Milestones

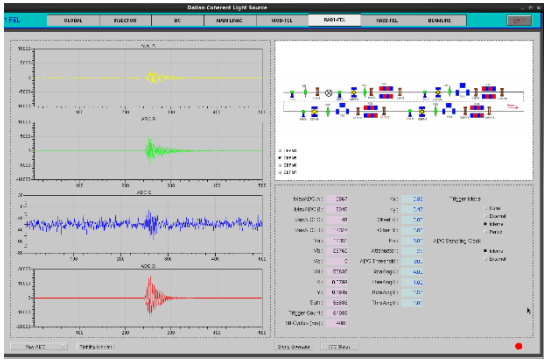
- **2009.9 Project Start**
- **2010.12 Principle Prototype: RF front-end and Digital Signal Processing**
- Lai Longwei, Leng Yongbin*, Yi Xing, et al. DBPM signal processing with field programmable gate arrays[J], *NST* 22(2011), 129-133.
- Yi Xing, Leng Yongbin*, Lai Longwei, *et al*. RF front-end for digital beam position monitor signal processor[J], *NST* 22(2011), 65-69.
- 赖龙伟，冷用斌*，阎映炳，杨桂森等，数字BPM信号处理算法研究，核技术，2010年，第33卷第10期，734-739
- **2011.6 Version-I and Beam Tests**
- 易星，冷用斌*，赖龙伟等. 基于软件无线电的新型数字束流位置处理器[J]，核技术，2012年，第35卷第5期
- X. D. Sun, Y. B. Leng*, An DBPM Calibration Method Implemented on FPGA, IBIC 2012, Tsukuba, Japan
- Leng Yongbin, Yi Xin, Lai Longwei, et al. Online Evaluation of New DBPM Processor at SINAP[C]// Prof of ICALEPCS2011,
- 冷用斌，易星，赖龙伟等. 新型数字BPM信号处理器研制进展[J]，核技术，2011年，第33卷第5期，326-330
- X.D. Sun, Y.B. Leng. Implementation and integration of a systematic DBPM calibration [J], *NST* 25(2014), 020401-1-6.
- X.D. Sun, Y.B. Leng. MATLAB Simulation of DBPM Digital Down Conversion [J] *AMM*, 333(2013), 680-683.
- 赖龙伟，冷用斌，易星等. 数字束流位置信号处理算法优化[J], 强激光与粒子束,2013年，第25卷第1期，109-113
- **2014.6 Small amount(5) tests**
- **2015.6 Optimization, Intelligent Trigger Application Development**
- L.W. Lai, Y.B. Leng, AN INTELLIGIENT TRIGGER ABNORMAL BEAM OPERATION MONITORING PROCESSOR AT THE SSRF, IPAC2015
- 赖龙伟，冷用斌等. 数字BPM信号处理器研制进展[J], 原子能科学技术,2015
- **2016.6 Version-II, Volume Application on SXFEL, DCLS and Sirius LINAC**
- L.W. Lai, Y.B. Leng, BATCH APPLICATIONS OF DIGITAL BPM PROCESSORS FROM THE SINAP, IBIC2016
- L.W. Lai, Y.B. Leng, DESIGN AND PERFORMANCE OF DIGITAL BPM PROCESSOR FOR DCLS AND SXFEL, IPAC2017
- **2017.12 Firmware and software upgrade for SXFEL**
- L.W.Lai, , et.al, UPGRADE OF DIGITAL BPM PROCESSOR AT DCLS AND SXFEL, IPAC2018
- **2017 Ideas on direct RF sampling BPM processor for C band cavity BPM**
- L.W.Lai, et.al, THE APPLICATION OF DIRECT RF SAMPLING SYSTEM ON CAVITY BPM SIGNAL PROCESSING, IBIC2017
- **2018.1 Firmware and software upgrade for SSRF**
- L.W.Lai , et.al, THE DEVELOPMENT AND APPLICATIONS OF THE DIGITAL BPM SIGNAL PROCESSOR AT SINAP, FLS2018
- L.W.Lai , et.al, THE DEVELOPMENT AND APPLICATIONS OF DIGITAL BPM SIGNAL PROCESSOR ON SSRF, IBIC2018
- **2019.4 10 units on-line operation on SSRF**
- **2019 Start new processor design for SHINE**

Processor Overview









Channels	4
Central Frequency	500MHz/wideband
Bandwidth	~20MHz/wideband
Dynamic range	31dB/NA
ADC bits	16
ADC bandwidth	650MHz
Max ADC rate	125MSPS
FPGA	Xilinx xc5vsx50t
Clock	Ext./Int.
Trigger	Ext./Self/Period
Software	Arm-Linux/EPICS

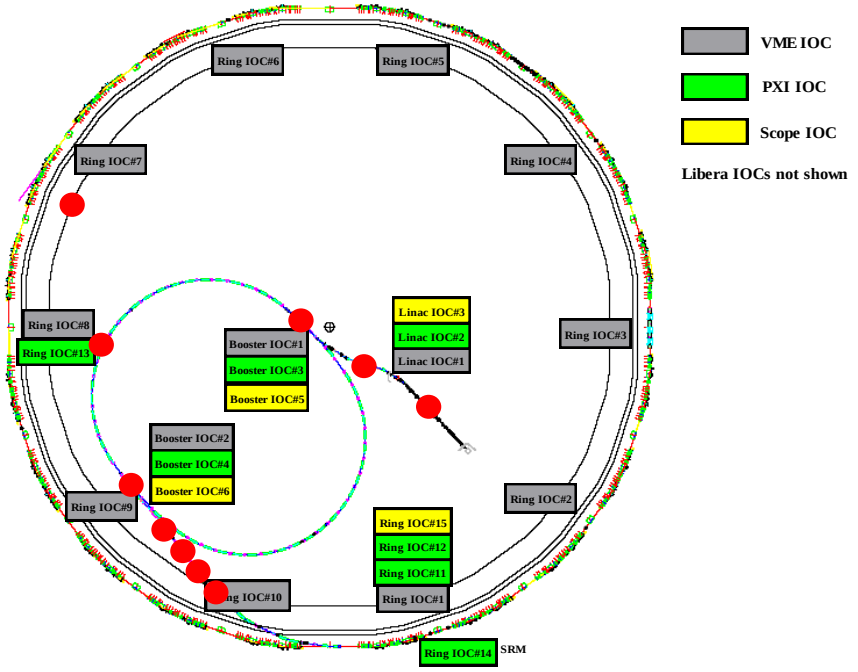
Applications on SSRF

Applications on SSRF

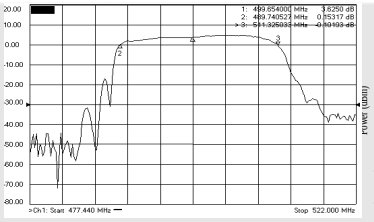
Small amount of processors are installed on SSRF:

- LINAC 1/3
- LTB 1/3
- Booster 3/30
- BTS 4/5
- Storage ring 1/140

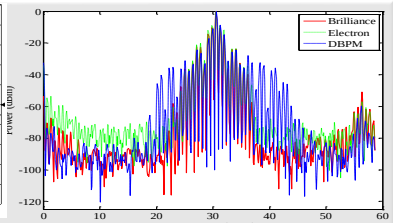
More will be installed gradually…



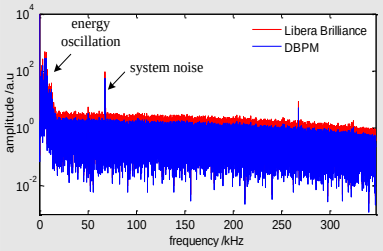
Version-I DBPM Beam Tests on SR@2012



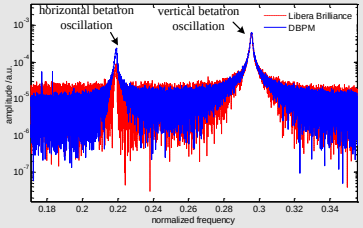
RF 3dB bandwidth



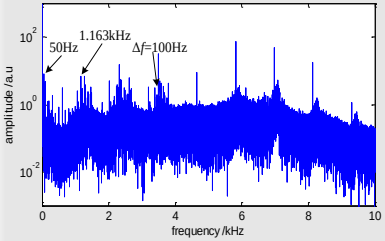
ADC Spectrum



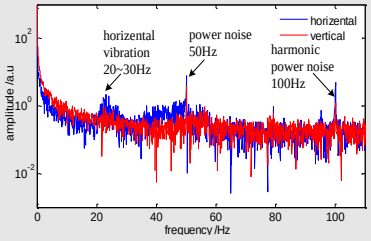
TBT Spectrum



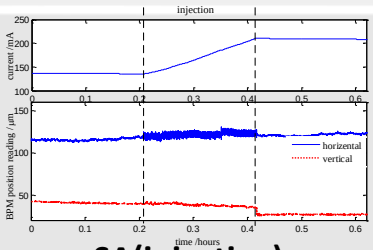
TBT Spectrum(injecting)



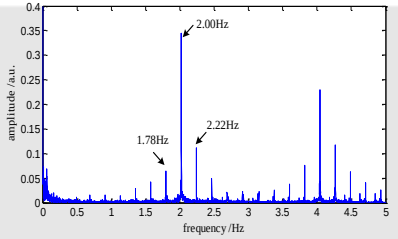
FA Spectrum



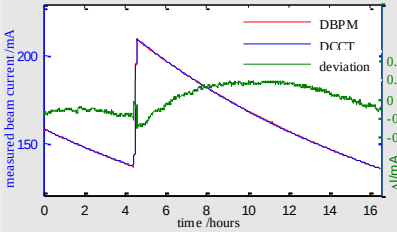
FA Spectrum(zoom in)



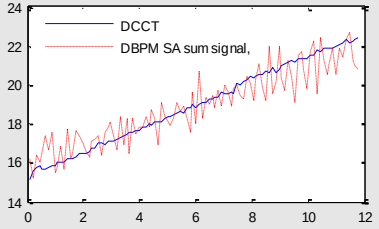
SA(injecting)



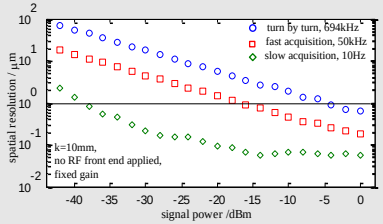
SA Spectrum(injecting)



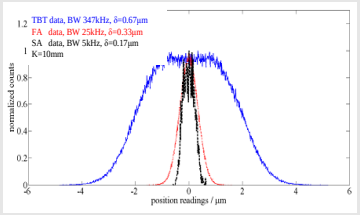
Current Meas. With SA



Life Meas. With SA

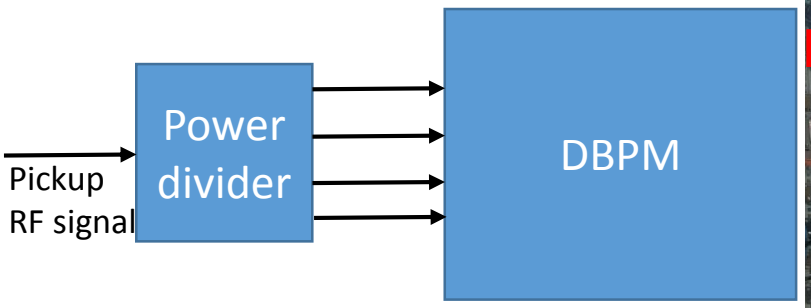


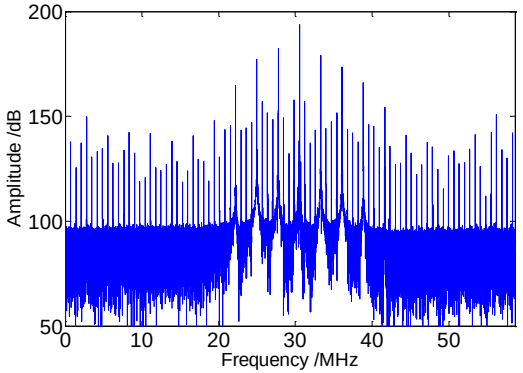
RMS Eval. At Lab

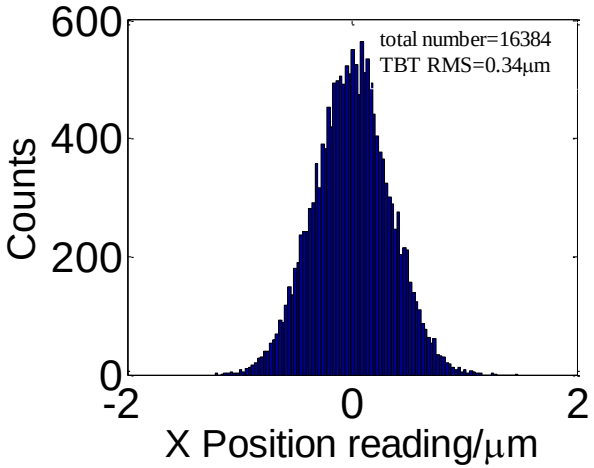


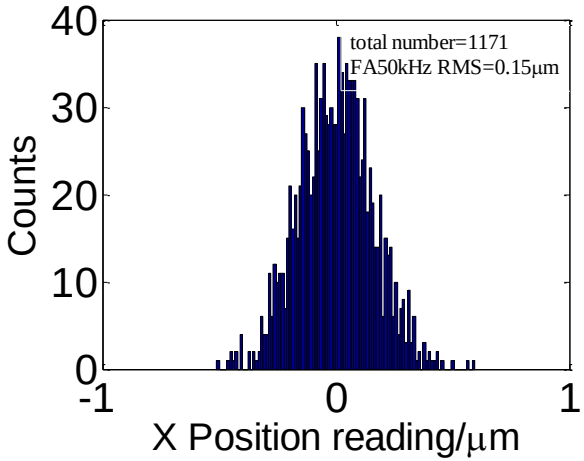
RMS Eval. On SSRF

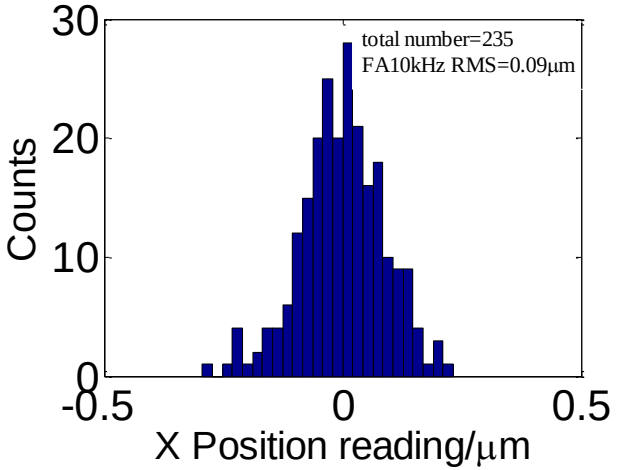
Version-II DBPM Beam Tests on SR@Jan. 2018





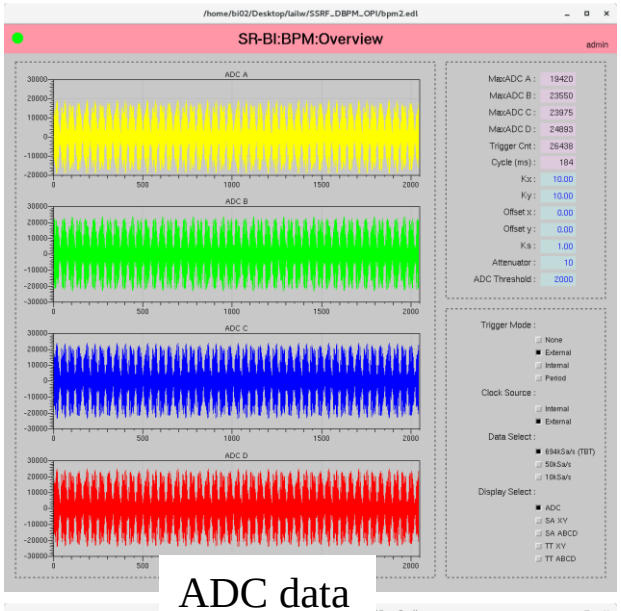




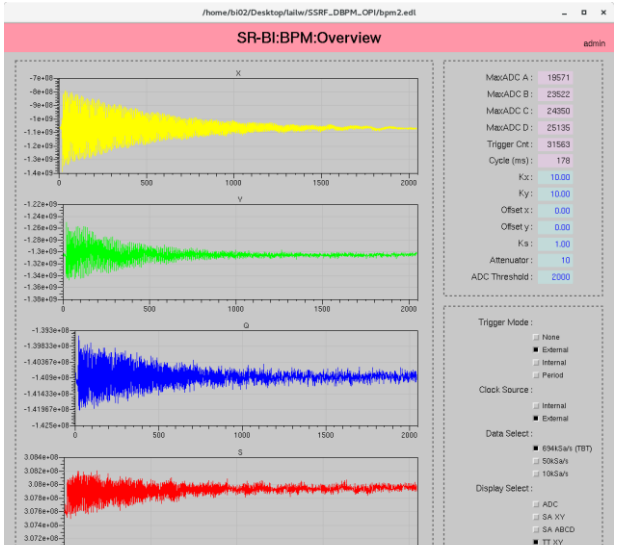


K=10mm, Turn-by-turn resolution:0.34μm

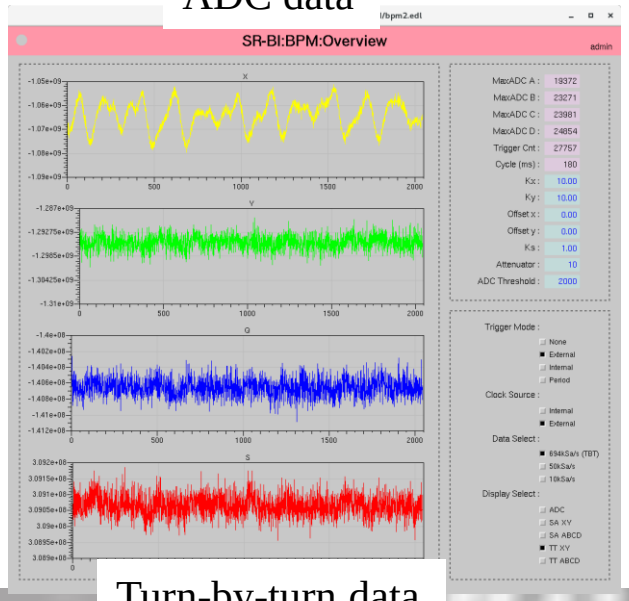
Control panel and data



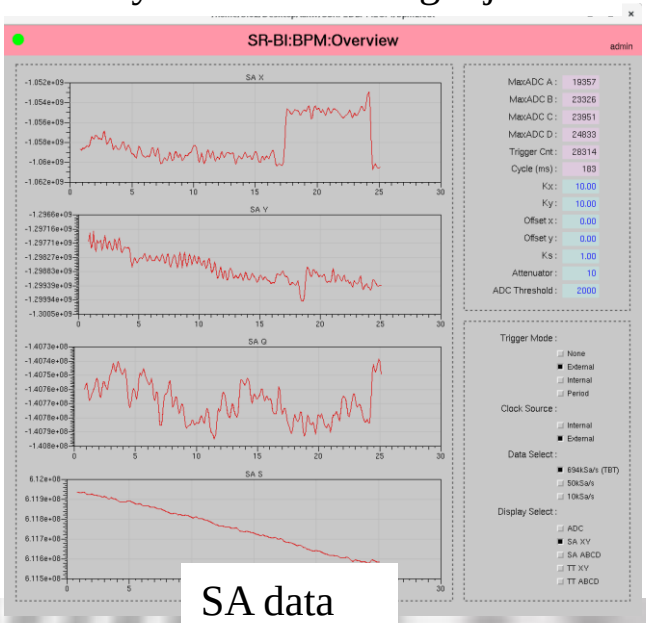
ADC data



Turn-by-turn data during injection

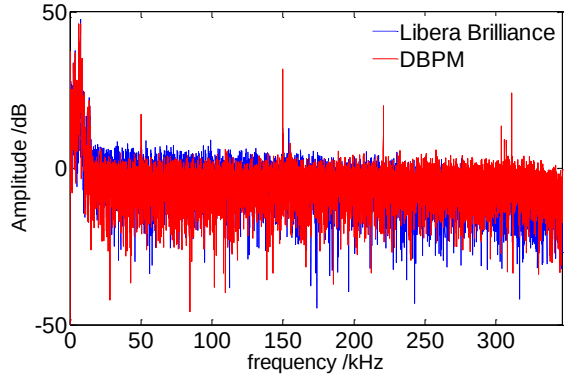


Turn-by-turn data

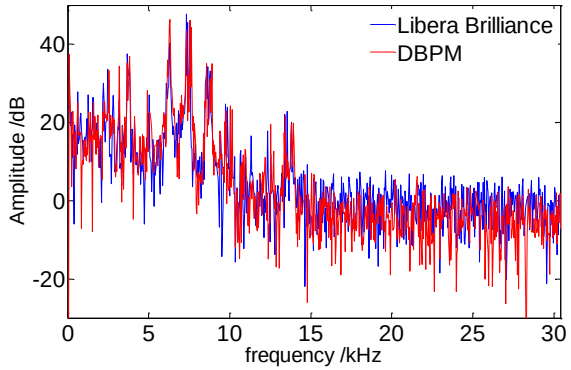


SA data

SSRF Beam Test—Check With Brilliance

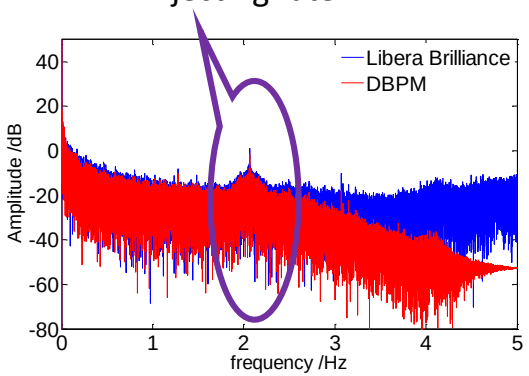


TBT X

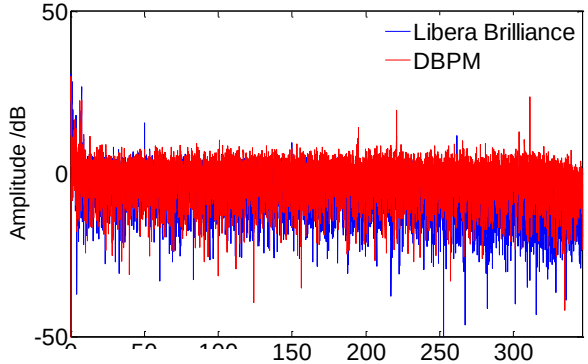


TBT X(zoom in)

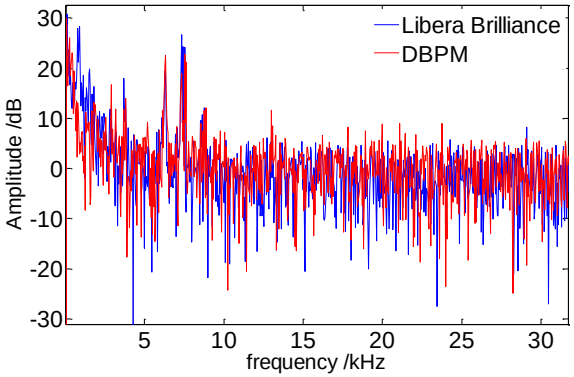
~2Hz injecting rate



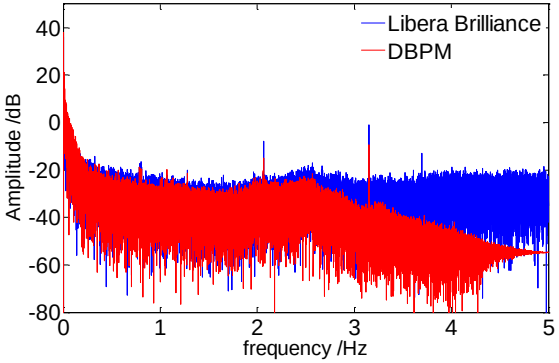
SA X



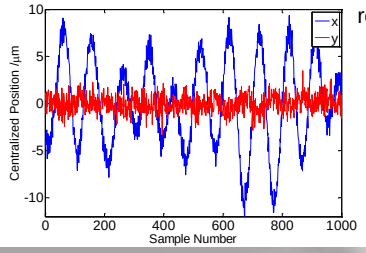
TBT Y



TBT Y(zoom in)



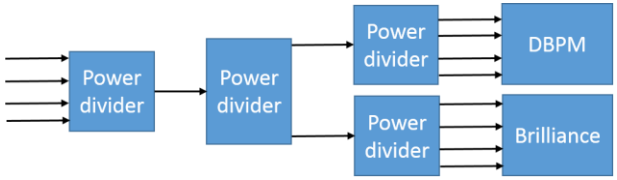
SA Y

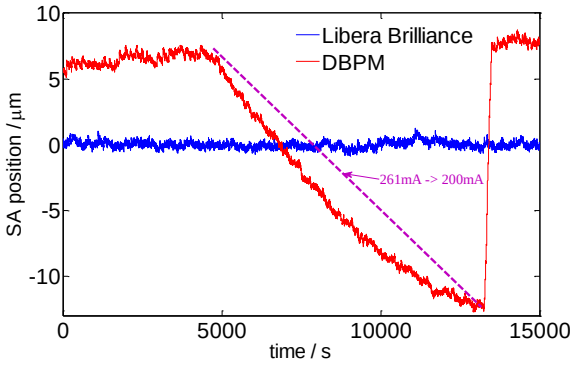


Assuming the Brilliance results are correct.

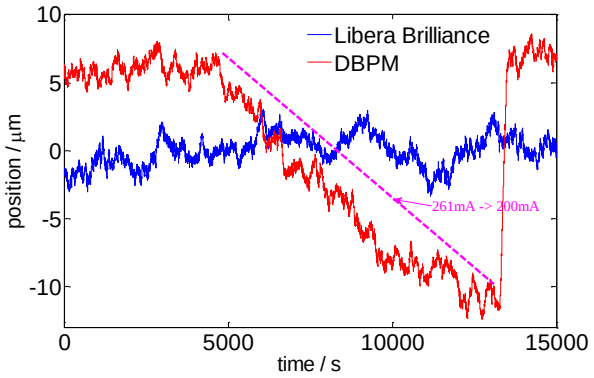
Data spectrums show they fit quite well.

SSRF Beam Test—Current Dependency





SA X



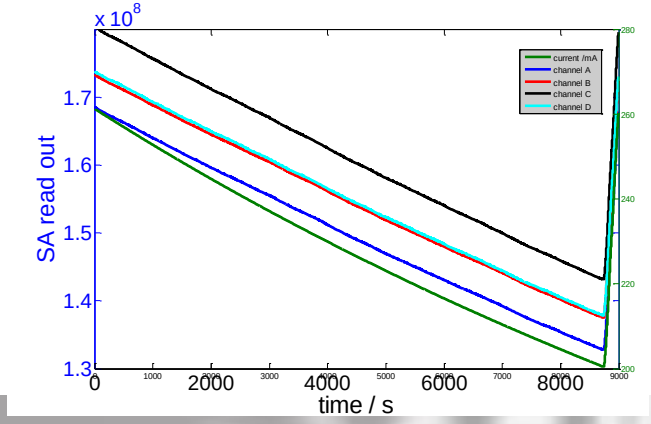
SA Y

BPM pickup sum signal is divided into 8 channels and put into DBPM and Brilliance, similar to beam passing through BPM center. The output position value should be stable.

The DBPM output is drifting when beam current decays from 260mA to 200mA.

Brilliance output is stable when crossbars are switched off.

The main reason is the inconsistency between the four channels.



Fit polynomial to data.

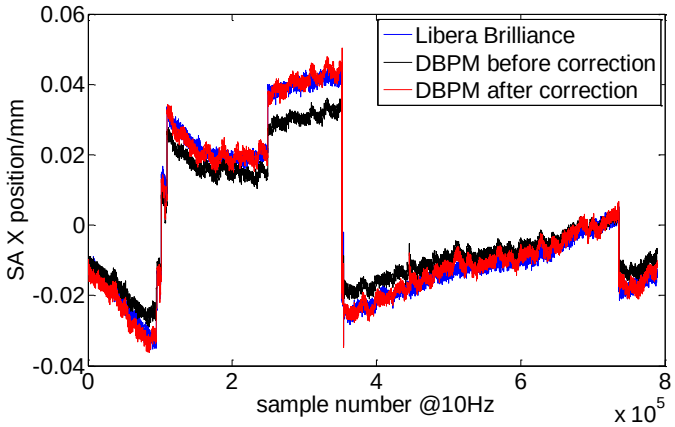
P = POLYFIT(X,Y,N), N=3

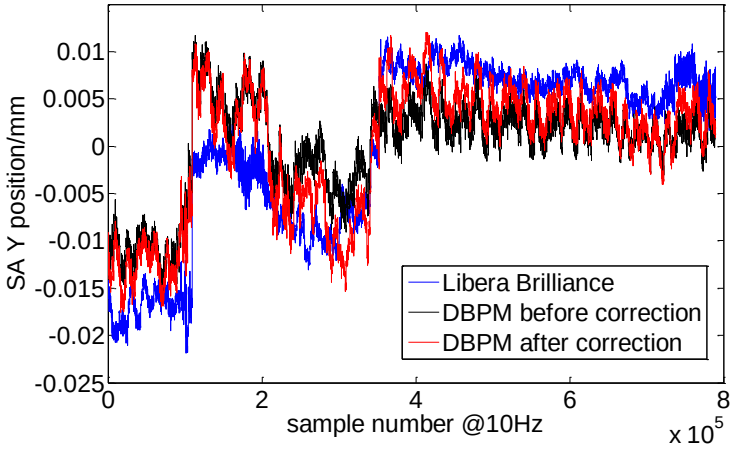
X: SA channel read out

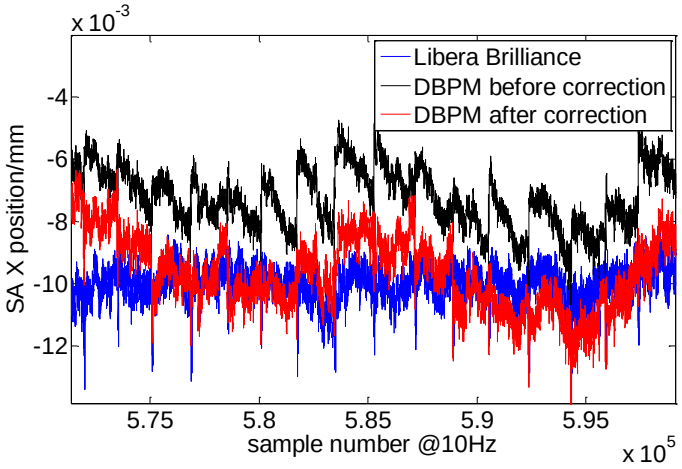
Y: current, mA

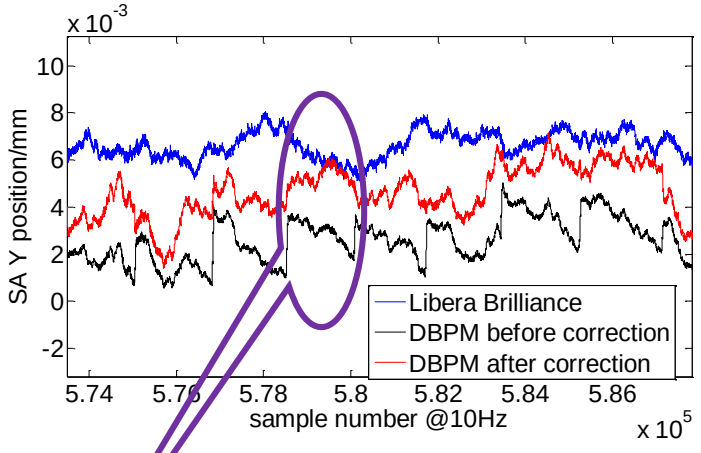
Y=P(1)*X^3 + P(2)*X^2+P(3)*X + P(4)

SSRF Beam Test—Correction









X fits well after correction.

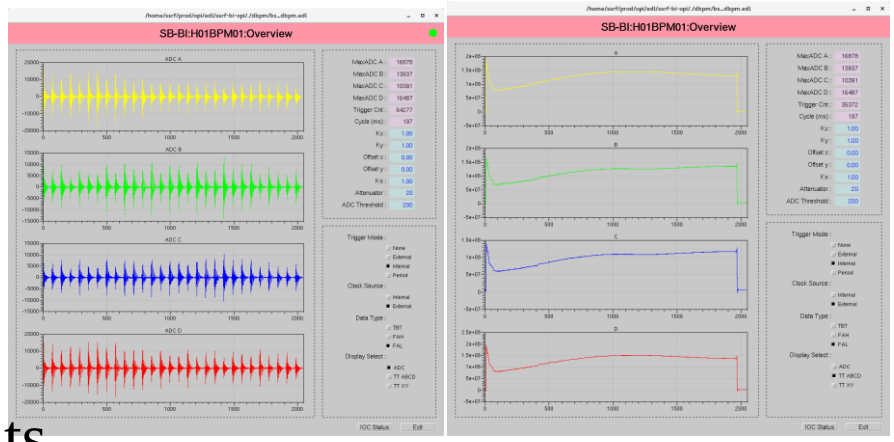
Y not very good.

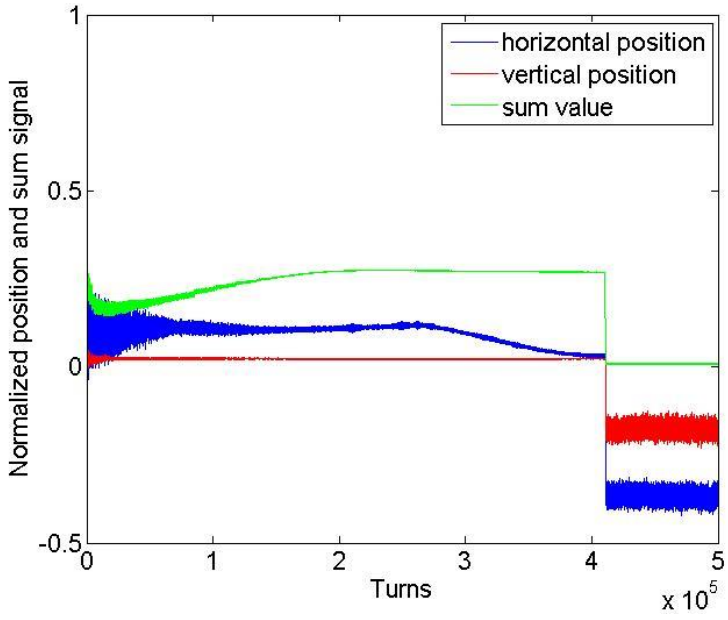
Correction effect is obvious during injection.

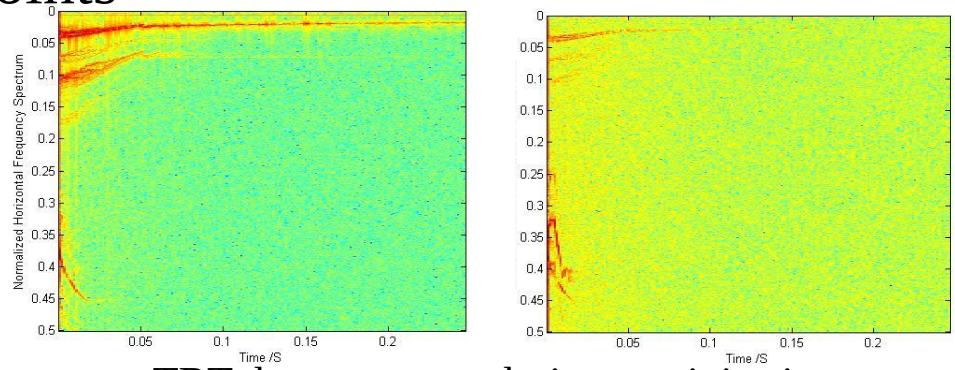
Beam test on booster

Streaming data or capture data for:

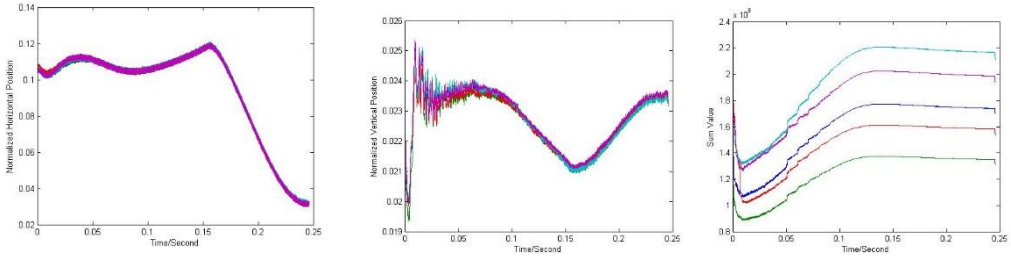
- ADC raw data
- turn-by-turn data
- 7.9kHz data(TBT/210), cover ramping period within 2000 points





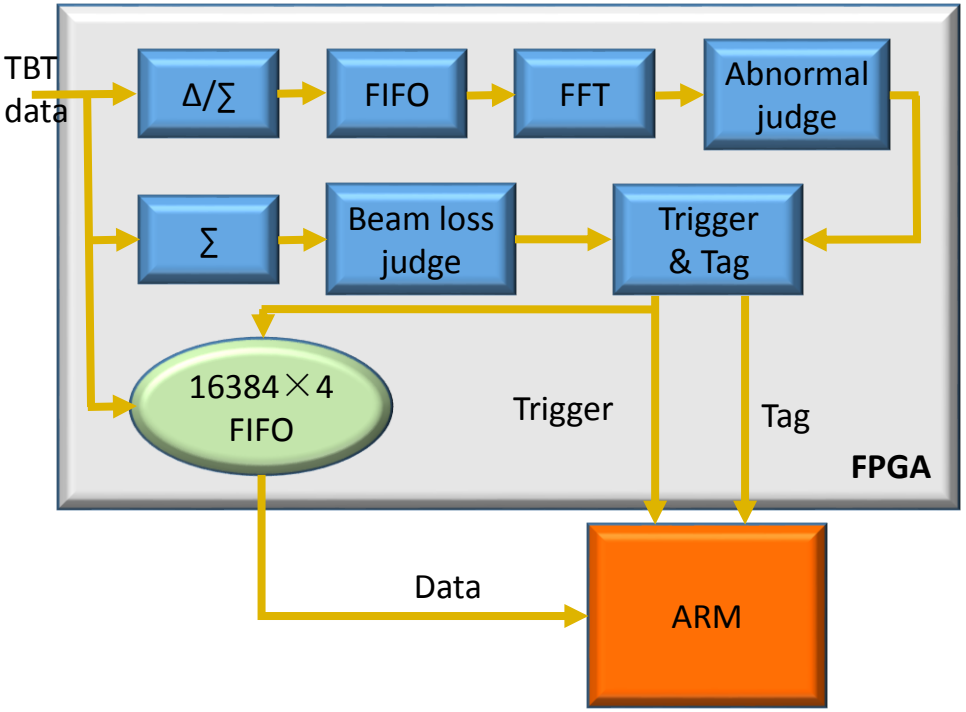


TBT data spectrum during one injection

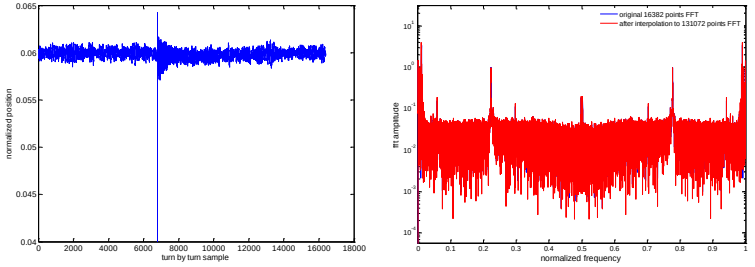


x/y/sum of one top-up period(five injections)

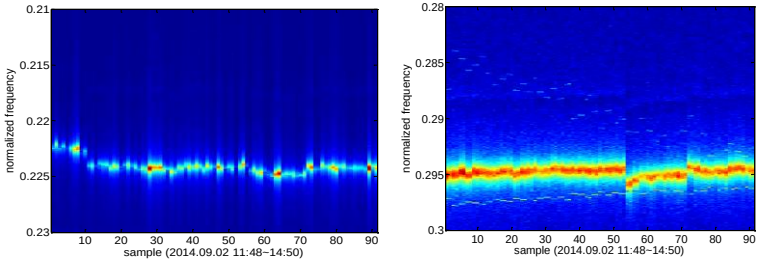
SSRF Operation Monitor



Monitoring beam status and capture data when injection is detected.



TBT data waveform and spectrum during injecting.(Hor.)

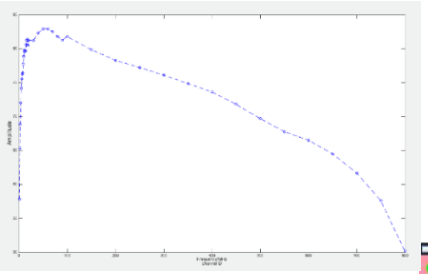


Tune monitoring.

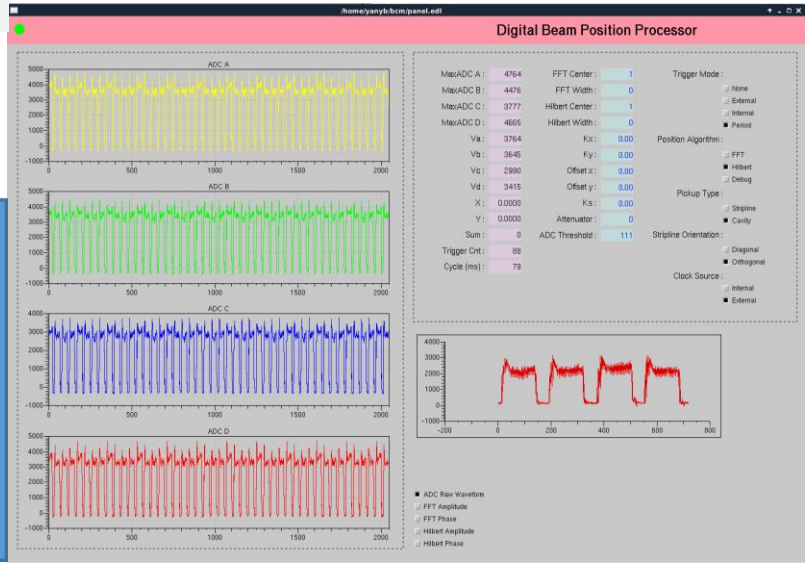
L.W. Lai, Y.B. Leng, Y.B. Yan, Z.C. Chen,An Intelligent Trigger Abnormal Beam Operation Monitoring Processor at the SSRF, IPAC2015

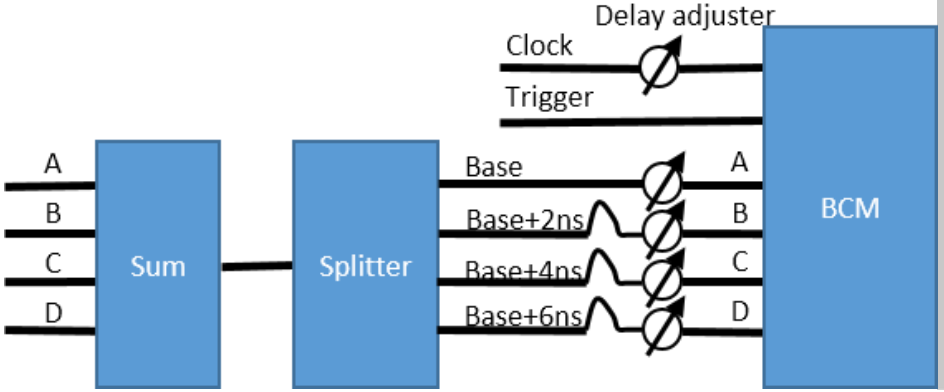
Bunch Charge Monitor

4 ADCs on wideband RF board make bunch-by-bunch charge measurement with interleaved sampling. Optimization is ongoing.



Wideband ADC board





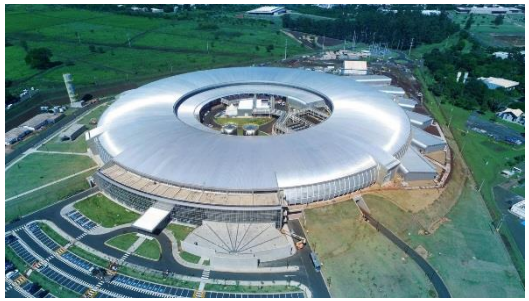
Interleaved Sampling

Applications on FEL/LINAC

Stripline BPM Processor
Cavity BPM Processor
BAM processor

DCLS

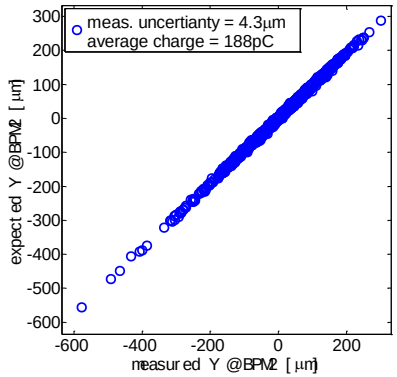
SXFEL

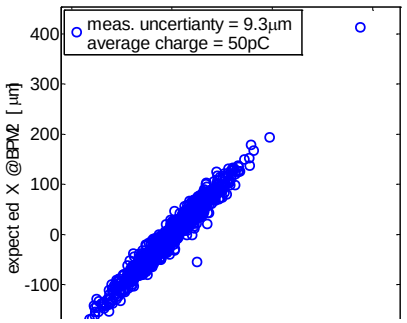


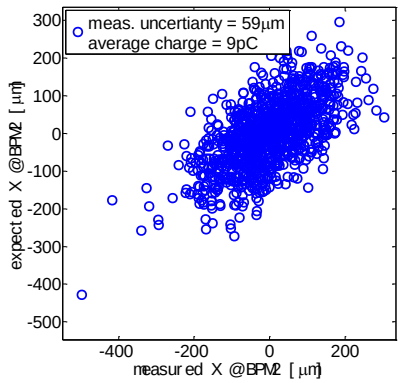
Sirius LINAC

Mass Application on SXFEL/DCLS

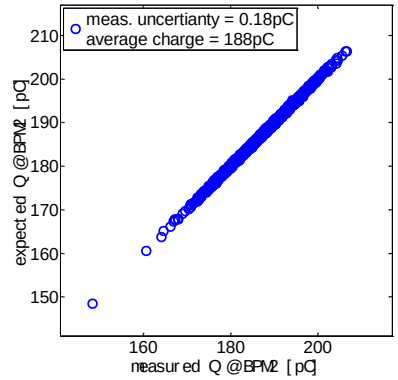
SBPM Evaluation

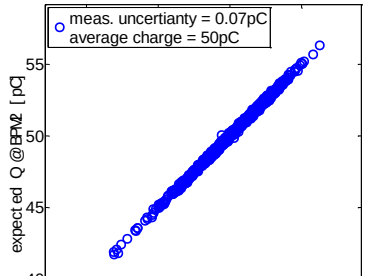


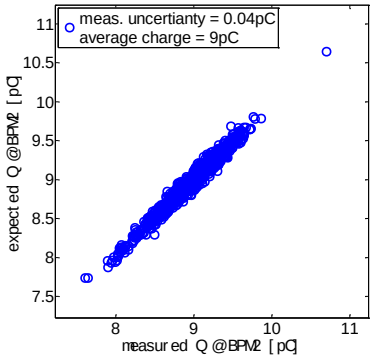




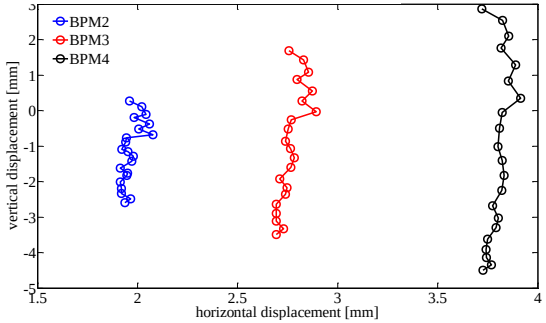
K=5.24, 4.3μm@188pC

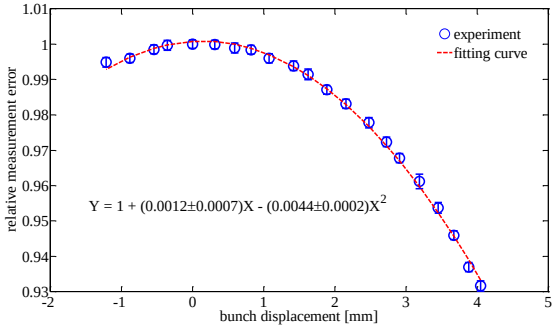






K=5.24, 0.18pC@188pC

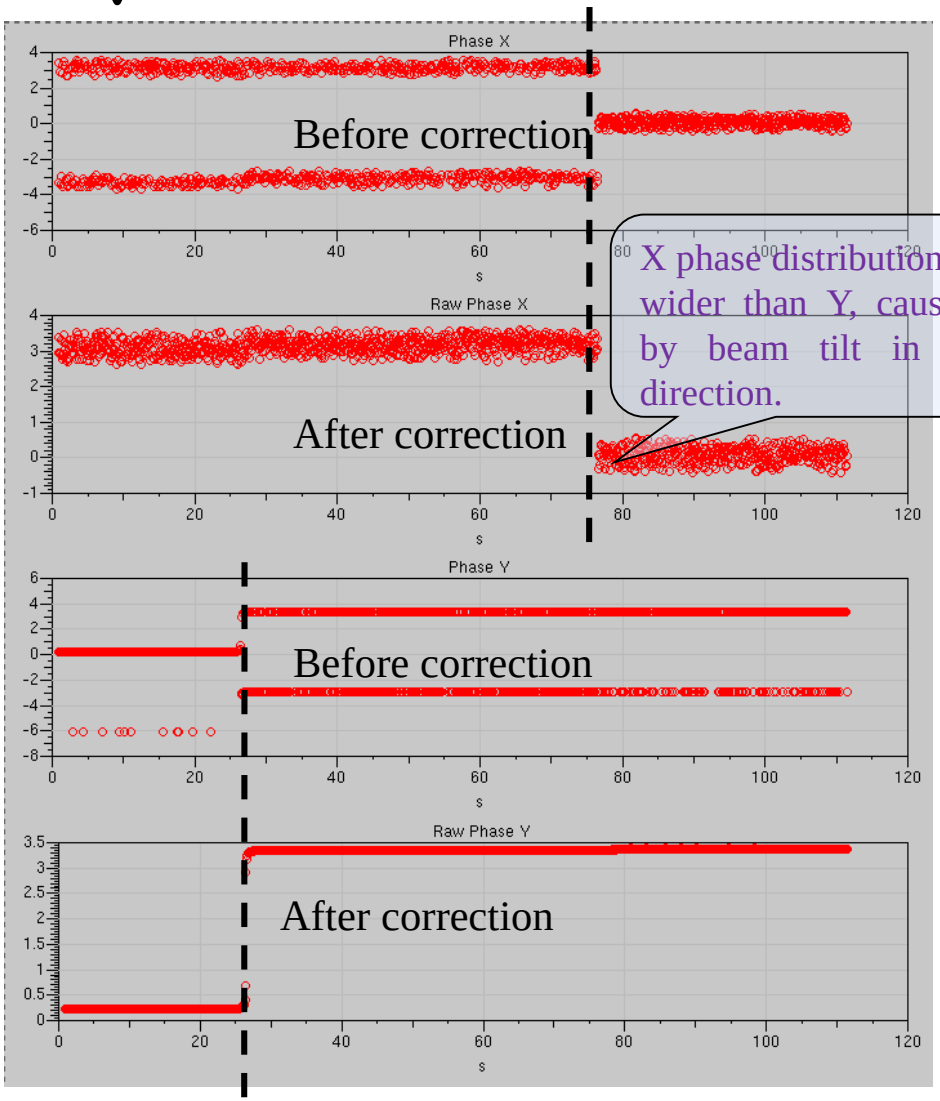




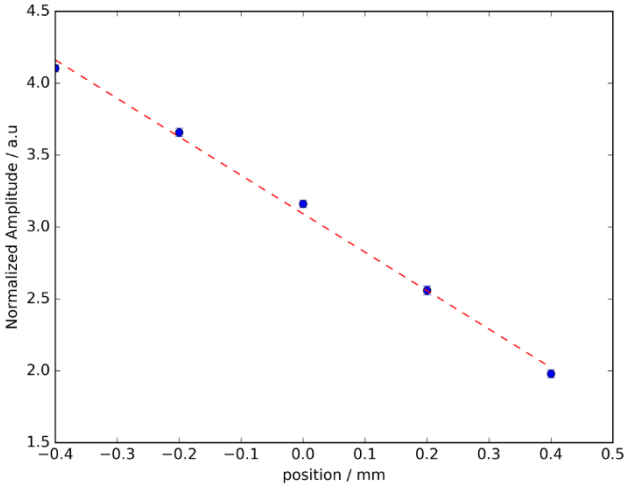
Vertical displacement is getting larger along the beam direction.

Charge measurement accuracy is getting worse when the beam moving from center.

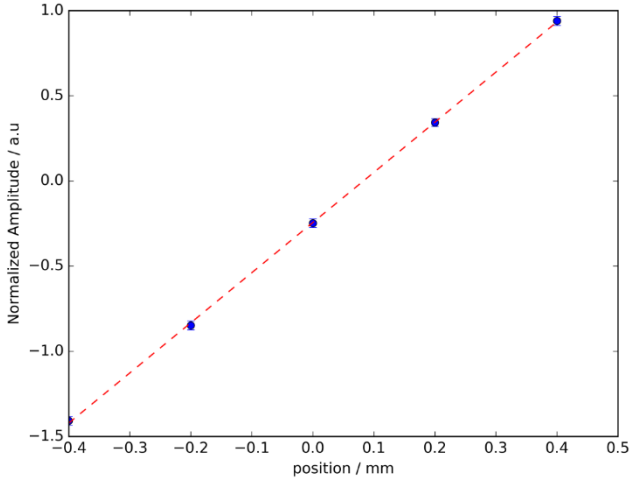
Phase and k Calibration



Phase calibration tests.



Kx = 0.37



Ky = 0.34

K calibration tests.

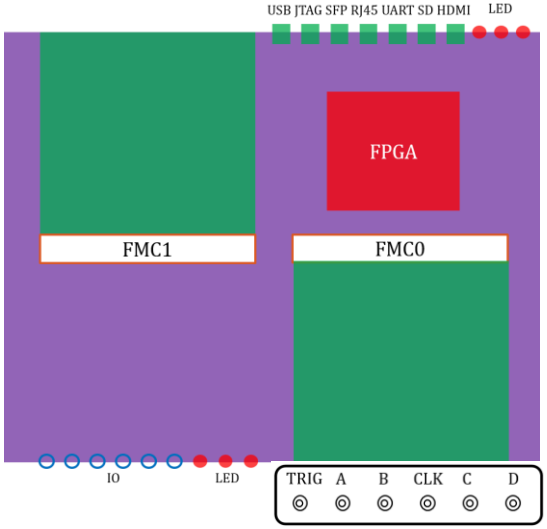
Processor for SHINE

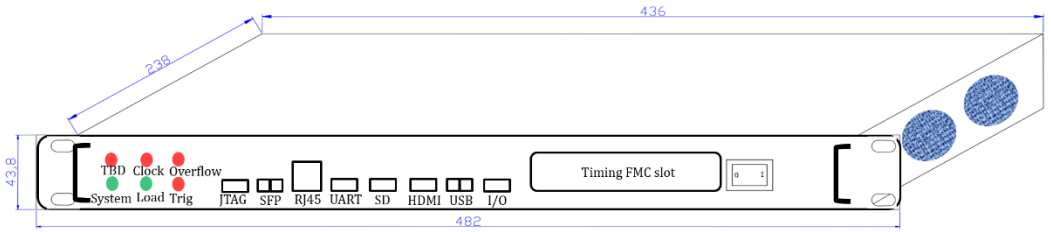
Cold button BPM processor
Stripline BPM processor
Cavity BPM processor
……

- **ADC+FPGA**

Processor Overview

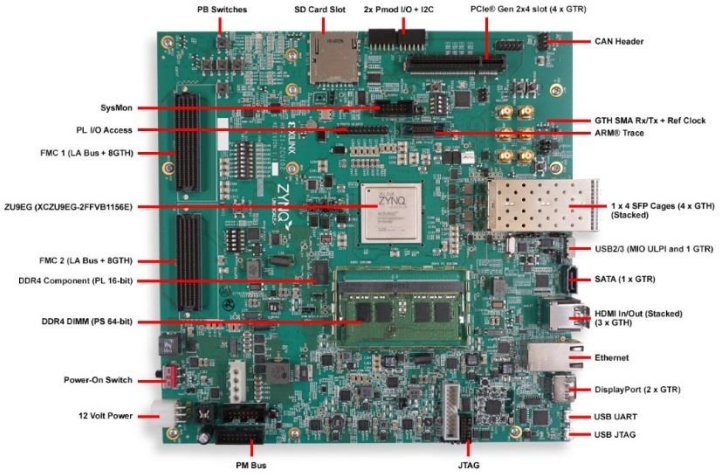
- standalone structure based on Xilinx SOC
- common platform for beam signal processing…
- FMC ADC and timing mezzanine cards
- IF sampling / RF sampling ADC card, 1MHz repetition rate

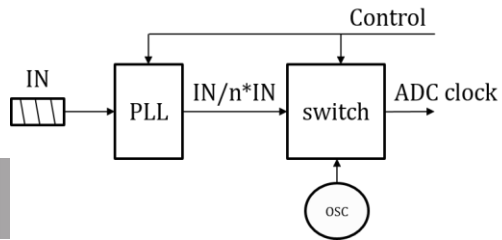


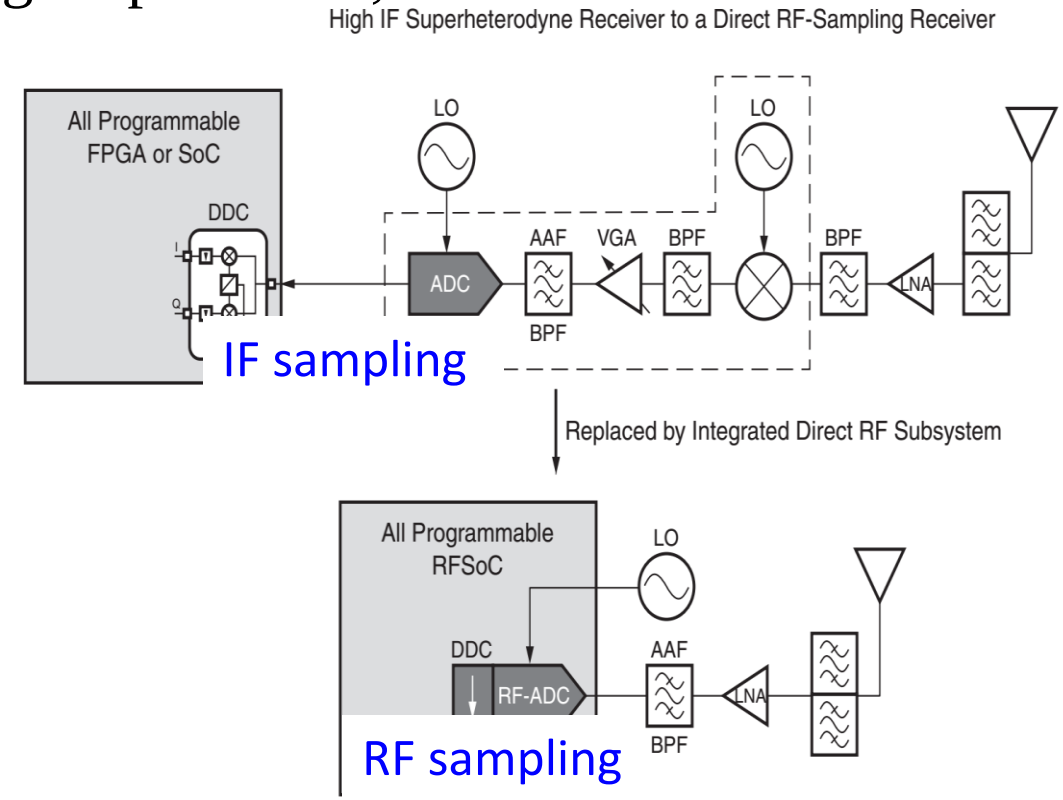


Hardware

- Refer to the design of Xilinx ZCU102 evaluation board
- Zynq Ultrascale SOC FPGA ZU19EG
- ⩾500MSPS, ⩾14bits IF sampling processor(AC&DC), also can be used as BxB processor on synchrotron facility
- RF direct sampling technique (bandwidth >5GHz) is also studied for C band cavity BPM signal processor, ⩾14bits







FPGA

Table 1: **Virtex-5 FPGA Family Members**

Device	Configurable Logic Blocks (CLBs)			DSP48E Slices[2]	Block RAM Blocks			CMTs[4]	PowerPC Processor Blocks	Endpoint Blocks for PCI Express	Ethernet MACs[5]	Max RocketIO Transceivers[6]		Total I/O Banks[8]	Max User I/O[7]
	Array (Row x Col)	Virtex-5 Slices[1]	Max Distributed RAM (Kb)		18 Kb[3]	36 Kb	Max (Kb)					GTP	GTX		
XC5VSX50T	120 x 34	8,160	780	288	264	132	4,752	6	N/A	1	4	12	N/A	15	480
XC5VSX95T	160 x 46	14,720	1,520	640	488	244	8,784	6	N/A	1	4	16	N/A	19	640

Zynq UltraScale+ MPSoC: EG Device Feature Summary

Table 13: **Zynq UltraScale+ MPSoC: EG Device Feature Summary**

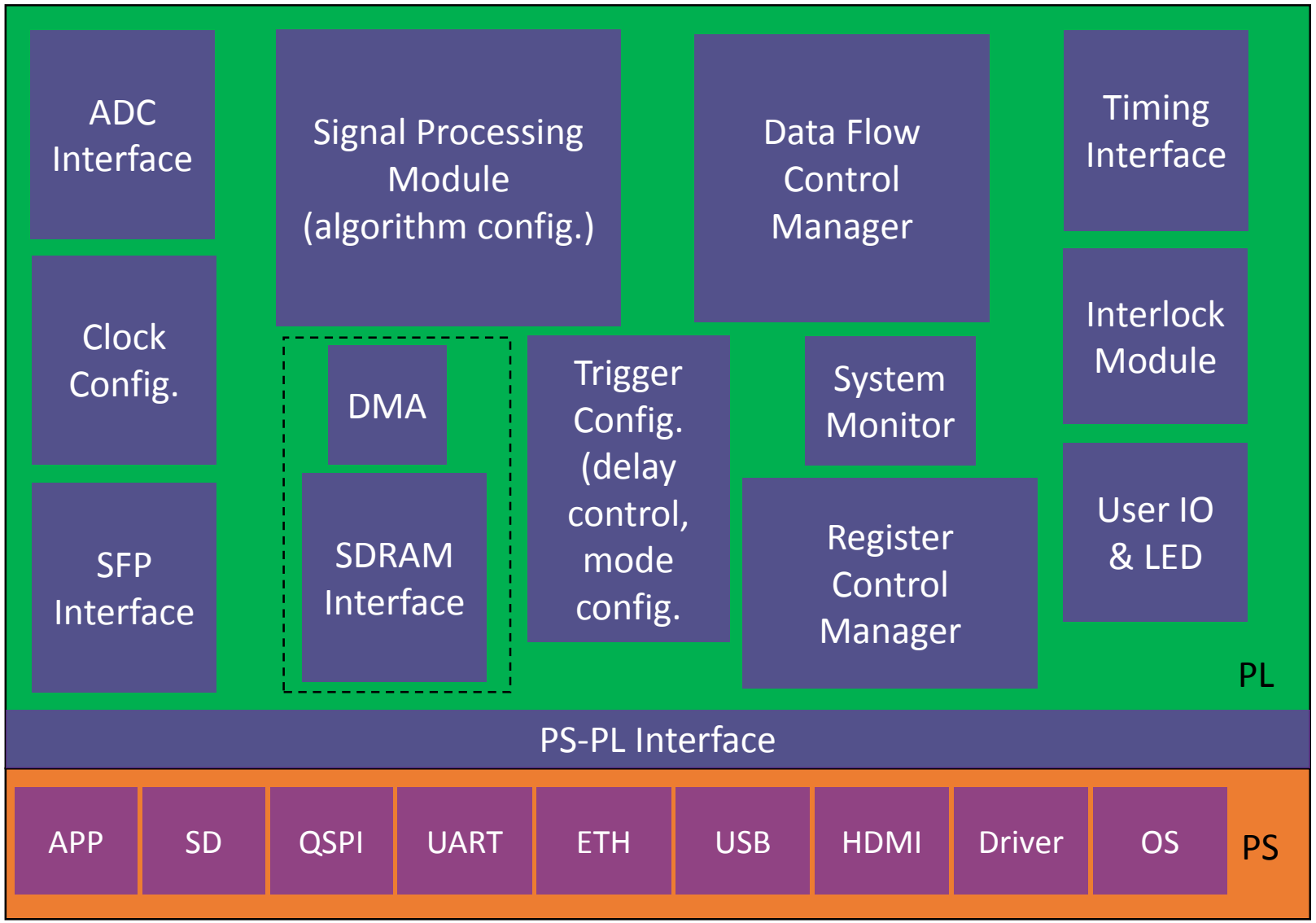
	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit	Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters										
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII										
Graphic Processing Unit	Arm Mali-400 MP2; 64KB L2 Cache										
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550	653,100	746,550	926,194	1,143,450
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
Block RAM Blocks	150	216	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	13.5	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	4	4	4	8	4	8	4	11	11
Max. HP I/O[1]	156	156	156	156	208	416	208	416	208	572	572
Max. HD I/O[2]	96	96	96	96	120	48	120	96	120	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s[3]	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 14.

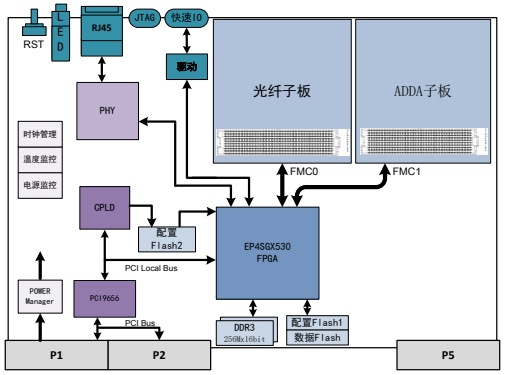
ZU19EG VS. XC5VSX50T

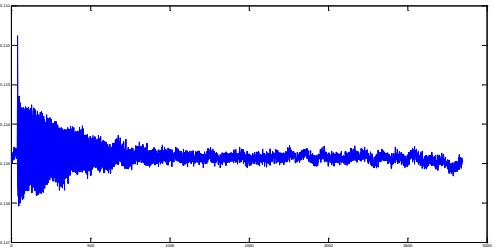
- ⩾ **16** times LUTs
- **6.8** times DSP
- **7.28** times block RAM
- **1.4** times user I/O
- **Quad-core Arm**

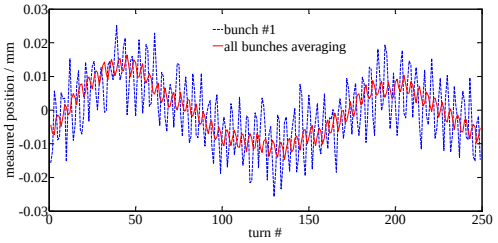
FPGA design overview



BxB DBPM / PT Acc. DBPM / TBF Processor

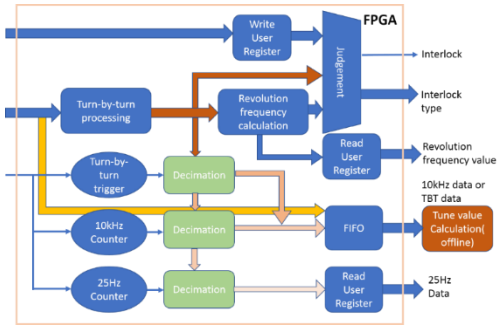




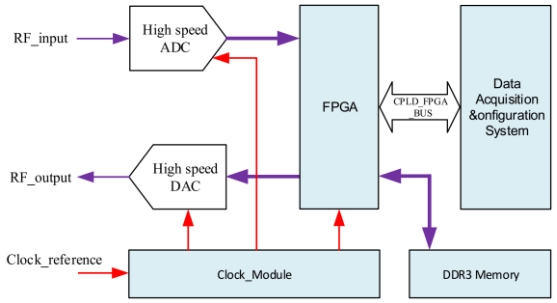


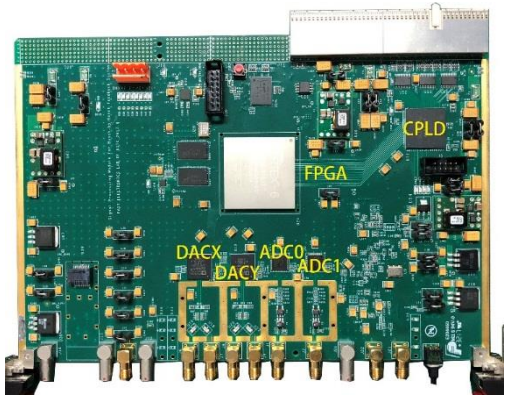
500M bunch-by-bunch BPM processor
Tested on SSRF.

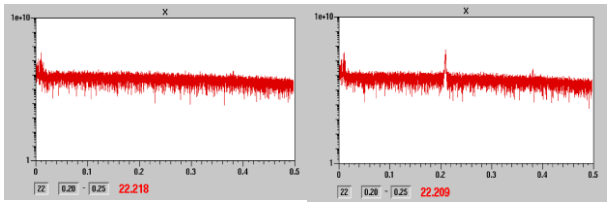
SP Device PXI board.



BPM Processor on Proton Therapy Accelerator.
On-line.







Bunch-by-bunch transverse feedback processor.
Tested on SSRF.

Facility	Number
Brazil Sirius LINAC	2+
DCLS	19+
SXFEL test facility	60
SXFEL user facility	50
SSRF	10+
SHINE	300+

Thanks for your attention