The design of Bunch-by-bunch BPM

Jianshe Cao, Xinger Zhang

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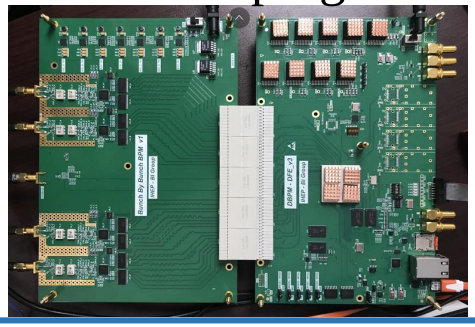
requirements

1、Beam diagnostics :Self-developed BPM – BBB_board to replace the commercial board – Beecube on BEPCII.

Beecube
（Commercial board ）

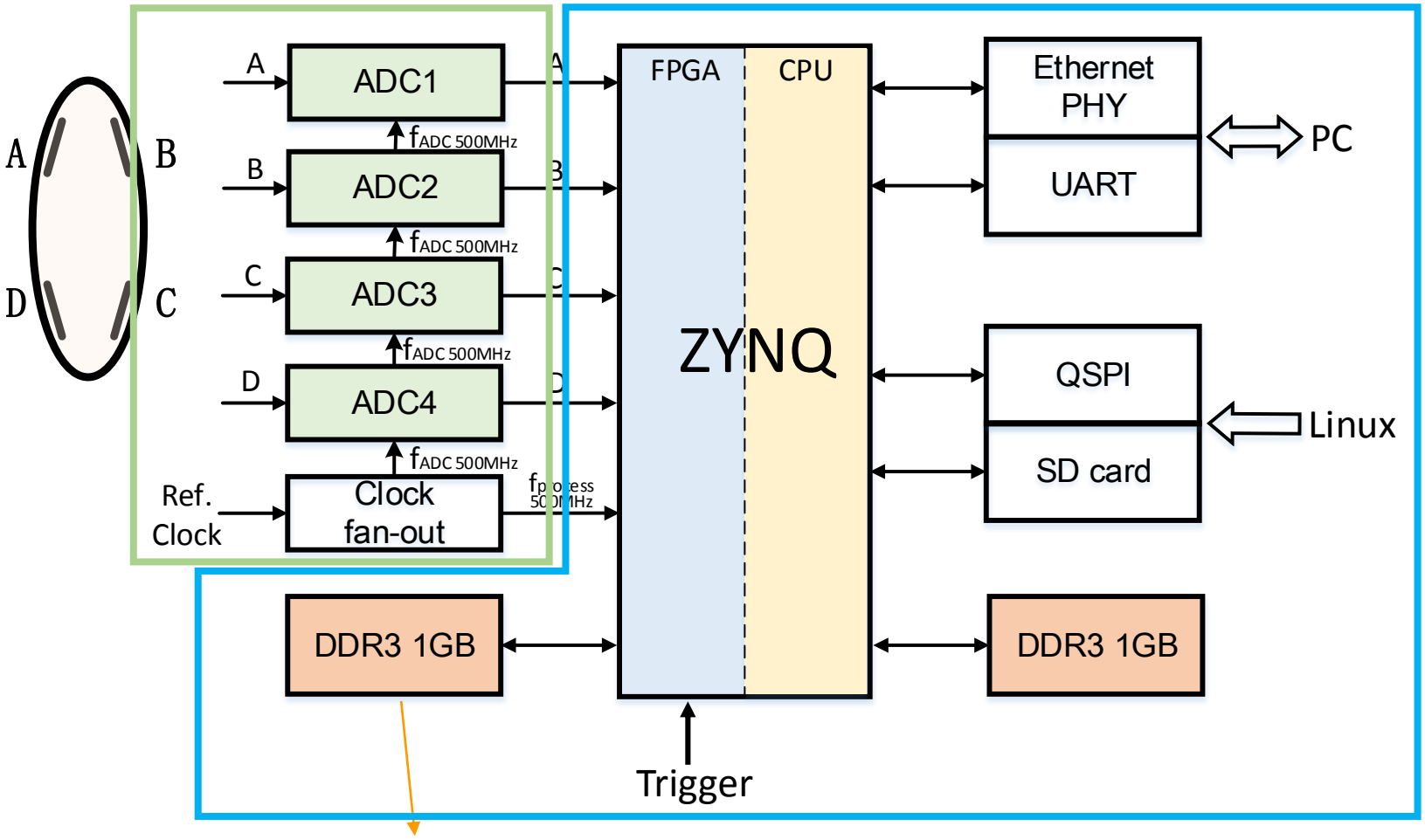
BBB_board
（self developing board）



2、Technical reserve for bunch-by-bunch BPM research of HEPS (High Energy Photon Source)

2 Hardware of bunch-by-bunch BPM

Function Block



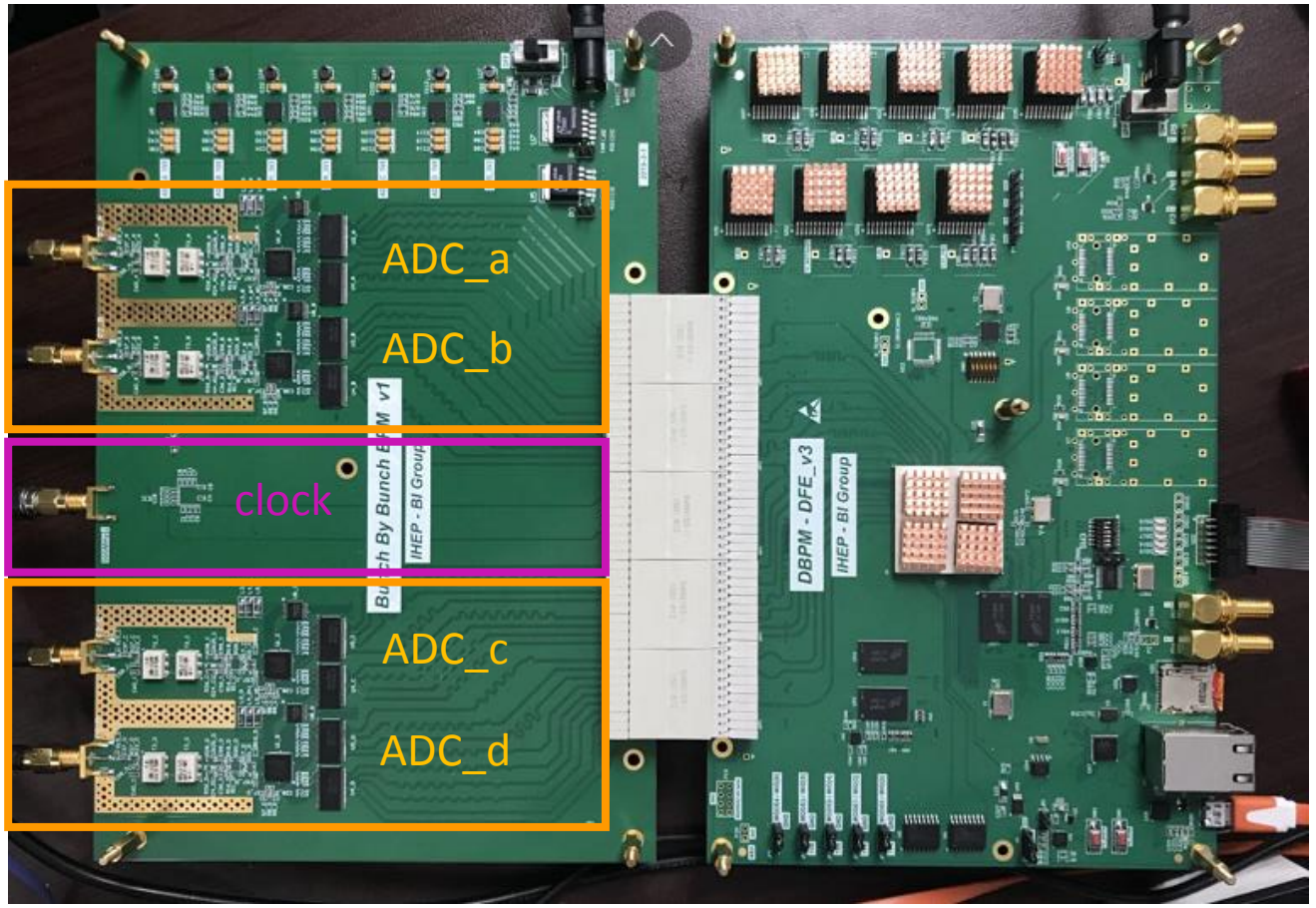
Buffer of bunch by bunch raw ADC data

Hardware

ADC : 500Msps - 12bits, AC coupled

Sampling clock: 500MHz,free running clock or externally clock locked with beam signal

AFE



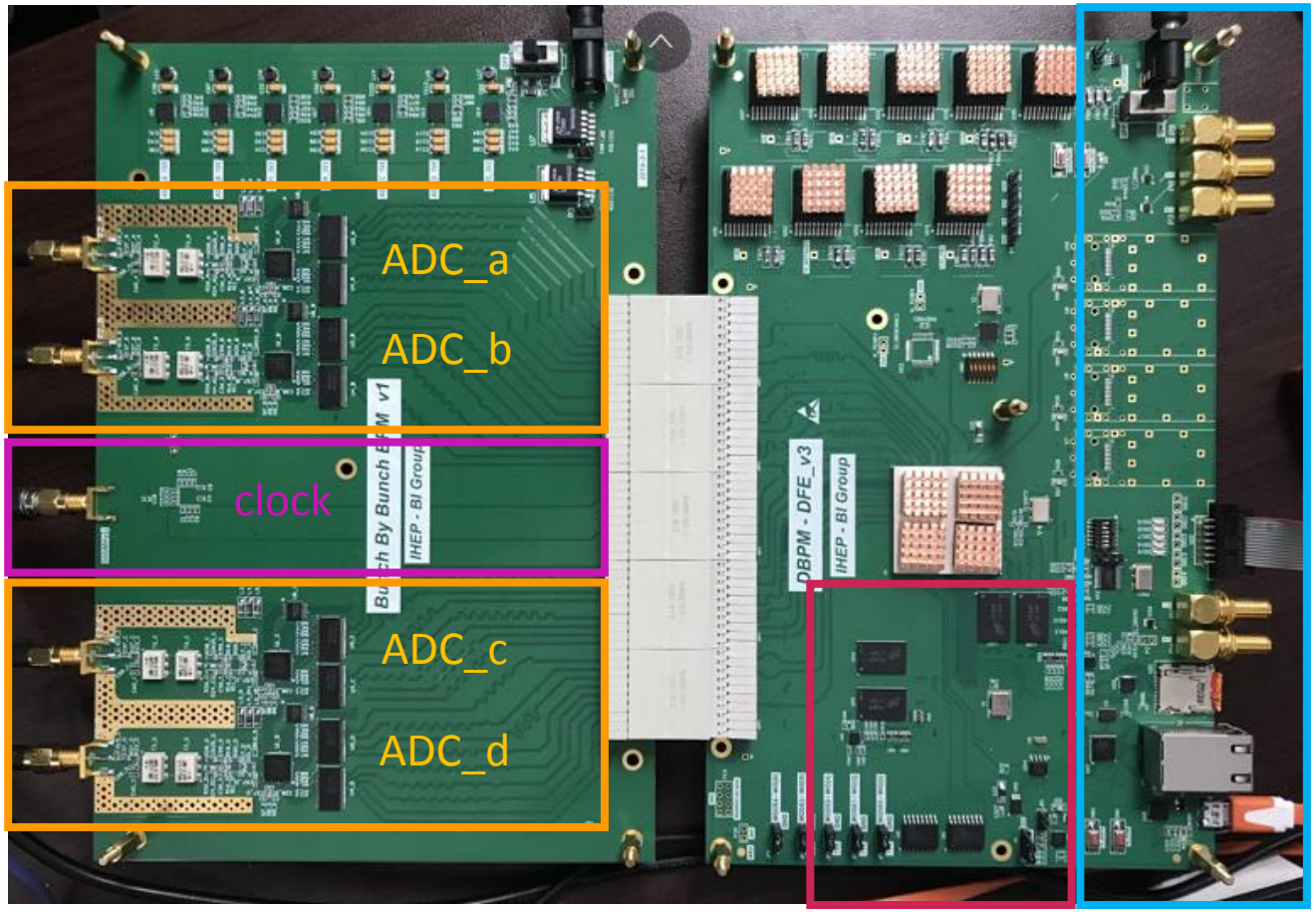
DFE

Hardware

Interface: SMA, Ethernet, UART, JTAG, SFP

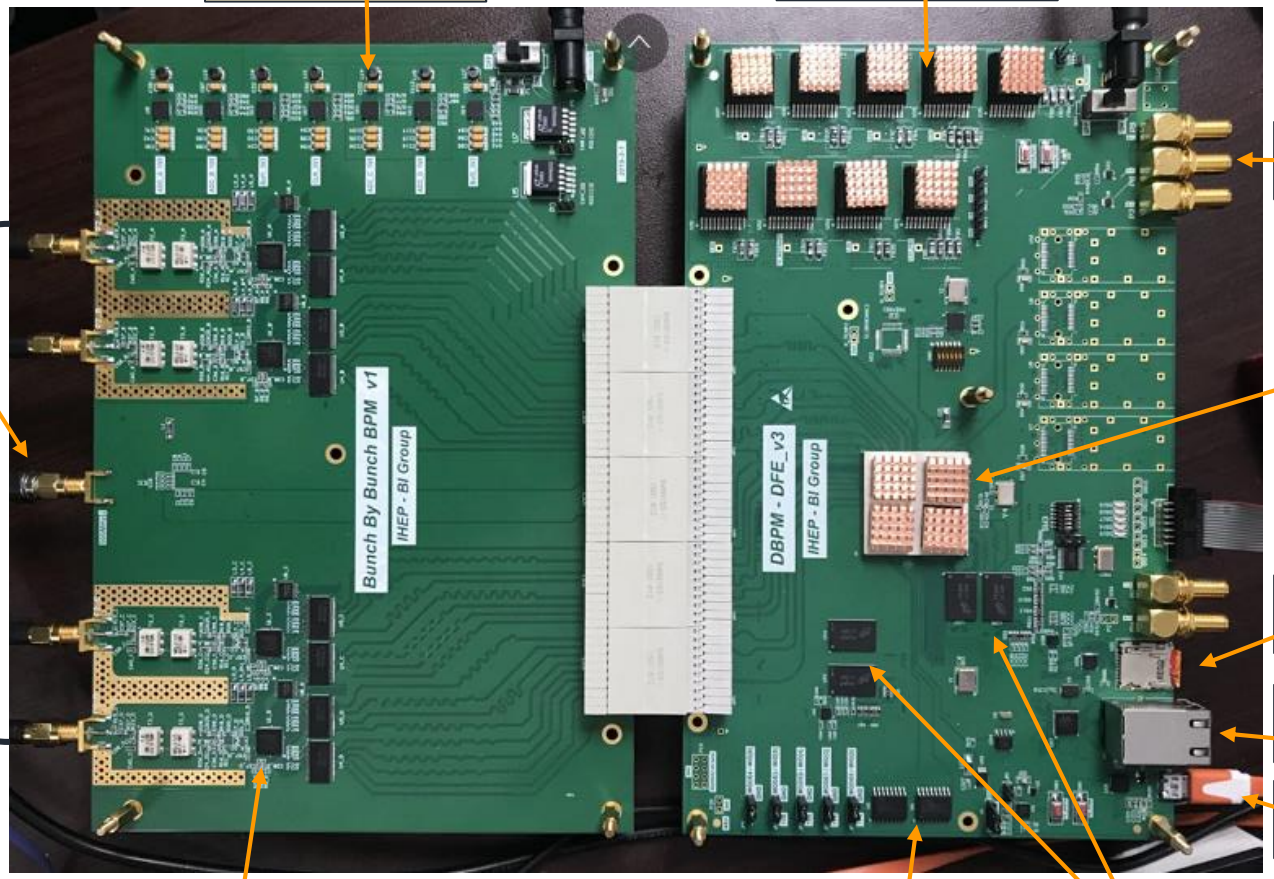
Memory : DDR3_PL, DDR3_PS, QSPI_flash, SD_card

AFE

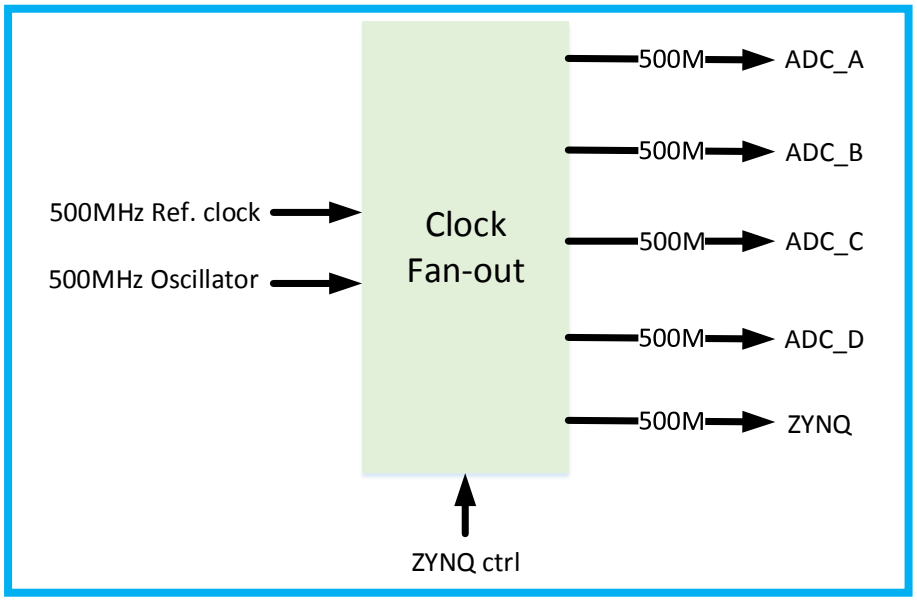


DFE

Hardware


POWER
POWER
clock signal inputs
BPM signal inputs
trigger
ZYNQ
SD card
Ethernet
uart
ADC
QSPI flash
DDR3 (PL &PS)
Bunch By Bunch BPM v1
IHEP - BI Group
DBPM - DFE_v3
IHEP - BI Group

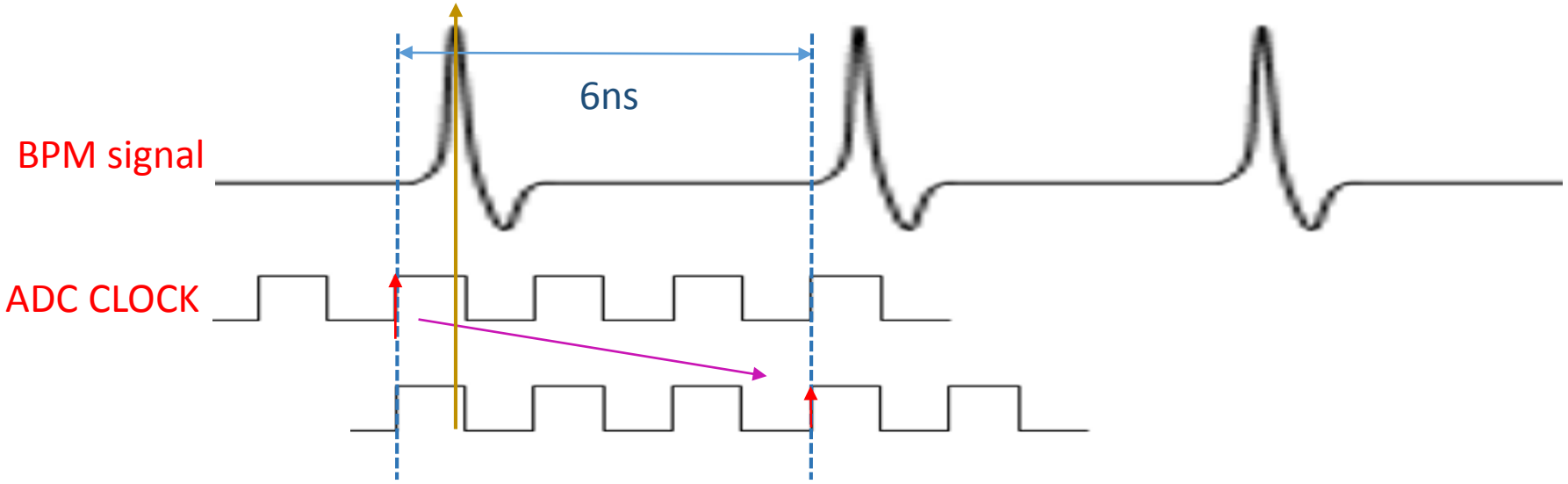
ADC CLOCK



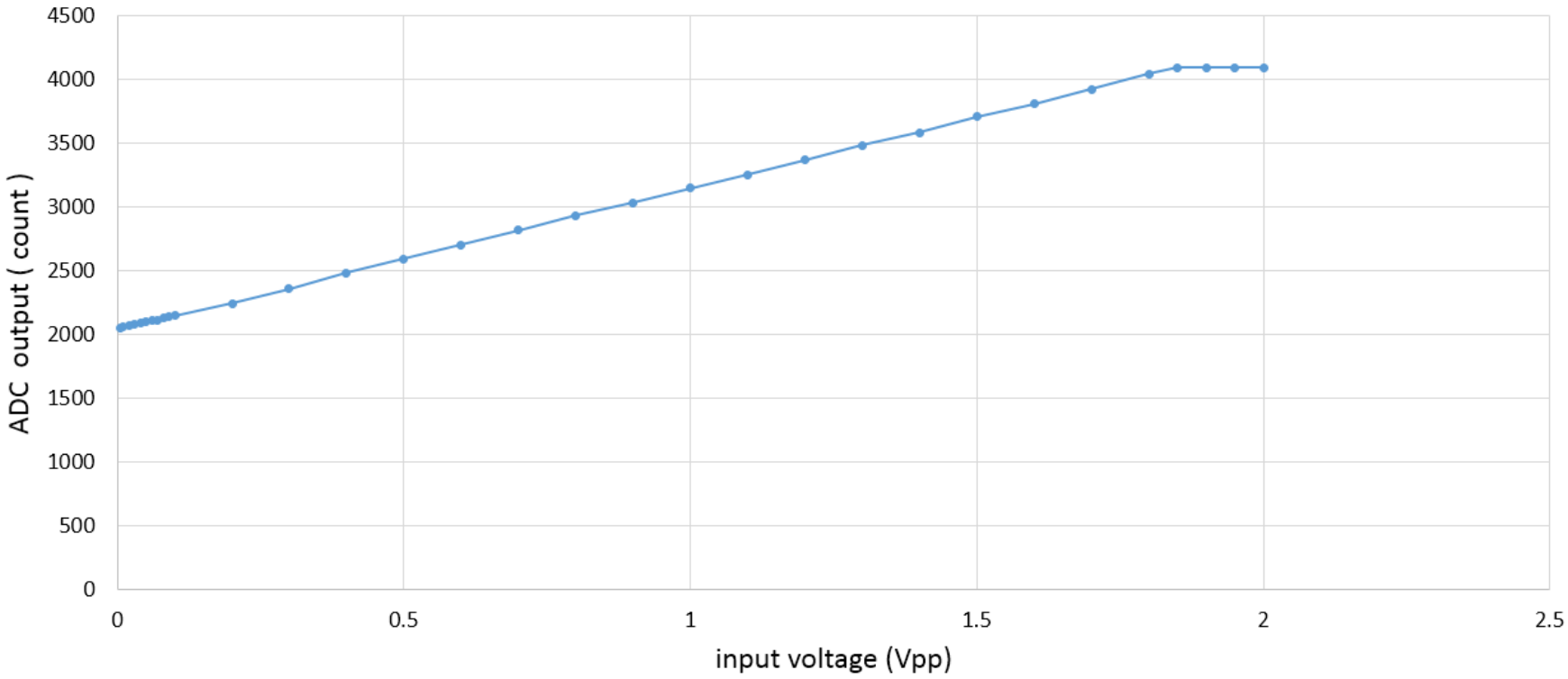
Clock chip Jitter： 100fs

Each clock output delay:
150ps step size ,
range from 0 to 2250ps

Automatic find the peak value of BPM signal， No need to use a phase shifter



ADC signal linearity



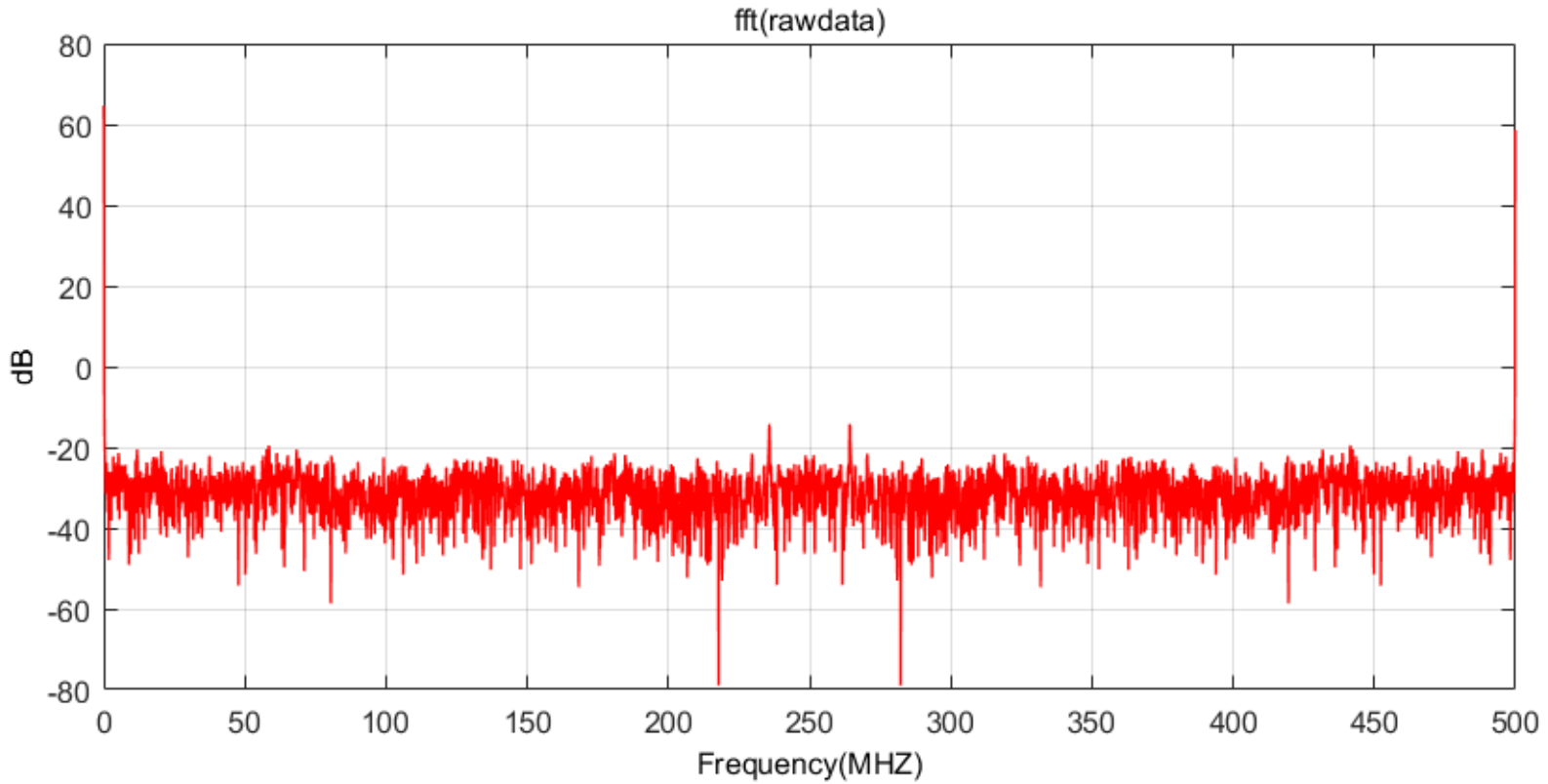
Input signal ：500MHz sine wave

Offset count : 2048 （offset binary 1000_0000_0000）

ADC linear range : 5mVpp to 1.8Vpp

-33dbm to 18dbm

SNR



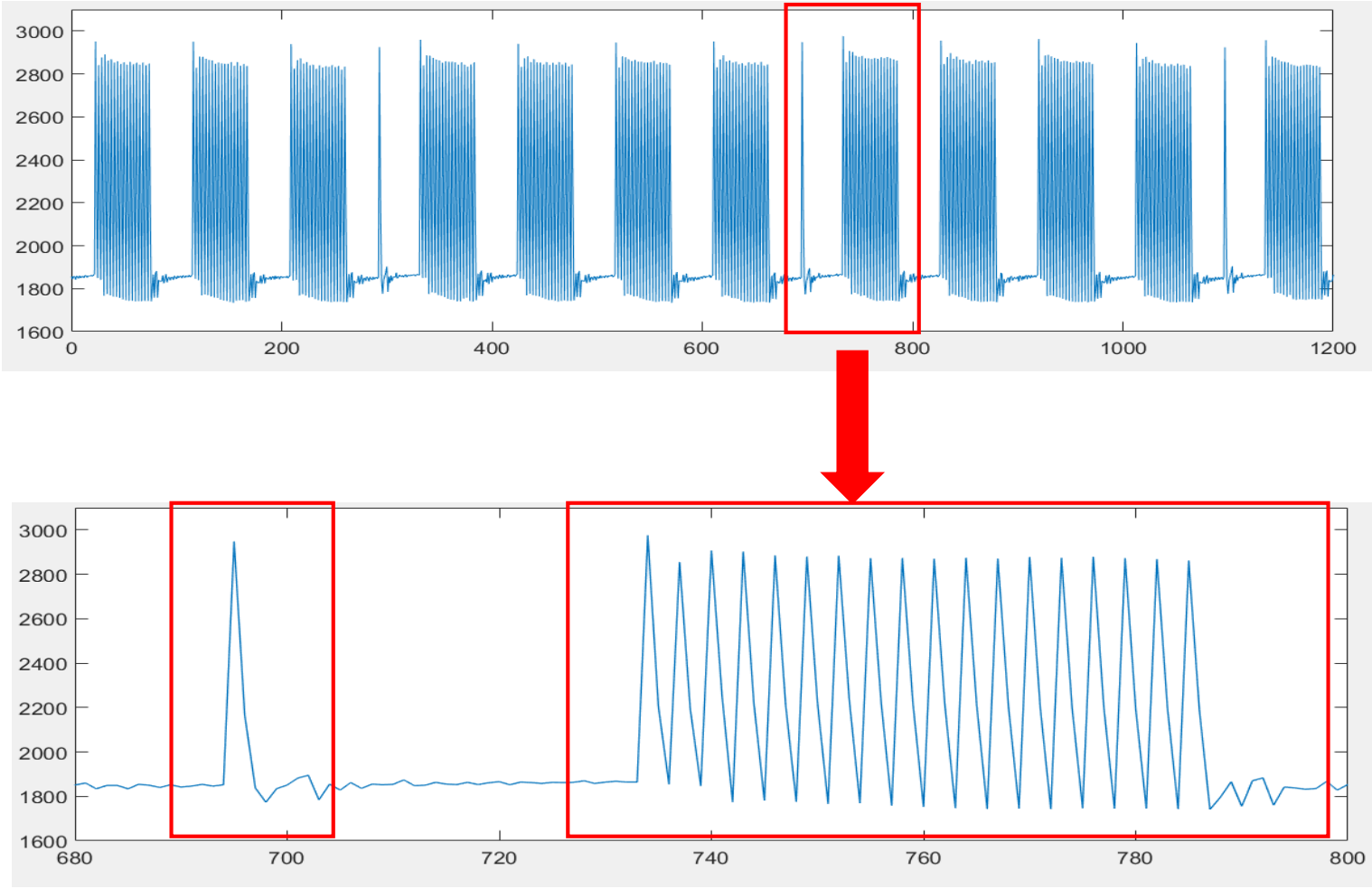
SNR : 68dB

Input signal: 500MHz， 13dbm

Terminated inputs: @50ohm

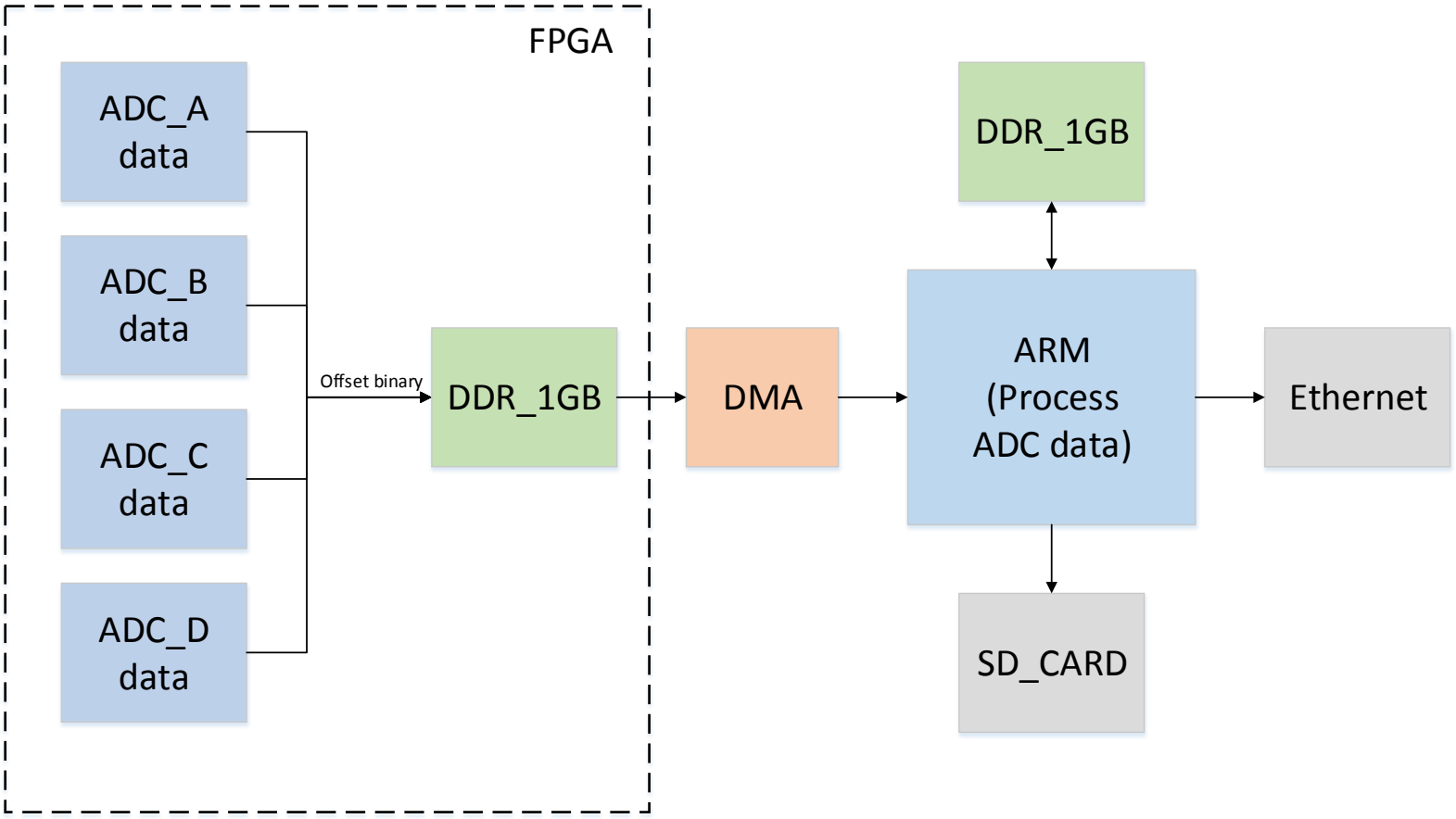
raw_ADC data

Input: simulation pattern of BEPCII , repetition period 6ns

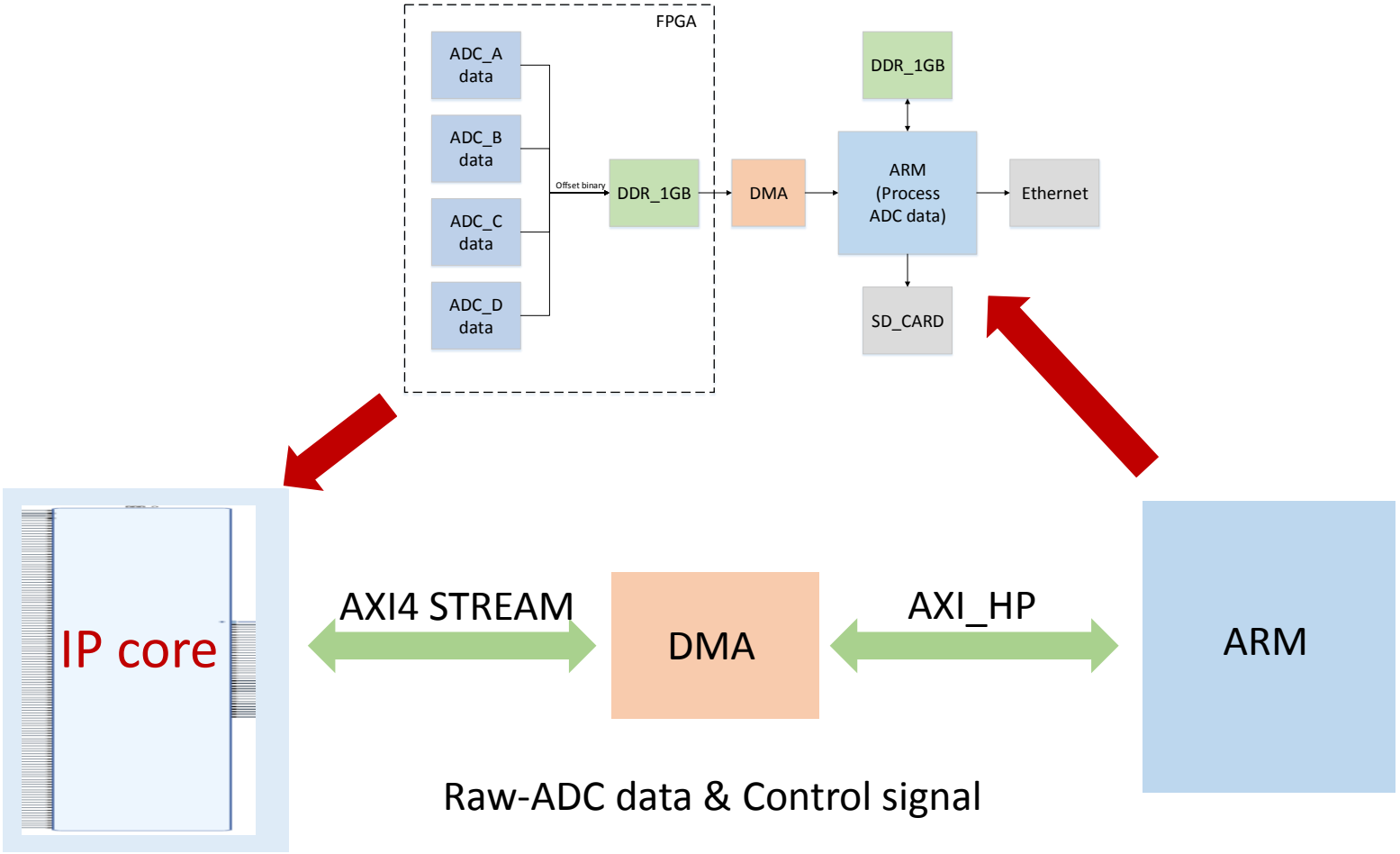


3 data acquisition

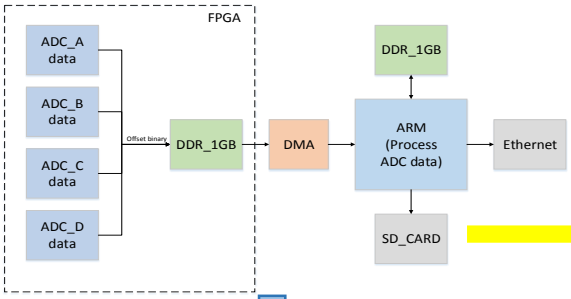
Data acquisition

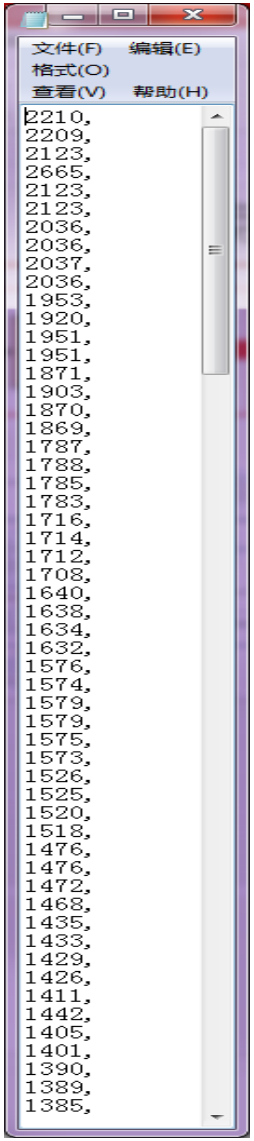


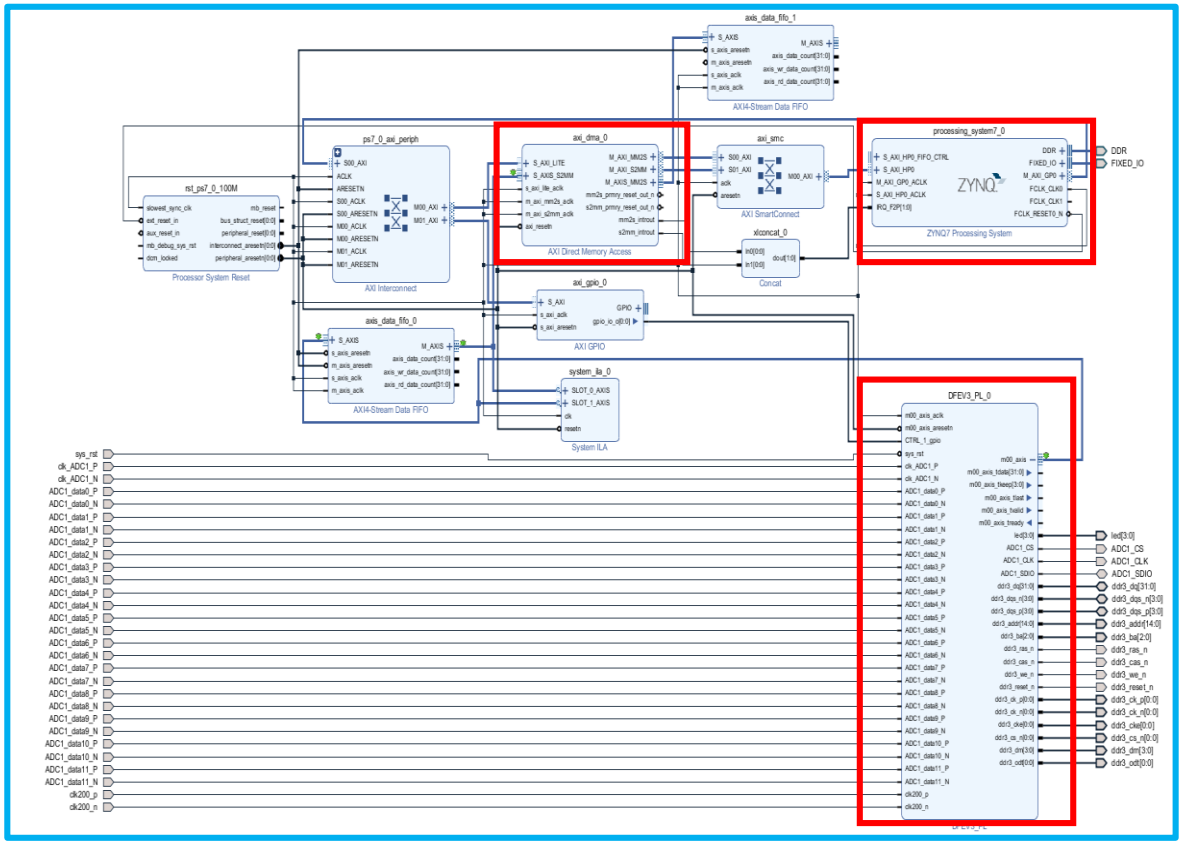
Data acquisition



Data acquisition



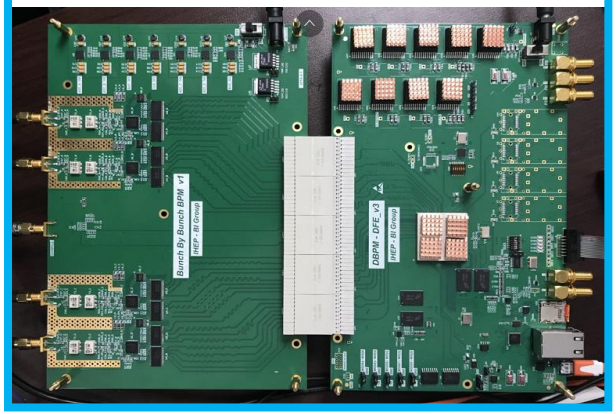




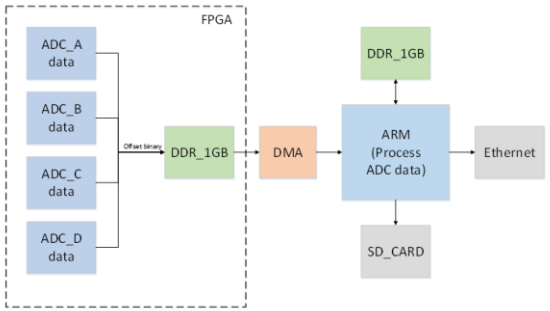
4 next step

Software of Beam diagnostics

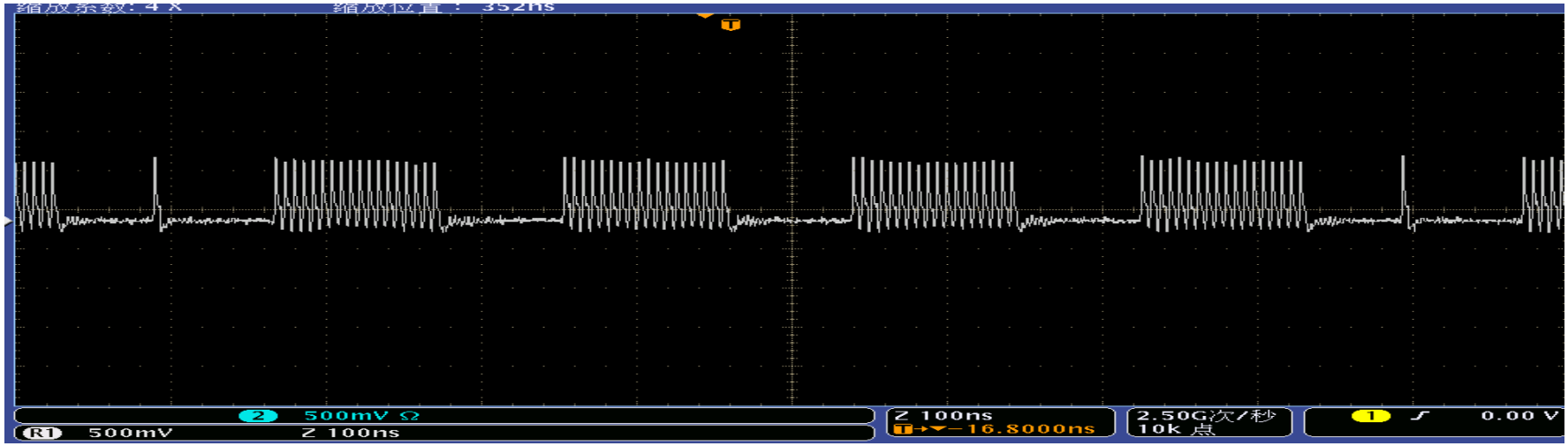
hardware



firmware



Thanks

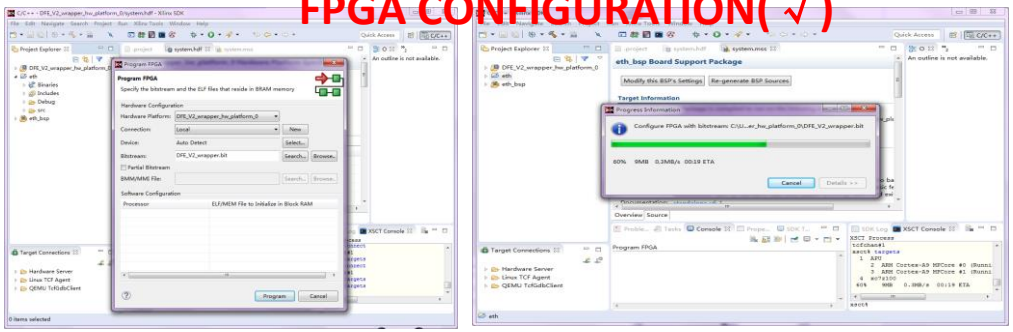

缩放系数: 4 x
缩放位置: 352ns
2 500mV Ω
R1 500mV
Z 100ns
Z 100ns
T→ -16.8000ns
2.50G次/秒
10k 点
1
0.00 V

DFE test

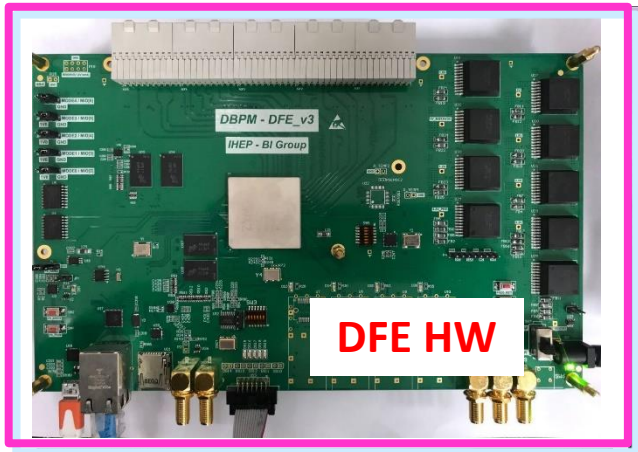
DFE POWER(√)

设计电压（V）	实测电压（V）	用电引脚
1	1.006	VCCINT, VCCPINT, VCCBRAM, ETH,
1	1.003	MGTAVCC
1.2	1.213	GTX_MGTAVTT
1.5	1.494	VCCO, DDR3
1.8	1.780	VCCPAUX, VCCPLL, VCCOMIO, VCCAUX, MGTAVCCAUX, UART, SD, I2C
2	1.998	VCCAUX_IO
2.5	2.513	VCCO
3.3	3.315	VCCO, ETH, JTAG, QSPI, POR,
3.3_pre	3.295	1.5V, 1.2V, 1V

FPGA CONFIGURATION(√)

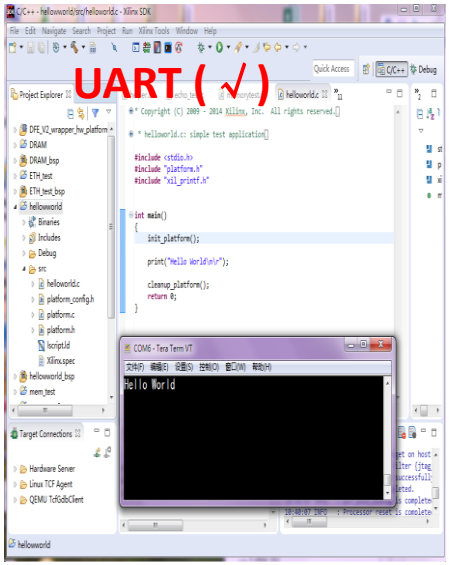


I2C BUS(√)



DDR3 (√)

UART (√)



GbE (√)

LINUX (√)