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The design of bunch-by-bunch beam position monitor

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A bunch-by-bunch beam position monitor is being designed for HEPS. The BPM consists of two parts: Analog Front End (AFE) and Digital Front End (DFE). There are four input ADC channels at 500MS/s,12bit and an adjustable phase clock fanout circuit at AFE. The sampling clock could be free running clock or externally clock locked with beam signal. DFE is designed with the high-performance FPGA/CPU ZYNQ 7100, four-channel raw-ADC data of beam signal can be processed here. The design of hardware has been completed, and bunch-by-bunch raw-ADC data is acquired.
Keywords: bunch by bunch, BPM ,FPGA ,HEPS

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