# Beam diagnostics for fourth generation Russian light source. Concept of the high performance beam position monitoring system.

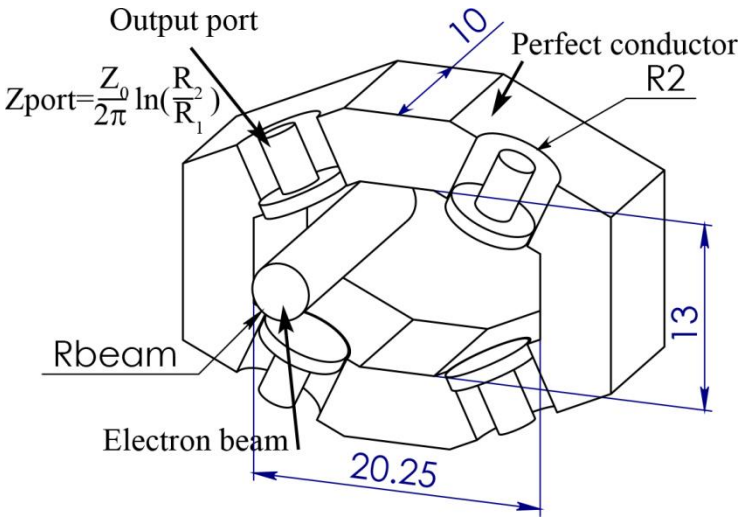
D. Liakin, S. Barabin, A. Orlov, T. Kulevoy

В рамках проекта на основании Соглашения о предоставлении субсидии № 14.616.21.0088 от 24 ноября 2017 г. (Уникальный идентификатор соглашения RFMEFI61617X0088)

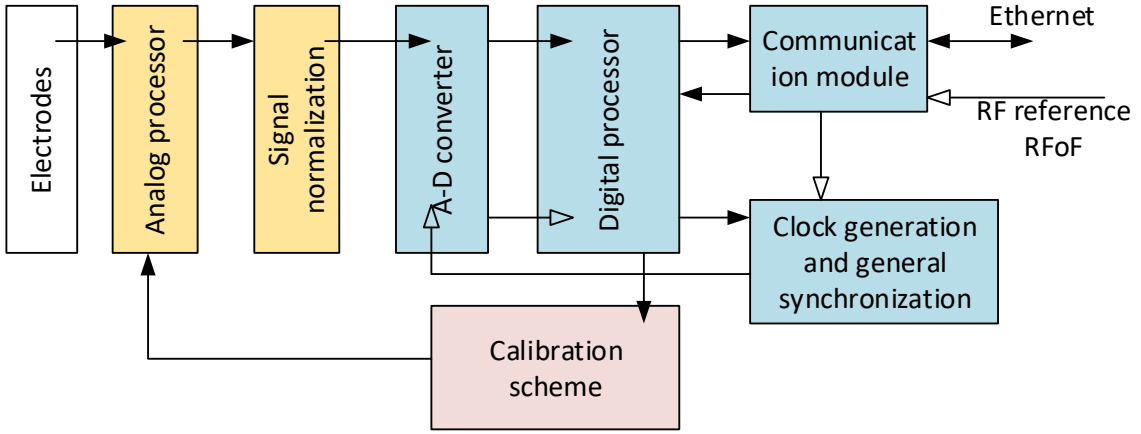
# The BPM for fourth generation synchrotron

This means:

- High accuracy absolute positioning.
- Bunch-by-bunch operation.
- Turn by turn mode for each bunch in the train.
- Acceptable accuracy for the first turn operation mode.
- Enlarging of the amount of the collected data.
- As a result, extensive data processing in front-end modules is required.



# The BPM for fourth generation synchrotron



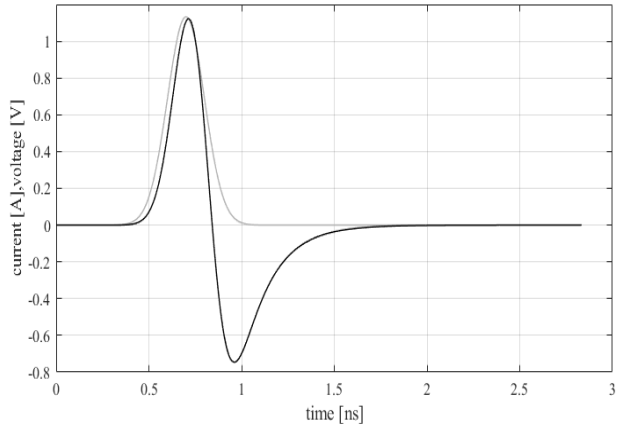

The design concerns:

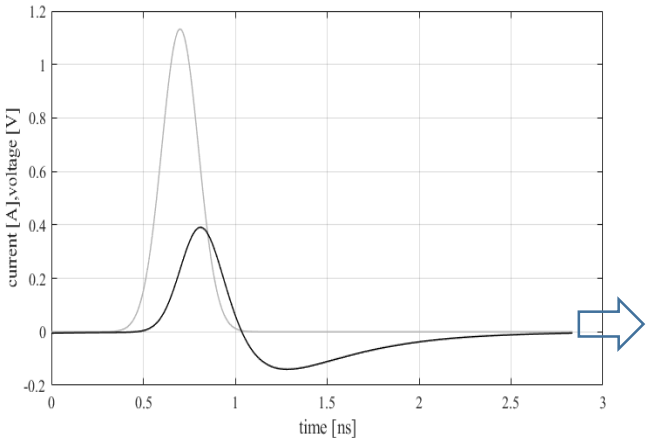
- Electrodes and cable system.
- Analog system processing.
- Digital signal processor.
- Some options like calibration or compensation schemes.
- System integration. Data net and synchronization devices.
- Coherent data processing and feedbacks.

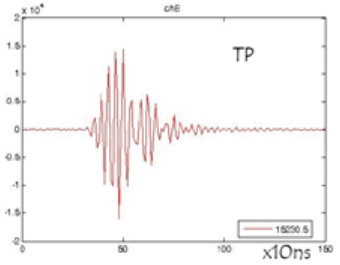
# Clear BPM signals is required.

- BPM functionality depends on the budget!
- From functionality point of view an RF sampling (6GSPS) ADC embedded into FPGA package is able to solve most of BPM tasks.
- But such module as well as 14 bit, 3GSPS ADCs probably make the electronic too expensive.
- We could formulate a minimal requirements for electronics. Bunch by bunch operation requires 500 MHz bandwidth to separate adjacent bunches from each other(see figure on the right). It also needs ADC with sampling rate 500 MSPS or higher.
- Affordable solution could be 1.5 GSPS ADC with 2 GHz analog bandwidth.

Fig.1 The pulse of current and the signal at the pick-up RF connector.



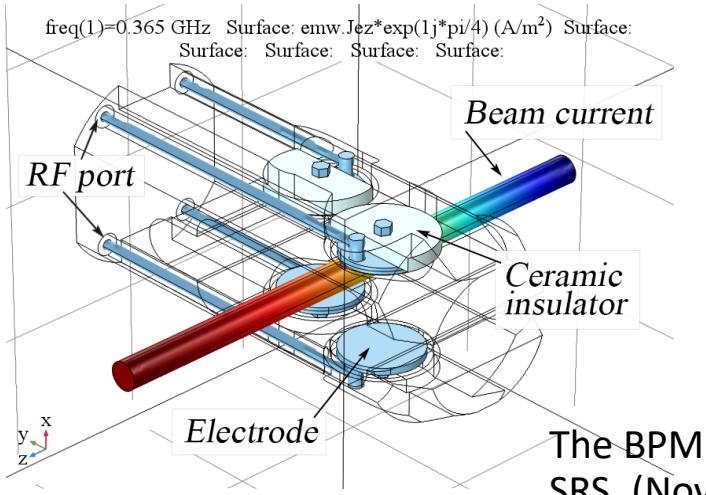




Signal tail covers tens of followed pulses due to the narrow-band filter in Libera

Fig.2 The same signal as on Figure 1 but after a low-pass filter. Small portion of power of the signal leaks to the next bunch. Therefore we demand for processing a frequency band at least 500 MHz

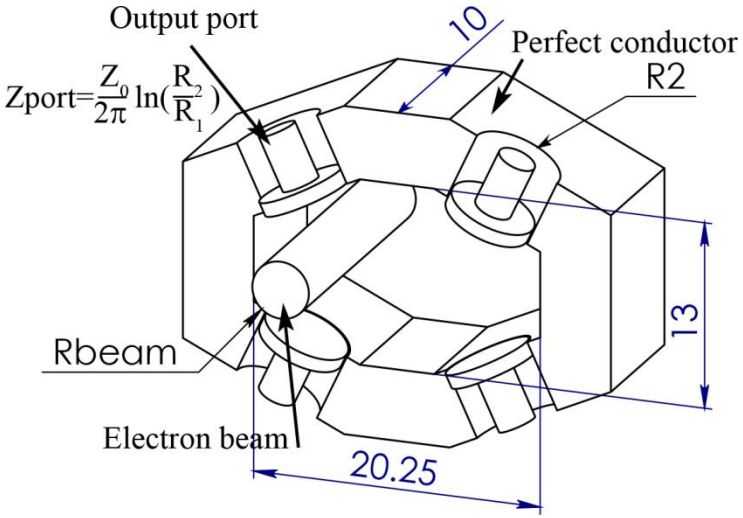
# BPM. BPM electrodes.

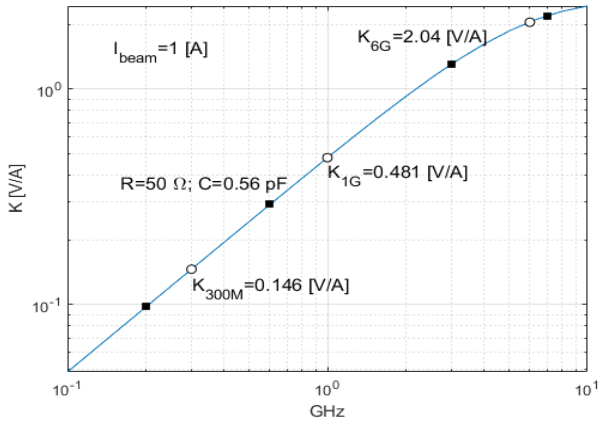
- The common practice is to use a combined signal form ‘45-degree‘ electrodes.
- But there are reasons for separated vertical and horizontal systems of electrodes




The BPM for a 2nd generation SRS. (Novosibitsk,NRC KI,Moscow)

6 mm ESRF-type BPM

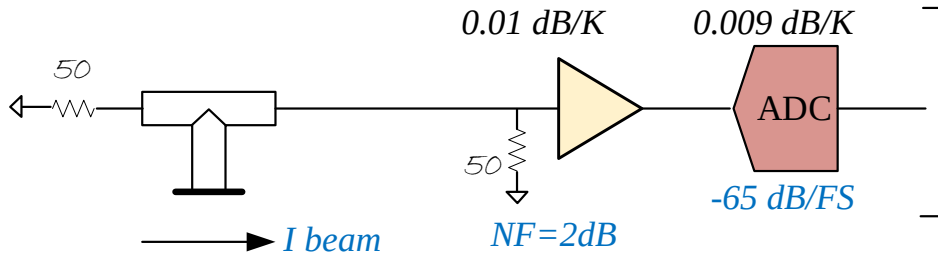



Frequency characteristic of the ESRF-type electrodes. It operates like a first order high-pass filter. Therefore the high-frequency fraction of the beam signal may have better signal-to-noise factor.

# Noise and drift analysis of the analog schemes. In a good design the thermal noise is a main contributor

*5 micrometer accuracy constraints the overall drift of the transmission coefficient with value 0.002 dB(ca. 0.02%)*

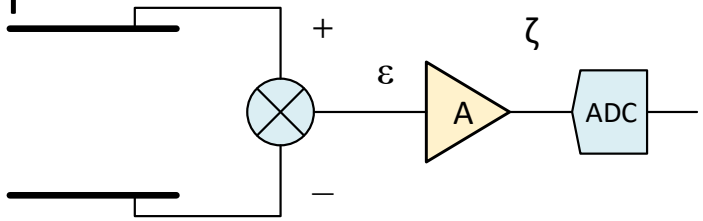



**Drift affects the DC measurements**

**The noise limits the performance of the oscillating processes control**

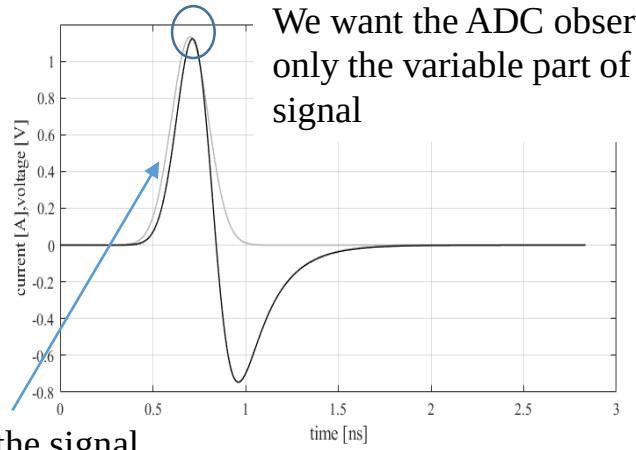
*For the chosen electrodes the thermal noise is equivalent to 0.7 micrometers (rms)in single measurement*

*Without combining of the signals the ADC is dominant noise contributor*

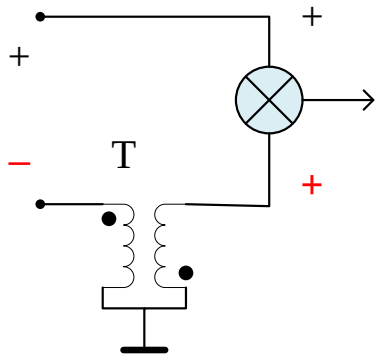



The use of the signal difference could improve the performance of the device reducing both drift and the ADC noise contribution.

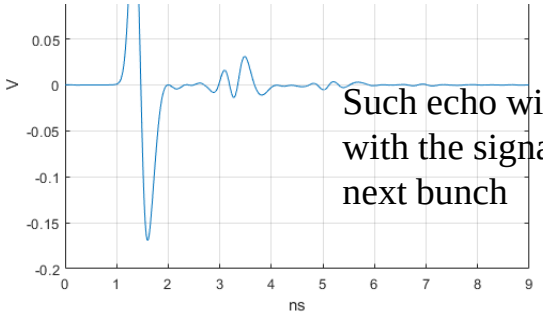
We want the ADC observing only the variable part of the signal




Regular part of the signal wastes the ADC scale



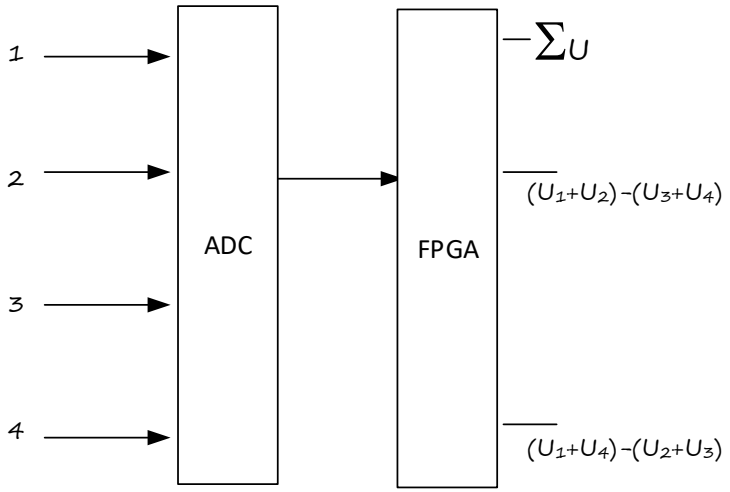

The problem is to get a good signal subtractor with proper frequency and time domain behavior.

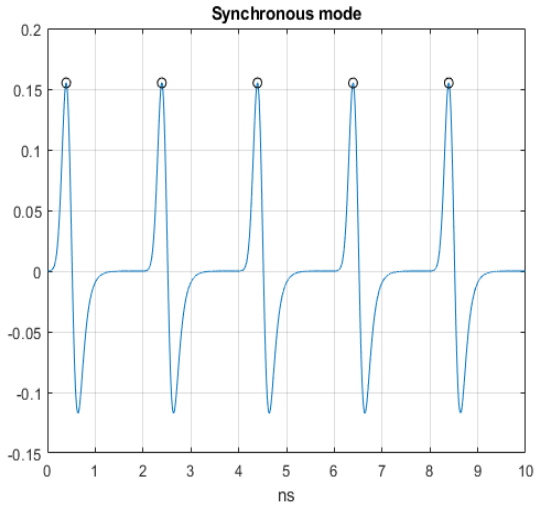



Such echo will interfere with the signal from the next bunch

# The signal digitizing

- Nowadays ADCs allow direct signal sampling up to GHz range. The trend is more digital signal processors replace the analog schemes.
- Also FPGAs provide appropriate interfaces to receive such data rates.
- So typical BPM node looks like it is shown in figure below.

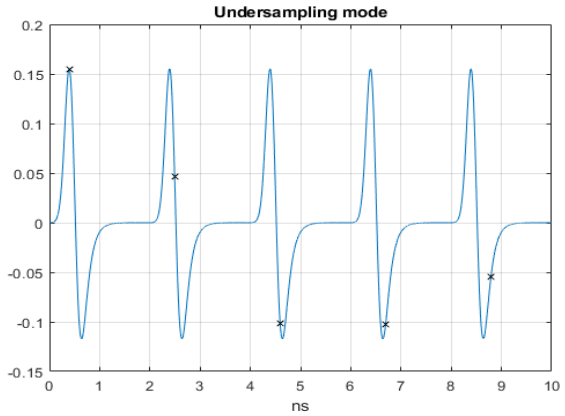



- Synchronous mode uses half of Nyquist sampling rate
- Data is taken at the point with the best signal-to noise ratio
- Data is taken for every bunch on every turn

- We may use an extra knowledge describing the input signals. In general we know the shape (after filtering) of the signal and for reconstruction we only need the magnitude and, probably, the phase of input pulses.

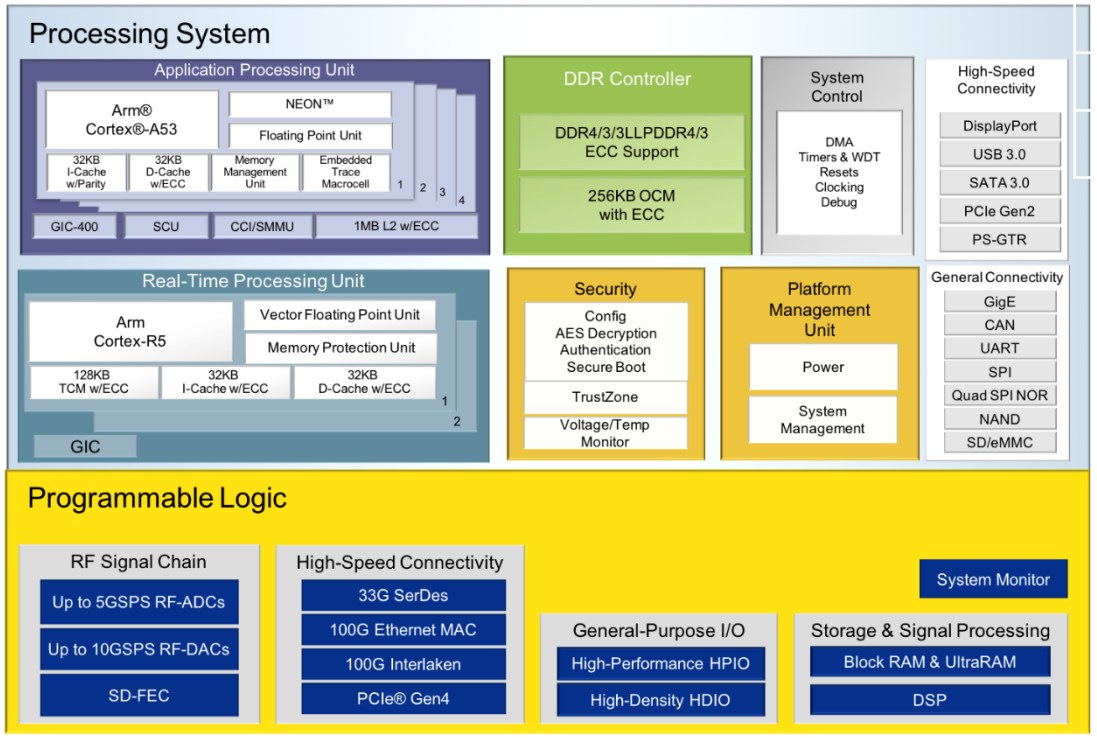
- Undersampling is less efficient but easier to implement



# The signal digitizing

- Many ADC's on the market propose ranges of rates, bandwidth and price.
- Fast ADC requires fast FPGA, so multigigabit SERDES is mandatory.

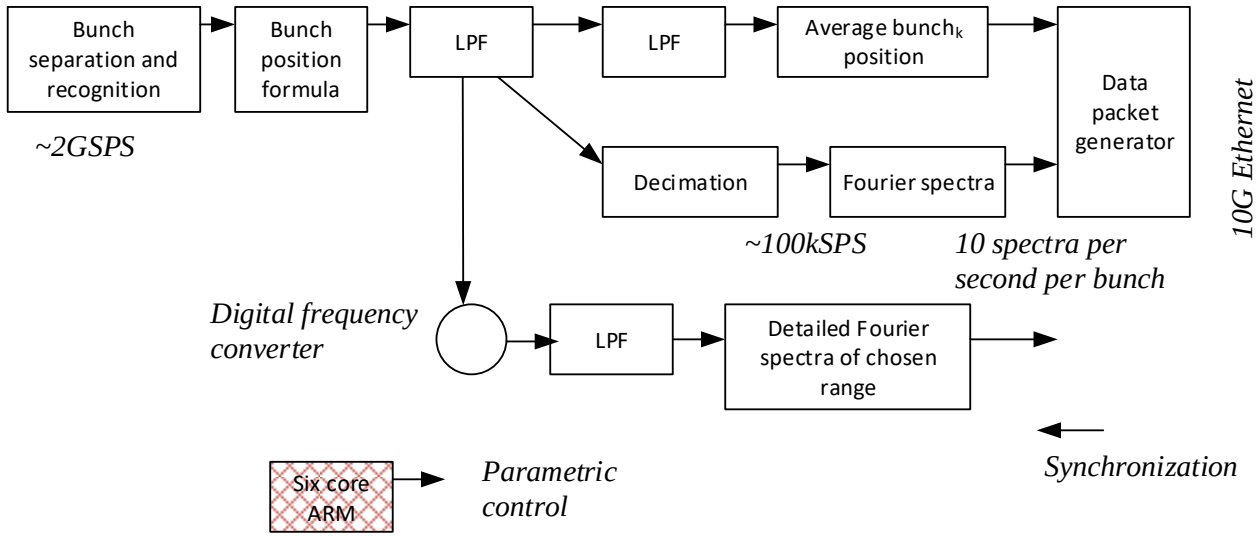
| | Resolution | SNR@30 0 MHz | Rate MSPS | No of channels | Cost per channel | Analog BW |
|---|---|---|---|---|---|---|
| **AD9680** | 14 | 65.3 dB | 820 | 2 | $185 | 2000 |
| **ADS54J20** | 12 | 67 | 1000 | 2 | $195 | 1200 |
| **ADS5400** | 12 | 59 | 1000 | 1 | $1080 | 2100 |
| **AD9208** | 14 | 60.2 | 3000 | 2 | $663 | 9000 |
| **AD9213*** | 12 | | 10000 | 2 | $1700 | 6500 |




- The industry offers also RF systems on chip –RFSoC. Xilinx Zynq Ultrascale+ provides 8 4GSPS ADC, quad core ARM system, FPGA in single package. 100G Ethernet allows the seamless integration of multiple devices into the common address space.

# Front-end signal processing

- Main task of the signal processor is a data reduction.
- Fast Fourier transform is a well known process which used moderate area in the FPGA
- There are no extensive calculation in front-end therefore we reduce requirements to the FPGA complexity
- Bare-metal ARM processors system provides a general parametric control and further more adaptive functions.



# The end. Thank you.