TT-PET project

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- Positron Emission Tomography (PET)
  - Positrons from a radionuclide introduced in a body annihilate with the nearby tissue, emitting two back-to-back photons
  - The photons are detected in coincidence, tracking a line of response (LOR)

- Hybrid PET-MRI Imaging
  - Combining functional Image by PET and morphological image by MRI

(10.2967/jnumed.110.074773)
Time-Of Flight PET

Improved resolution by measurement of difference in arrival time of the two photons.

Goal:
30 ps time resolution for ~mm spatial measurement

- less radio dose to patients
- better spatial resolution
- possible to be inserted in an MRI facility
TOF information improves the signal-to-noise ratio (SNR) of reconstructed images.

\[
\frac{\text{SNR}_{\text{TOF}}}{\text{SNR}_{\text{CONVENTIONAL}}} \sim \sqrt{\frac{D}{\Delta x}}
\]
Depth-of-Interaction (DOI)

- Sensitivity for photon depth of interaction improves the spatial resolution across the whole view of the scanner.
- It also reduces the uncertainty of TOF measurements.
Derenzo phantom GEANT4 simulation

TT-PET simulation

no – TOF information

TOF information

0.7 mm
1 mm
0.5 mm
1.2 mm
1.5 mm
2 mm
The TT-PET project: a 30 ps Time-of-Flight PET scanner with silicon

In collaboration with:

- Roberto Cardarelli - INFN Roma Tor Vergata
- Craig Levin - Stanford University
- Marzio Nessi - CERN IdeaSquare
- IHP microelectronics
TT-PET

✓ Fully financed by a SWISS research grant (>2MCH)
✓ First demonstrator phase will end in spring 2019
✓ A new proposal for a full device construction has been submitted to the Swiss grant system
✓ Very interesting THz electronics technology

THE TT-PET PROJECT

The Thin Time-Of-Flight Positron Emission Tomography (TT-PET) project (SNSF grant CRSII2_160808) aims at developing a pre-clinical TOF-PET scanner with very precise 3D spatial reconstruction, for ultimate use in an MRI scanner. The 3D measurement will be achieved by TOF measurement with 30ps time resolution, obtained by monolithic pixel silicon sensors in a Silicon-Germanium Bi-CMOS process. The chip we are designing with the colleagues of Rome Tor Vergata will have the world best timing performance for a monolithic pixel sensor and a very low power-consumption.

The scanner (a CAD design shown in the left-figure below) will be composed of 16 towers of 250µm thickness, each containing 60 layers of photon converter, monolithic pixel silicon sensor and front-end electronics. The dense layered structures and the monolithic integration of the detector provide a photon detection granularity of 500x500x250µm³. The mechanics has been designed and is being produced by the LHEP-Bern and the DPNC. The readout system by LHEP-Bern.

The PET scanner, comprising more than 1.5 million readout channels on 1920 chips, will be synchronised with 10 ps precision with an innovative technique, purposely developed for this project.
Sensor layout principle

- **Dielectric** for capacitive decoupling and low energy electron absorption.
- **Large PAD** ($<1\text{mm}^2$) readout to ensure uniform electric and weighting field.
- **Thin sensor** (100 $\mu$m) to minimize time walk correction.
- **Monolithic technology**: the electronics is embedded in the sensor. No need of wire bonding.
- **High-Z converter**, thickness optimized with dedicated simulation.

Monolithic integration of SiGe Bi-CMOS technology will lead to low-cost production of fast, solid state sensors.
The TT-PET scanner

“Detection Unit”

“Tower”

Adhesive tape (5 µm)
The TT-PET small-animal scanner

- The scanner will be made by 16 towers
- **1920 chips**; size: 25mm long, 7,9,11mm wide
- **1.6 M channels** synchronized at 10ps.
- High density of silicon pixel sensors: sensor power budget < 80 mW/cm²
- Finite-Element Analysis performed: active cooling:
  - Prototype cooling Block **produced**
  - Thermomechanical tower prototype **constructed**: results within power budget
The TT-PET small-animal scanner

- A scanner tower is a stack of 60 sensors, tightly coupled.
- Wedge-shaped units: three sensor widths
- Total tower thickness will be 1.5 cm.
- Two sensors per layer: length = 4.8 cm

Results of GEANT and FLUKA simulations: Tower efficiency for 511 keV photons: 27%
Challenges towards a monolithic ASIC:

**Time resolution of 30ps: ultra-fast electronics.**
- Achieved in discrete SiGe components, but need to implement it in ASIC.
  Need to **identify technology** that allows for it.

**Power consumption.**
- The initial testbeam results (discrete components) shown were obtained with a power consumption of \(\sim 1.4\text{W/cm}^2\). The target chip-power budget is **80mW/cm}^2**.

**Monolithic integration.**
- The monolithic integration requires to define a strategy on the sensor design to have a simple and effective structure, a detailed simulation work and **collaboration with the foundry**.

**Synchronisation of a thousand chips at few ps precision.**
- Given the low power budget, we have to work out a **new concept** for the TDC and synchronisation system.
• 3 \times 10 \text{ matrix, } 500 \times 500 \mu m^2 \text{ pixels.}
• Preamplifier, discriminator, 50 \text{ ps binning TDC, logic, serializer integrated in chip.}
• Thinned to 100 \mu m \text{ and backside metallized}

Three chips tested in the DPNC cleanrooms and at CERN testbeam.
CERN testbeam: Efficiency
CERN testbeam: Time resolution

- **4 articles:**
  - Demonstrator chip design: arxiv:1811.10246
  - Demonstrator chip testbeam: arxiv:1811.11114
  - TT-PET engineering: arxiv:1812.00788
  - TT-PET simulation & performance: arxiv:1811.12381

- **2 patent submissions:**
CERN testbeam: Time resolution

Particle hit time difference chip 1 vs chip 0

Entries: 1746375
Std Dev: 186 ± 0.1
Const: 5581 ± 6.0
Mean: 3.3 ± 0.1
Sigma: 161.3 ± 0.1
% Tails: 2 ± 0.1

\[ \sigma_t = \frac{161 \text{ ps}}{\sqrt{2}} = 114 \text{ ps} \]

With minimum-ionizing particles (corresponding to ~114/4 ~ 30ps for 511 keV converted photons)
The TT-PET ASIC
A monolithic silicon pixel detector:

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC length</td>
<td></td>
</tr>
<tr>
<td>ASIC width</td>
<td></td>
</tr>
<tr>
<td>Pixel Size</td>
<td></td>
</tr>
<tr>
<td>Pixel Capacitance (comprised routing)</td>
<td></td>
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<tr>
<td>Preamplifier power consumption</td>
<td></td>
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<tr>
<td>Preamplifier E.N.C.</td>
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<tr>
<td>Preamplifier Rise time (10% - 90%)</td>
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<tr>
<td>Time resolution for MIPs</td>
<td></td>
</tr>
<tr>
<td>TDC time binning*</td>
<td></td>
</tr>
<tr>
<td>TDC power consumption</td>
<td></td>
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</tbody>
</table>

* NOTE: 1920 chips synchronized at 10 ps precision.

A new TDC synchronization technique developed for this project patented by UNITEC:

Patent EP18181123
Towards silicon sensor with 1 ps resolution

Such sensor \textbf{does not exist}

We designed it

Need to control many things:
• GAIN (50-100 $\Rightarrow$ Avalanche detector)
• Minimize capacitance $\Rightarrow$ geometry with small pixels
• ...
Present performance of our electronics

\[ E_{\text{ENC}} = 80 \, e^+ \quad \text{Equivalent Noise Charge for } C = 50 \, fF \quad \Rightarrow \quad \sigma_{\text{time}} = 4 \, \text{ps} \]
The **PicoAD**: Picosecond Avalanche Detector

**Monolithic integration in a SiGe BiCMOS process:**
- Fast, low noise SiGe HBT.
- Ultra fast time digitization.
- Control of the gain at single pixel level.
- Scalable design for very large active area.
- **Low cost** production.
- Mechanically **robust**.

**Pixelated readout:**
- Tracking capability **AND** picosecond time measurement with full fill factor

**5 µm PN-drift region:**
- Low pixel capacitance.
- Fast induction by capacitive coupling.

**1 µm PN-gain region:**
- Uniform gain layer for stable operation in avalanche mode.
- Electric field modelling.
- Very high **fill factor**.
- Modular design: can be adapted to different purposes.

**Patent submitted via UNITEC**
Photon Detection with the PicoAD

Visible light
- Exceptional time resolution: $\lambda \rightarrow 500 \text{ nm}$
- Low voltage (20-30V) operation.

Near IR light
- Excellent time resolution: $\sigma_t < 30 \text{ ps}$
- First: INNOGAP project
- $\lambda \rightarrow 900 \text{ nm}$

Customizable converter layer
- Deposit of epi-layer or coating: SiGe layer & Ge implants
- $\lambda > 900 \text{ nm}$

Hybrid solutions
- Bump bonding of different sensors: Germanium III-V substrates SiC, CdTl...