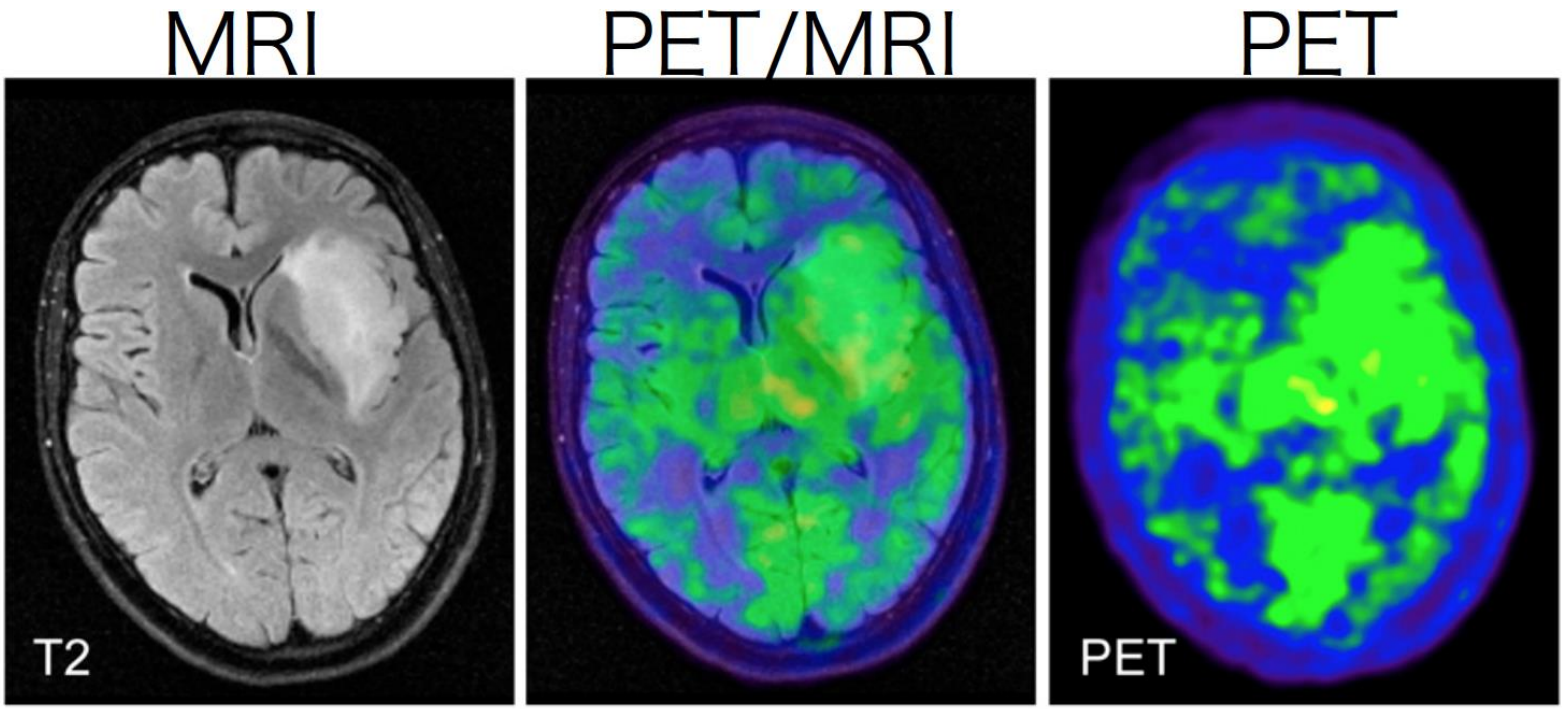
TT-PET project

M.Nessi

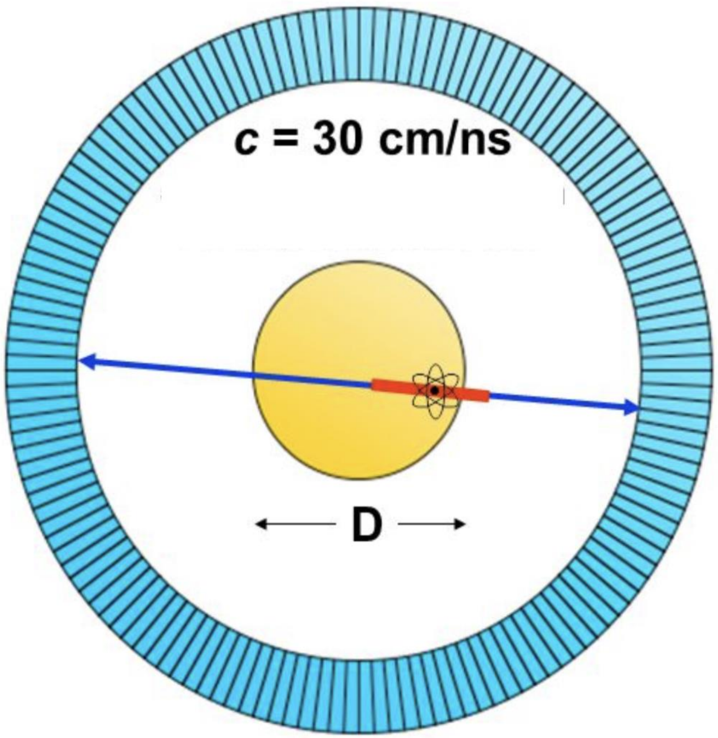
22-02-2019



(10.2967/jnumed.110.074773)

- Positron Emission Tomography (PET)
  - Positrons from a radionuclide introduced in a body annihilate with the nearby tissue, emitting two back-to-back photons
  - The photons are detected in coincidence, tracking a line of response (LOR)
- Hybrid PET-MRI Imaging
  - Combining functional Image by PET and morphological image by MRI

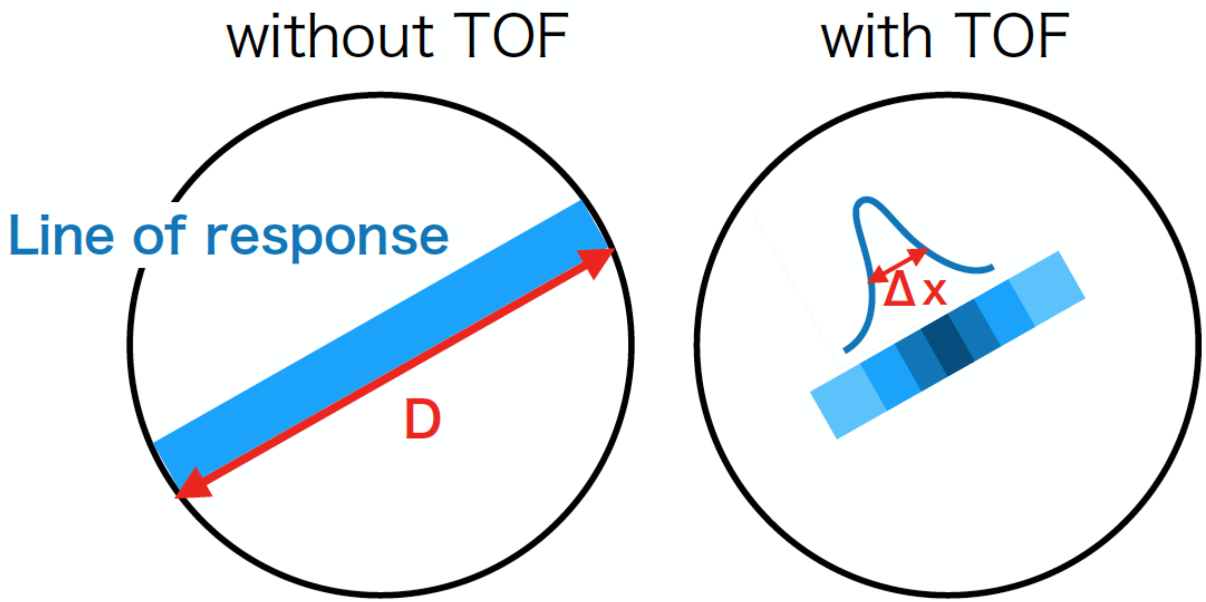
Time-Of Flight PET



Improved resolution
by measurement of
difference in arrival time
of the two photons.

Goal:
30 ps time resolution
for ~mm spatial measurement

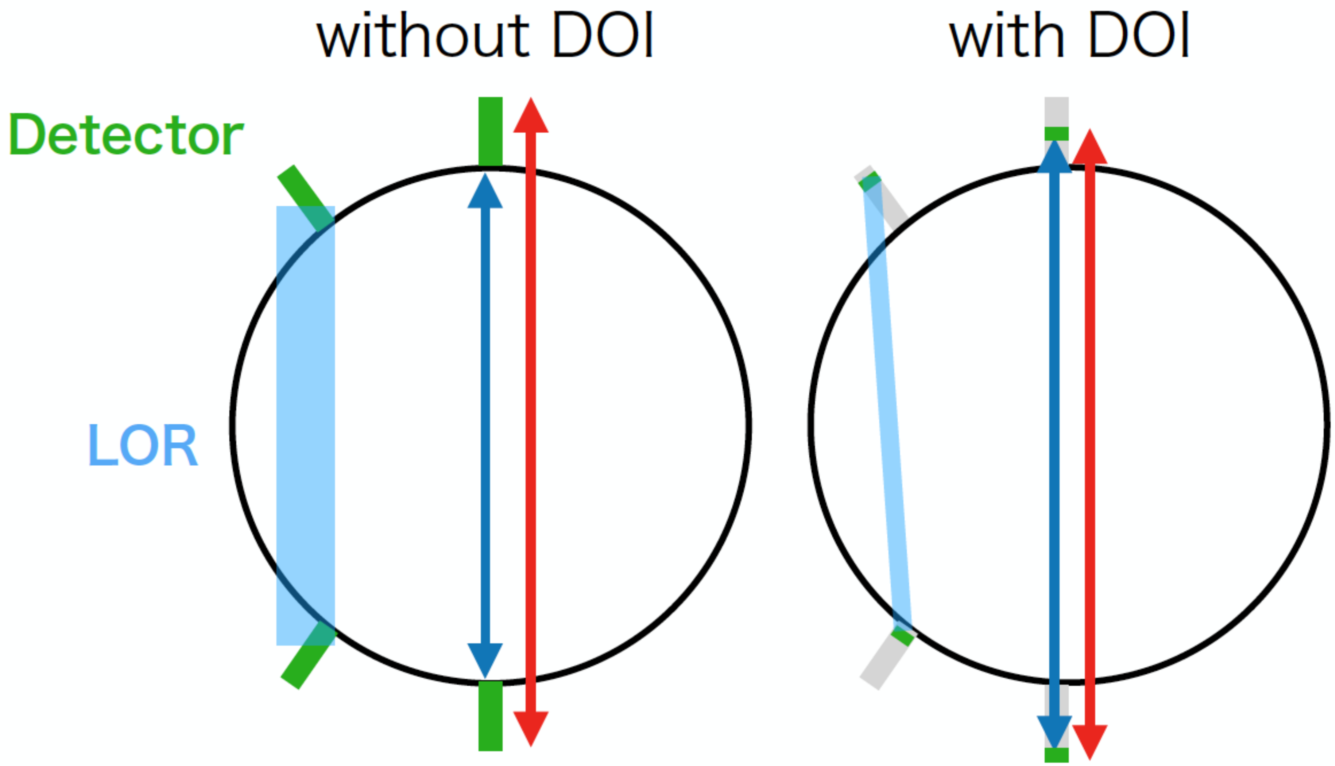
- *less radio dose to patients*
- *better spatial resolution*
- *possible to be inserted in an MRI facility*



- TOF information improves the signal-to-noise ratio (SNR) of reconstructed images

$$\frac{\mathrm{SNR}_{TOF}}{\mathrm{SNR}_{CONVENTIONAL}} \sim \sqrt{\frac{D}{\Delta x}}$$

Depth-of-Interaction (DOI)

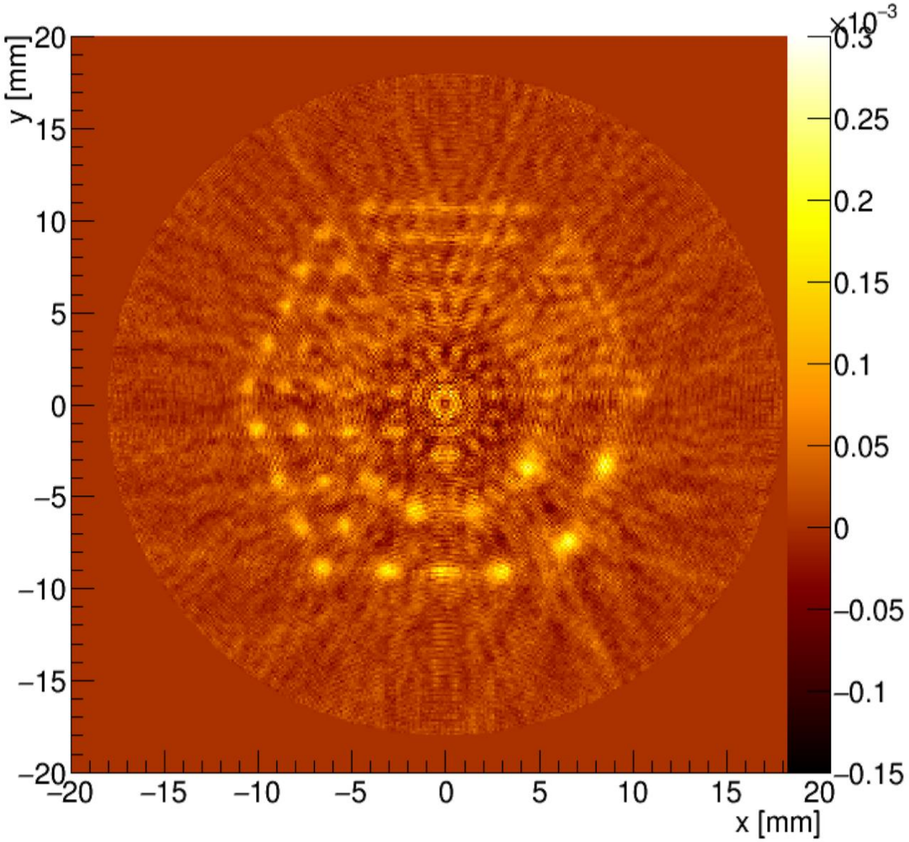


- Sensitivity for photon depth of interaction improves the spatial resolution across the whole view of the scanner
- It also reduces the uncertainty of TOF measurements

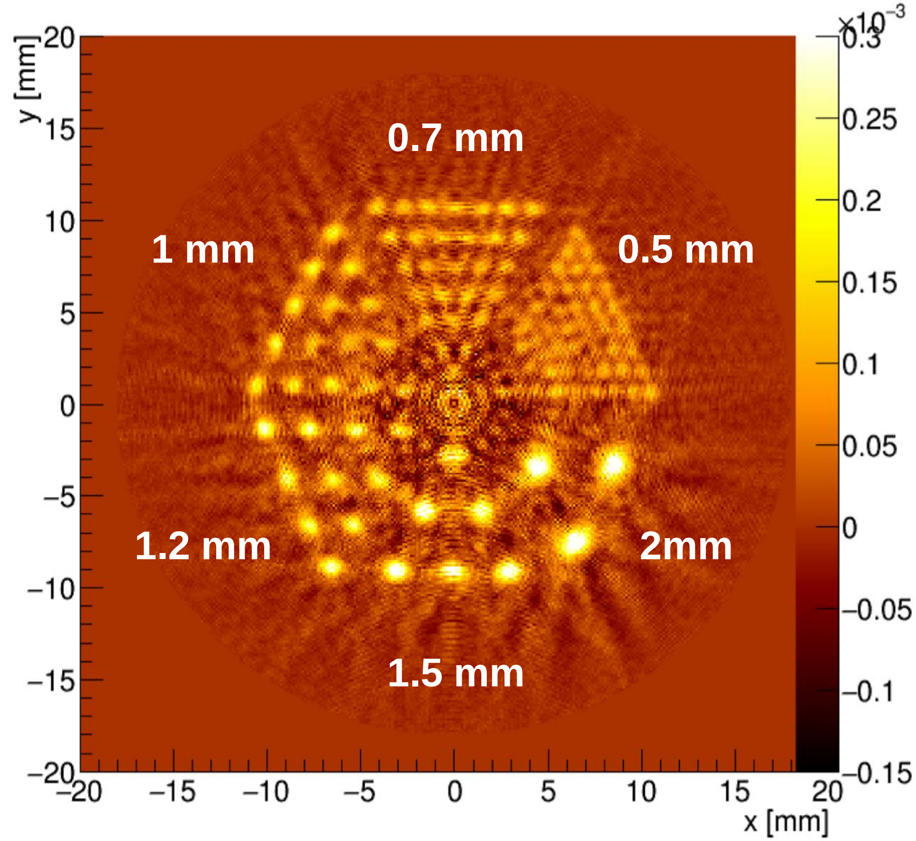
Derenzo phantom GEANT4 simulation

TT-PET simulation

no – TOF information

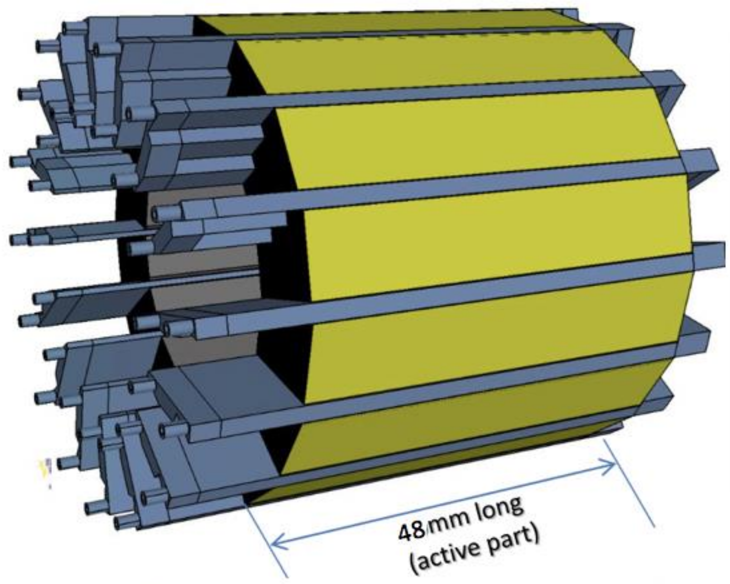


TOF information



The TT-PET project:
a 30 ps Time-of-Flight PET scanner with silicon

TT-PET Project



UNIVERSITÉ DE GENÈVE

Hôpitaux Universitaires Genève

UNIVERSITÄT BERN

AEC ALBERT EINSTEIN CENTER FOR FUNDAMENTAL PHYSICS

Funded by:

FNSNF SWISS NATIONAL SCIENCE FOUNDATION

In collaboration with:

- Roberto Cardarelli - INFN Roma Tor Vergata
- Craig Levin - Stanford University
- Marzio Nessi - CERN IdeaSquare
- IHP microelectronics

GR02/TT-PET

Thin Time-Of-Flight PET project

Overview | Teams | Participations

SPOKESPERSON:	Giuseppe IACOBUCCI
DEPUTY SPOKEPERSON(S):	Marzio NESSI
CONTACT PERSON:	Markus Yrjo NORDBERG
TECHNICAL COORDINATOR:	Frank Raphael CADOUX
RESOURCES COORDINATOR:	
GROUP LEADER IN MATTERS OF SAFETY (GLIMOS):	
DEPUTY GLIMOS:	
DEPARTMENTAL FLAMMABLE GAS SAFETY OFFICER (FGSO):	
DEPARTMENTAL CRYOGENICS OFFICER (CSO):	
EXPERIMENT SECRETARIAT E-MAIL:	sandy.petitfrere@cern.ch
EXPERIMENT SECRETARIAT WEB SITE:	

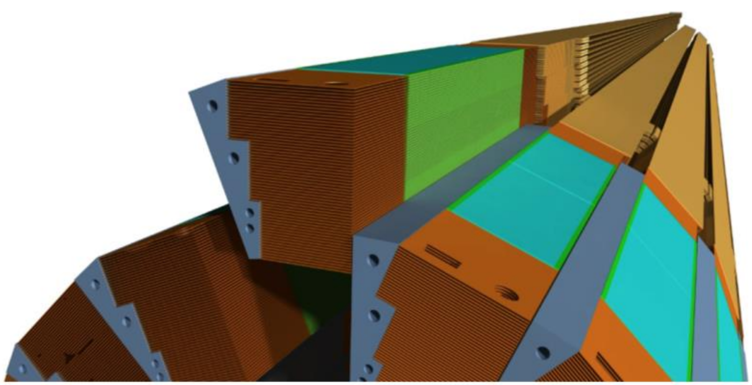
TT-PET

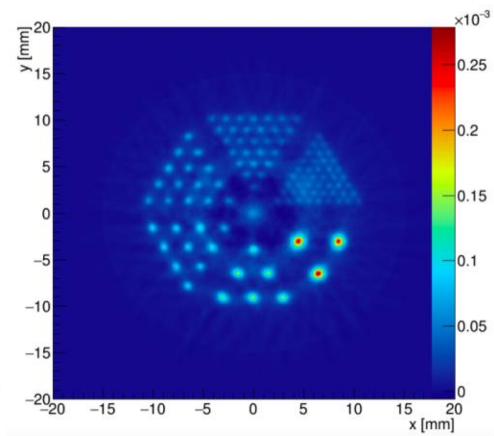
- ✓ Fully financed by a SWISS research grant (>2MCH)
- ✓ First demonstrator phase will end in spring 2019
- ✓ A new proposal for a full device construction has been submitted to the Swiss grant system
- ✓ Very interesting THz electronics technology

THE TT-PET PROJECT

The **Thin Time-Of-Flight Positron Emission Tomography** (TT-PET) project (SNSF grant CRSII2_160808) aims at developing a pre-clinical TOF-PET scanner with very precise 3D spatial reconstruction, for ultimate use in an MRI scanner. The 3D measurement will be achieved by TOF measurement with 30ps time resolution, obtained by monolithic pixel silicon sensors in a Silicon-Germanium Bi-CMOS process. The chip we are designing with the colleagues of Rome Tor Vergata will have the world best timing performance for a monolithic silicon pixel sensor and a very low power-consumption.

The scanner (a CAD design shown in the left-figure below) will be composed of 16 towers of 250μm thickness, each containing 60 layers of photon converter, monolithic pixel silicon sensor and front-end electronics. The dense layered structures and the monolithic integration of the detector provide a photon detection granularity of 500x500x250μm³. The mechanics has been designed and is being produced by the LHEP-Bern and the DPNC. The readout system by LHEP-Bern.





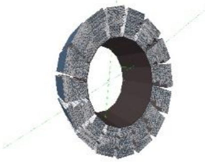
The PET scanner, comprising more than 1.5 million readout channels on 1920 chips, will be synchronised with 10 ps precision with an innovative technique, purposely developed for this project.

Sensor layout principle

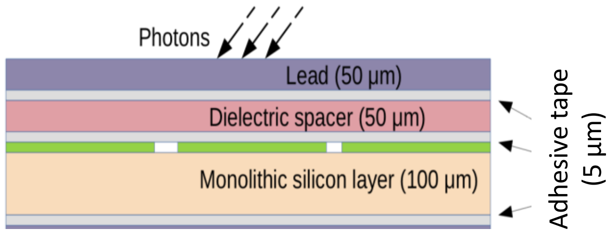
Monolithic integration of SiGe Bi-CMOS technology will lead to low-cost production of fast, solid state sensors.

- **Dielectric** for capacitive decoupling and low energy electron absorption.
- **Large PAD** (<1mm^2) readout to ensure uniform electric and weighting field.
- **Thin sensor** (100 μm) to minimize time walk correction.
- **Monolithic technology**: the electronics is embedded in the sensor. No need of wire bonding.
- **High-Z converter**, thickness optimized with dedicated simulation.

The TT-PET scanner

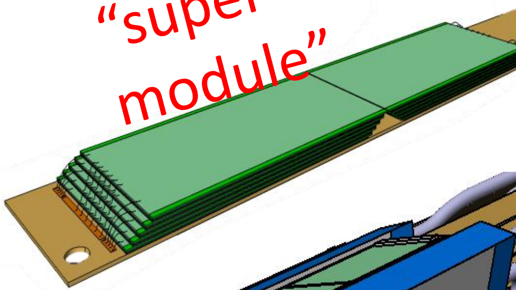


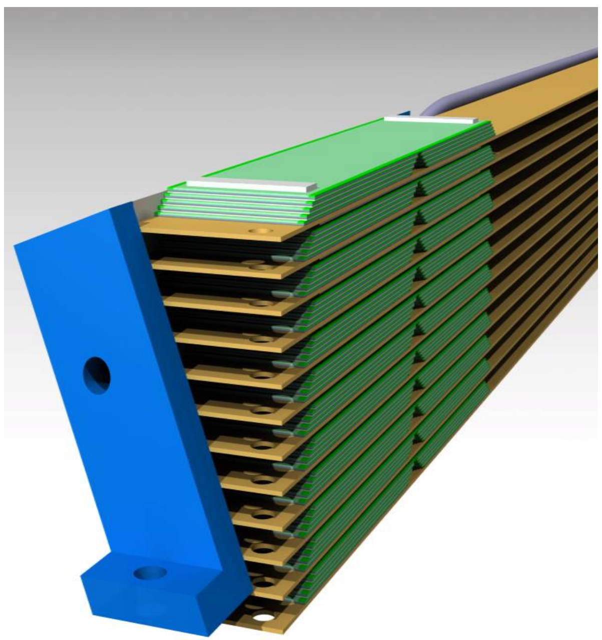
TT-PET



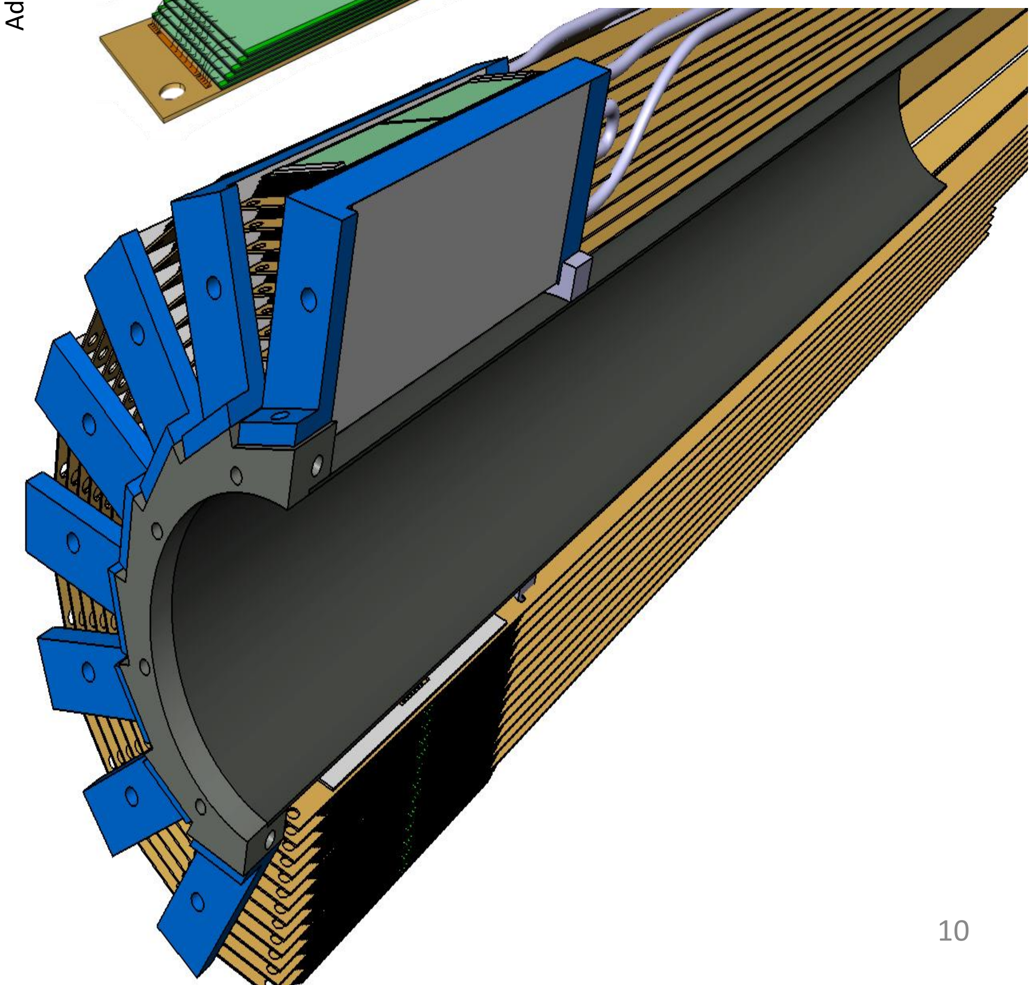
“Detection Unit”

“super-module”



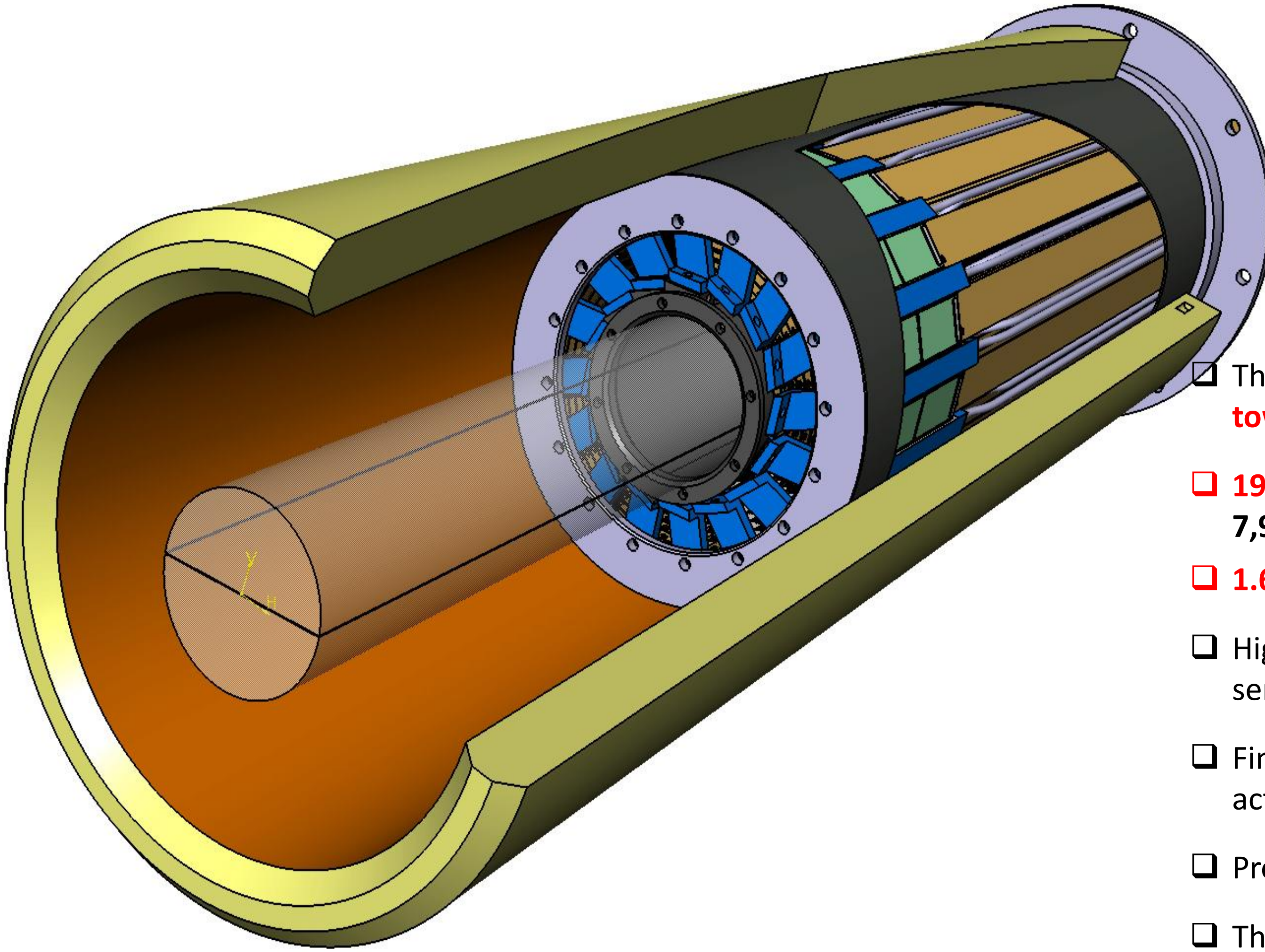


“Tower”



TT-PET

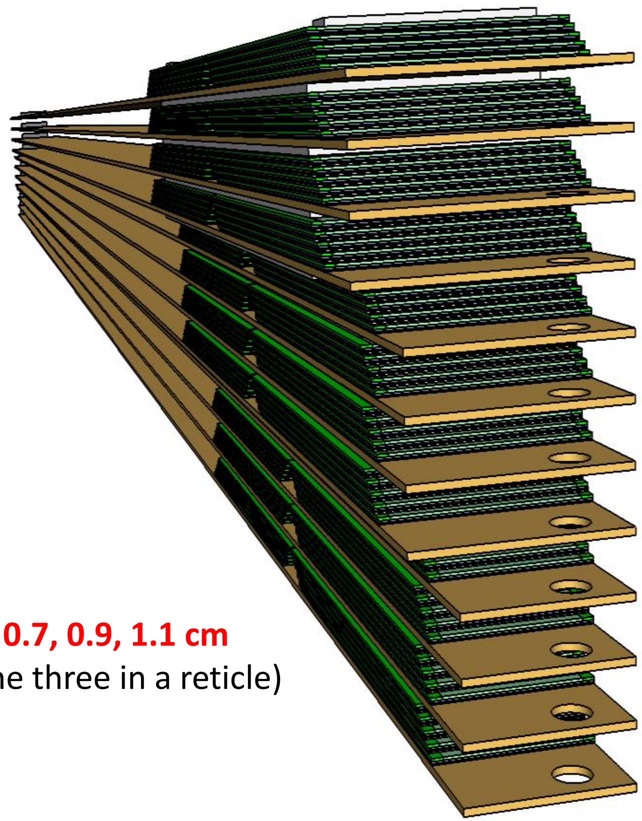
The TT-PET small-animal scanner



- The scanner will be made by **16 towers**
- **1920 chips; size: 25mm long, 7,9,11mm wide**
- **1.6 M channels** synchronized at 10ps.
- High density of silicon pixel sensors: sensor power budget < **80 mW/cm^2**
- Finite-Element Analysis performed: active cooling:
- Prototype cooling Block produced
- Thermomechanical tower prototype constructed: results within power budget

TT-PET

The TT-PET small-animal scanner



3 sensor widths: 0.7, 0.9, 1.1 cm
(sizes chosen to fit the three in a reticle)

- A scanner tower is a stack of **60 sensors**, tightly coupled.
- Wedge-shaped units: three sensor widths
- Total tower thickness will be **1.5 cm**.
- Two sensors per layer: length = **4.8 cm**

FLUKA and Geant4 simulations performed to predict the scanner efficiency to 511 keV photons, the expected detection rate per chip and the scanner space resolution.

Results of GEANT and FLUKA simulations: Tower efficiency for 511 keV photons: 27%

Challenges towards a monolithic ASIC:

Time resolution of 30ps: ultra-fast electronics.

- Achieved in discrete SiGe components, but need to implement it in ASIC.
  Need to **identify technology** that allows for it.

Power consumption.

- The initial testbeam results (discrete components) shown were obtained with a power consumption of ~1.4W/cm^2. The target chip-power budget is **80mW/cm^2**.

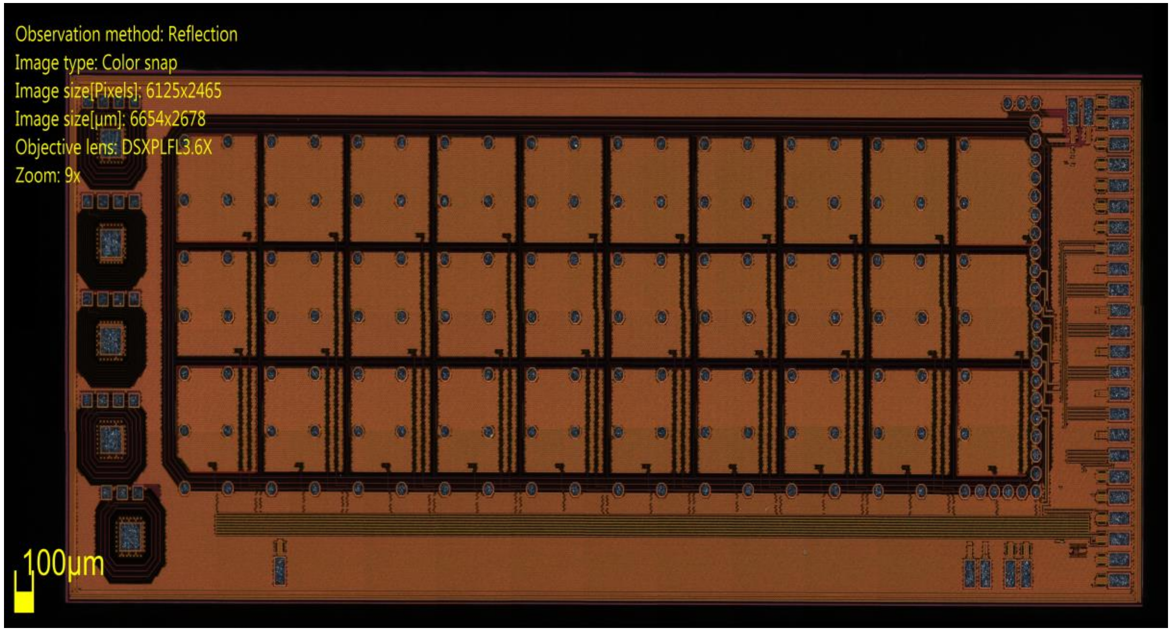
Monolithic integration.

- The monolithic integration requires to define a strategy on the sensor design to have a simple and effective structure, a detailed simulation work and **collaboration with the foundry**.

Synchronisation of a thousand chips at few ps precision.

- Given the low power budget, we have to work out a **new concept** for the TDC and synchronisation system

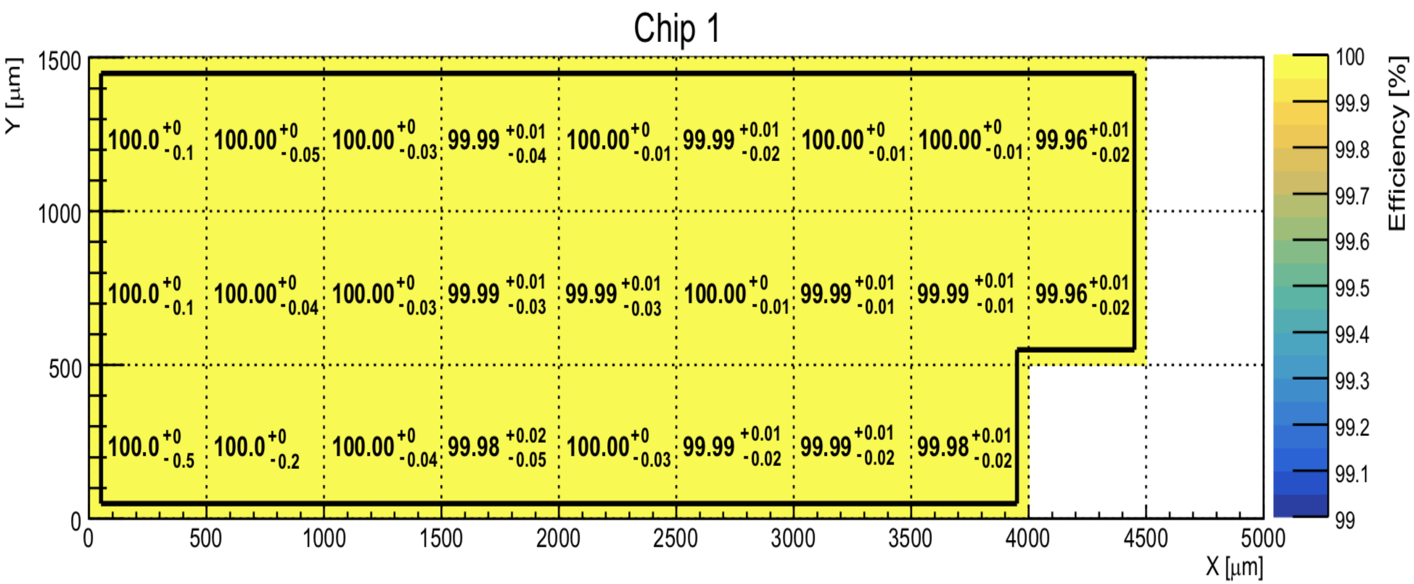
Layout of the TT-PET demonstrator



- 3×10 matrix, $500 \times 500\ \mu m^2$ pixels.
- Preamplifier, discriminator, $50\ ps$ binning TDC, logic, serializer integrated in chip.
- Thinned to 100 µm and backside metallized

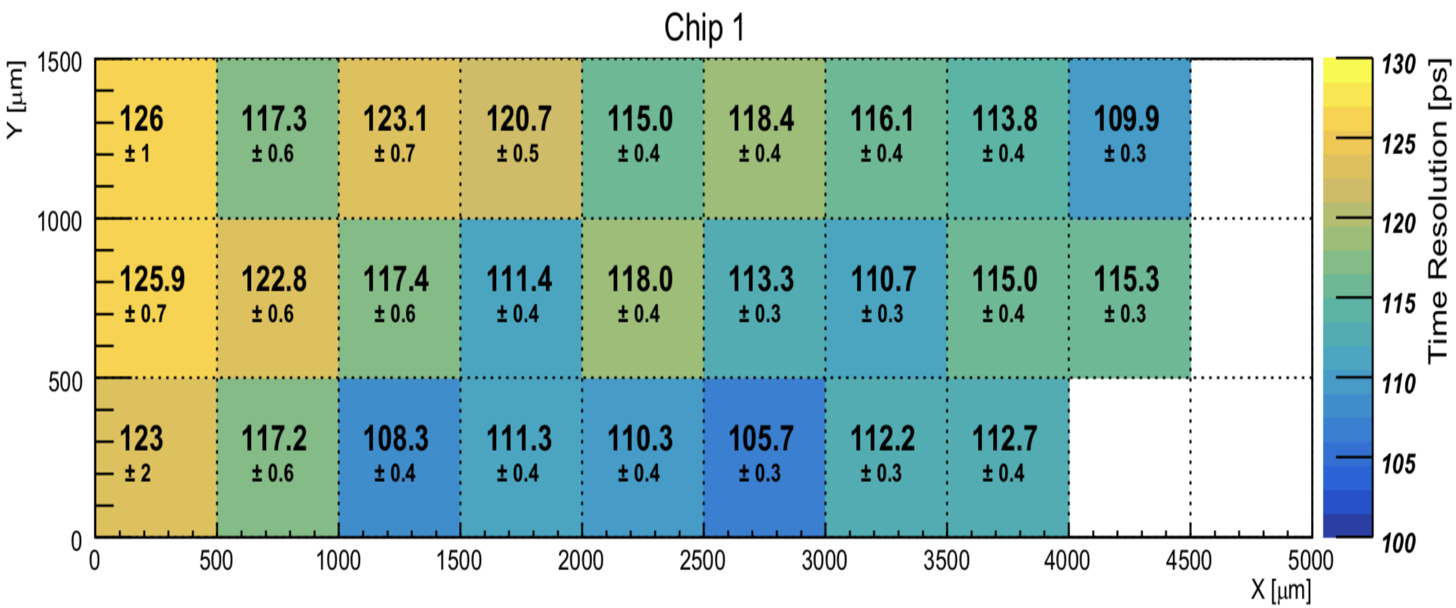
Three chips tested in the DPNC cleanrooms and at CERN testbeam.

CERN testbeam: Efficiency



TT-PET

CERN testbeam: Time resolution

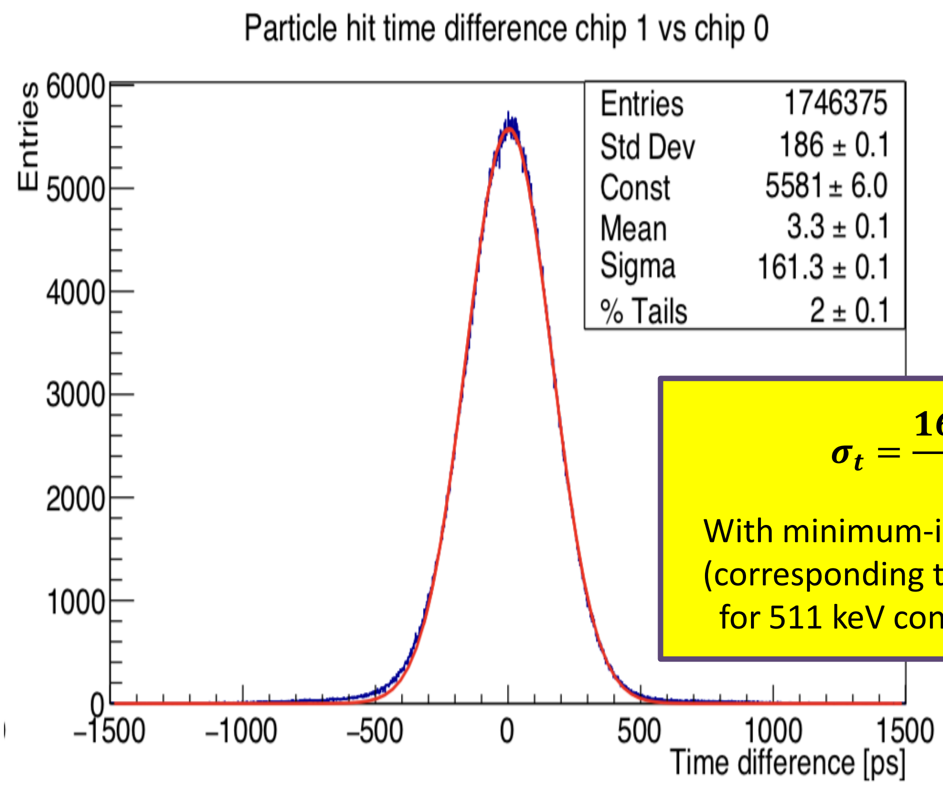


- 4 articles:
  - Demonstrator chip design: arxiv:1811.10246
  - Demonstrator chip testbeam: arxiv:1811.11114
  - TT-PET engineering: arxiv:1812.00788
  - TT-PET simulation & performance: arxiv:1811.12381

- 2 patent submissions:
  - PLL-less TDC & synchr. System: EU Patent Application EP18181123.3
  - Multi-Junction PicoAD: EU Patent Application EP18207008.6

CERN testbeam: Time resolution

TT-PET



$$\sigma_t = \frac{161\ ps}{\sqrt{2}} = 114\ ps$$

With minimum-ionizing particles (corresponding to ~114/4 ~ 30ps for 511 keV converted photons)

The TT-PET ASIC

A monolithic silicon pixel detector:

ASIC length	
ASIC width	
Pixel Size	
Pixel Capacitance (comprised routing)	
Preamplifier power consumption	
Preamplifier E.N.C.	
Preamplifier Rise time (10% - 90%)	
Time resolution for MIPs	
TDC time binning*	
TDC power consumption	

*** NOTE: 1920 chips synchronized at $10\ ps$ precision.**

A new TDC synchronization technique developed for this project patented by UNITEC:

Patent EP18181123

Towards silicon sensor with 1 ps resolution

Such sensor **does not exist**

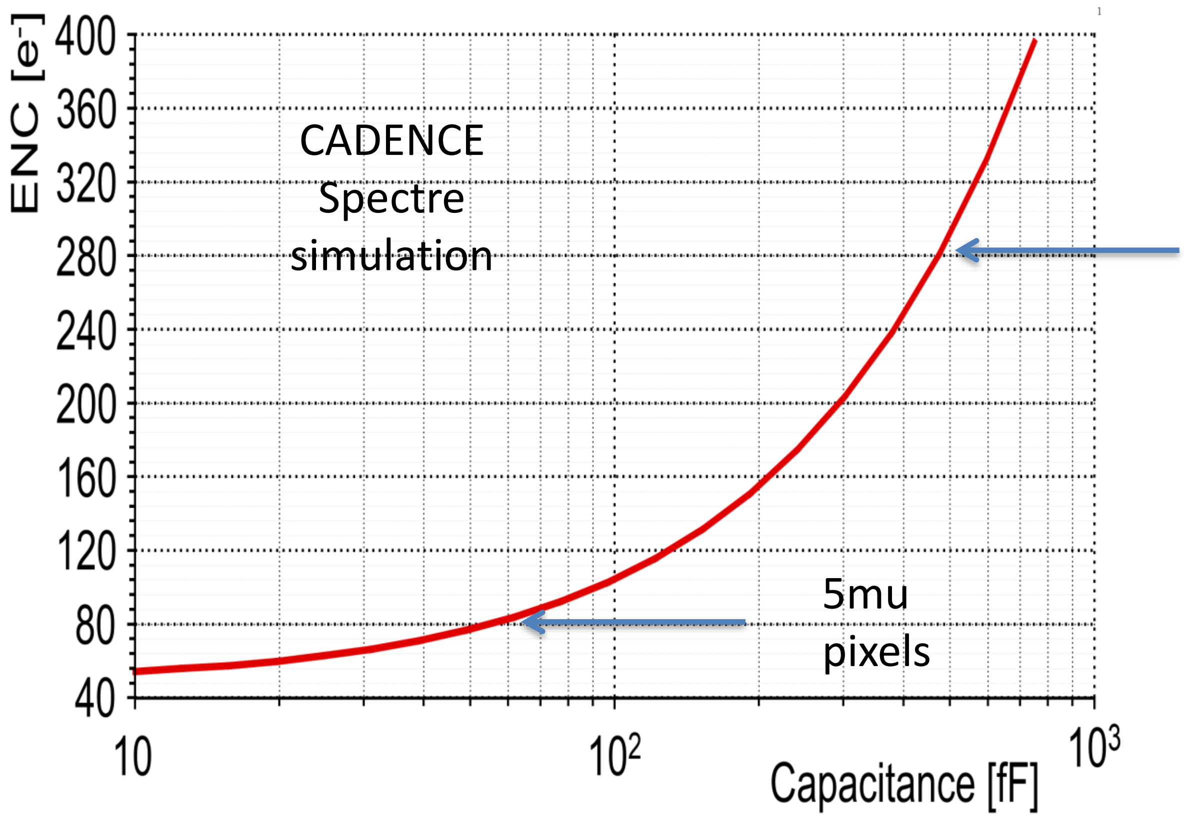
We designed it

Need to control many things:

- GAIN (50-100 $\Longrightarrow$ Avalanche detector)
- Minimize capacitance $\Longrightarrow$ geometry with small pixels
- …

Patent submitted via UNITEC

Present performance of our electronics



80 e^- Equivalent Noise Charge for C = 50 fF $\Longrightarrow$ $\sigma_{time} = 4$ ps

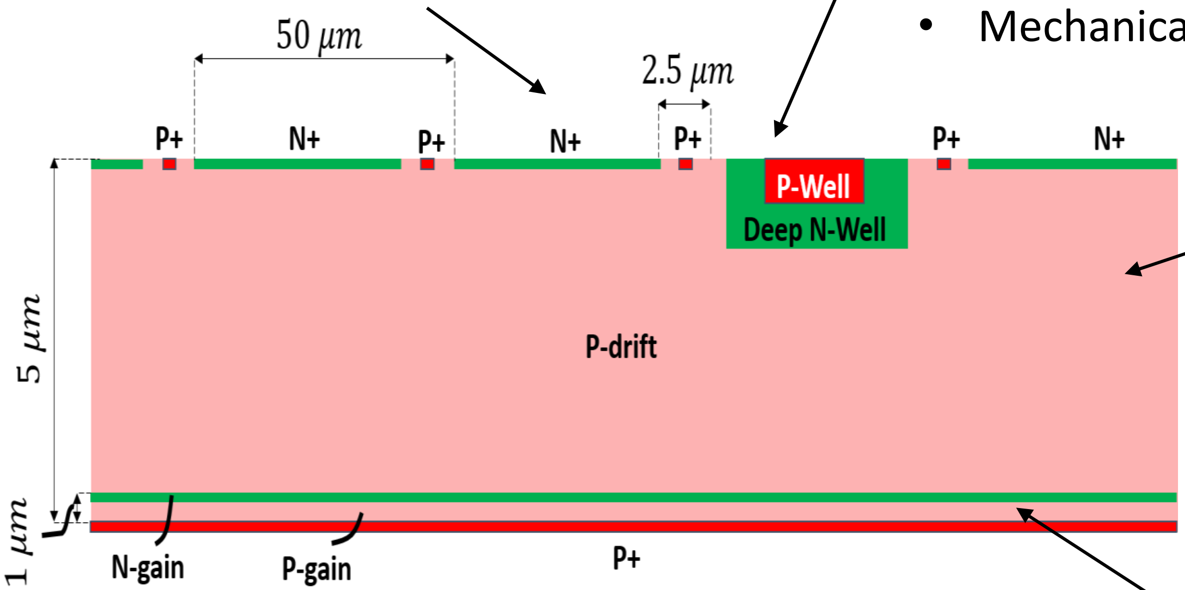
The **PicoAD**: Picosecond Avalanche Detector

Pixelated readout:

- **Tracking capability AND picosecond time measurement** with **full fill factor**

Monolithic integration in a SiGe BiCMOS process:

- **Fast, low noise SiGe HBT.**
- Ultra fast time digitization.
- Control of the gain at single pixel level.
- Scalable design for very large active area.
- **Low cost** production.
- Mechanically **robust**.



5 μm PN-drift region:

- **Low pixel capacitance.**
- **Fast** induction by capacitive coupling.

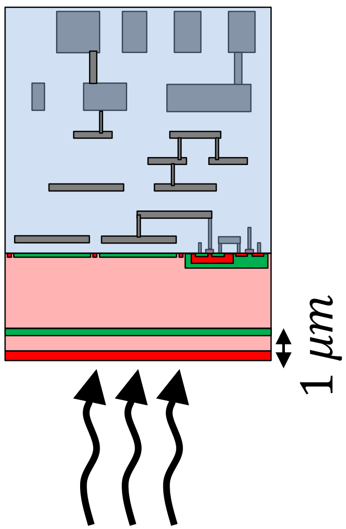
1 μm PN-gain region:

- Uniform gain layer for **stable operation** in avalanche mode.
- Electric field modelling.
- Very high **fill factor**.
- Modular design: can be adapted to different purposes.

Patent submitted via UNITEC

Photon Detection with the PicoAD

Visible light

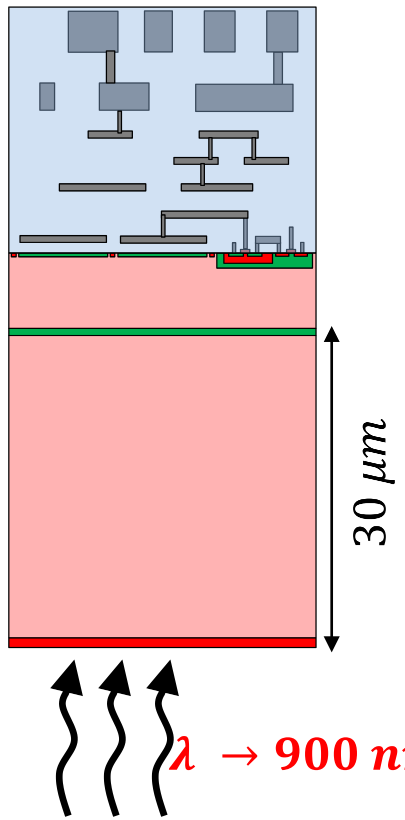


$\lambda \rightarrow 500\ nm$

Exceptional time resolution:

Low voltage (20-30V) operation.

Near IR light



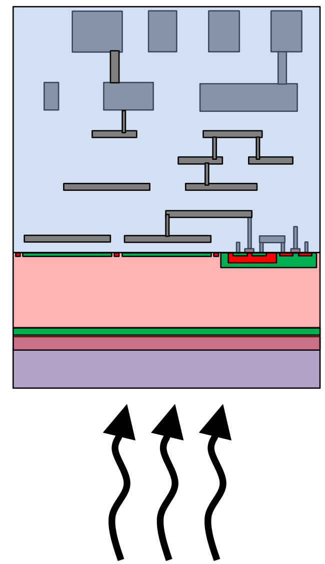
$\lambda \rightarrow 900\ nm$

Excellent time resolution:

$\sigma_t < 30\ ps$

First: **INNOGAP project**

Customizable **converter** layer

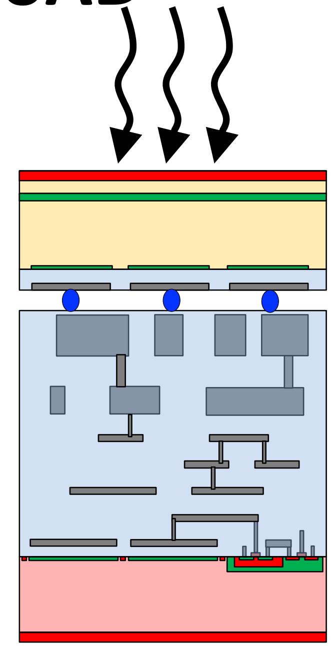


$\lambda > 900\ nm$

Deposit of epi-layer or coating:

SiGe layer & Ge implants

…



Hybrid solutions

Bump bonding of different sensors:

Germanium

III-V substrates

SiC, CdTl…