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SI LAB
Silizium Labor Bonn

# RD53A WAFER PROBING
# RESULTS AND CUTS

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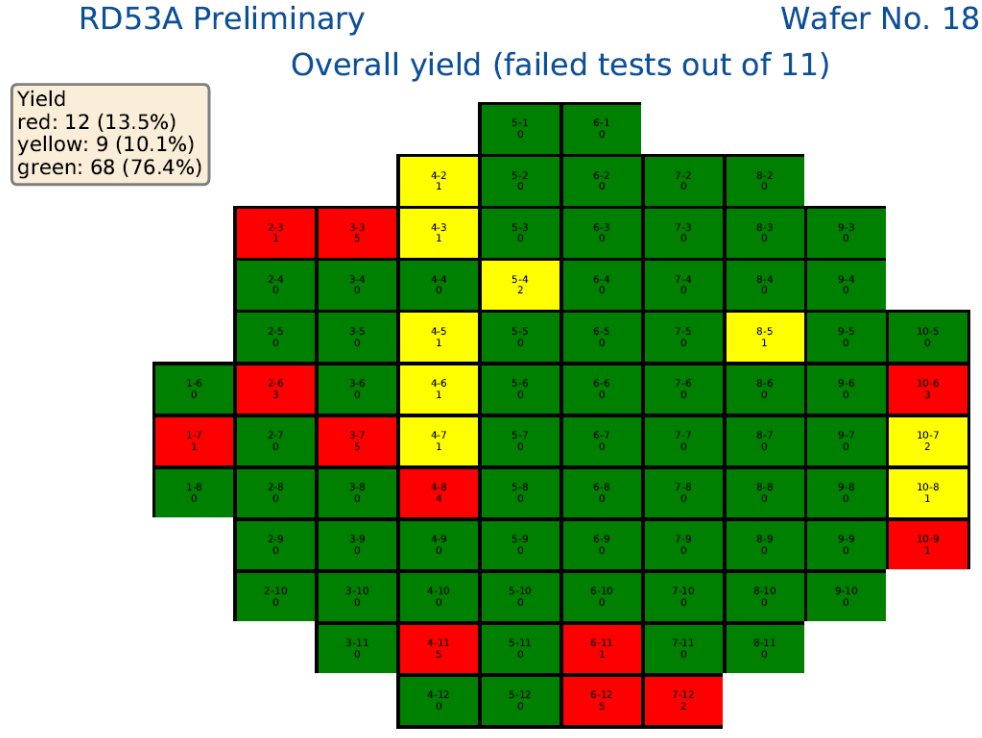
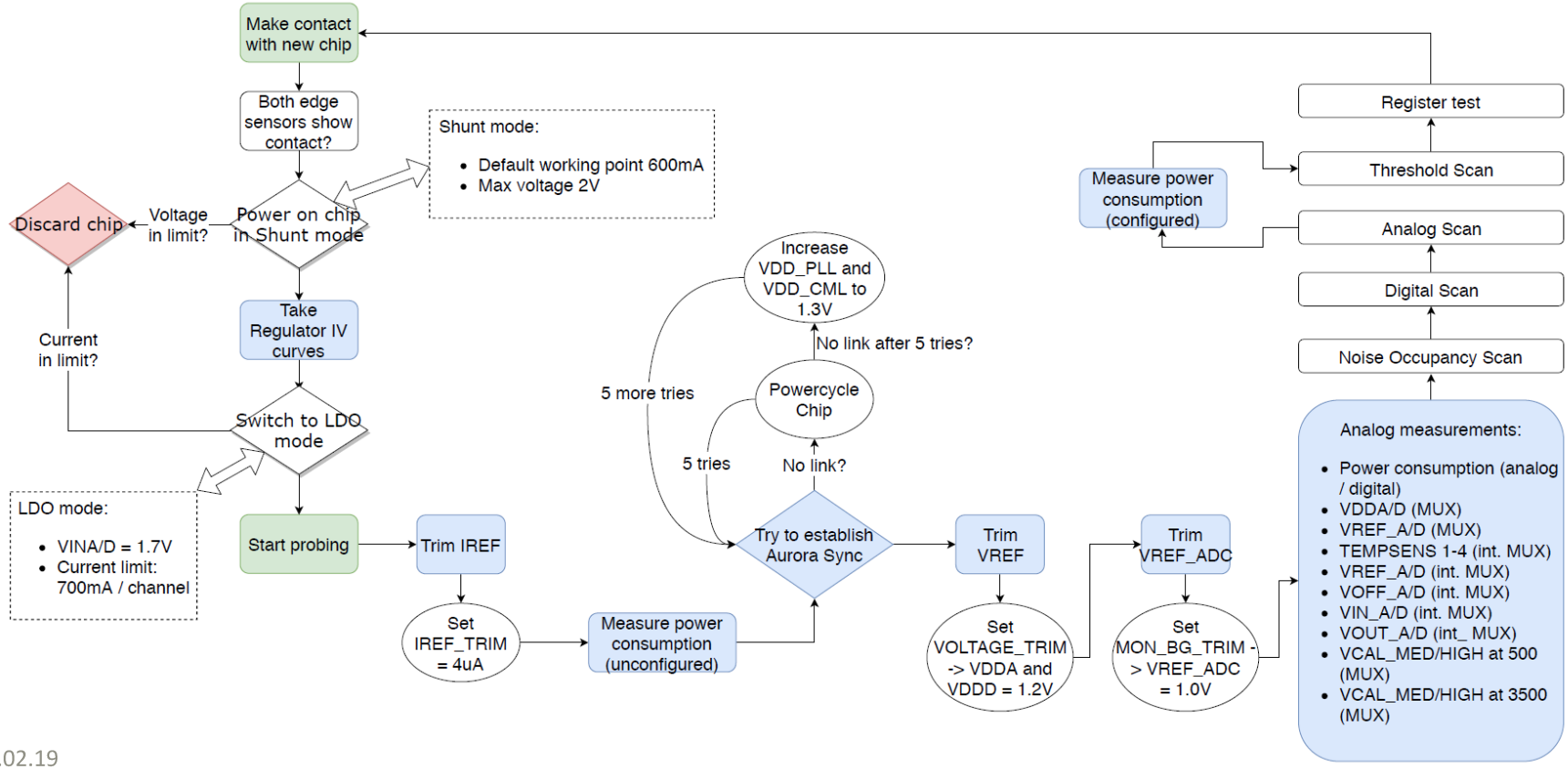
# OVERALL RESULTS

- This talk: 10 wafers from Lot 1
- Mean yield:
  - 65.4% green (min 54%, max 78%)
  - 7.6% yellow (min 2%, max 13%)
  - 27% red (min 11%, max 42%)
    - 2-3 and 10-9 **removed from distribution**
    - Not fully processed on the wafer
    - Never work, artificially lower yield



# TEST PROCEDURE



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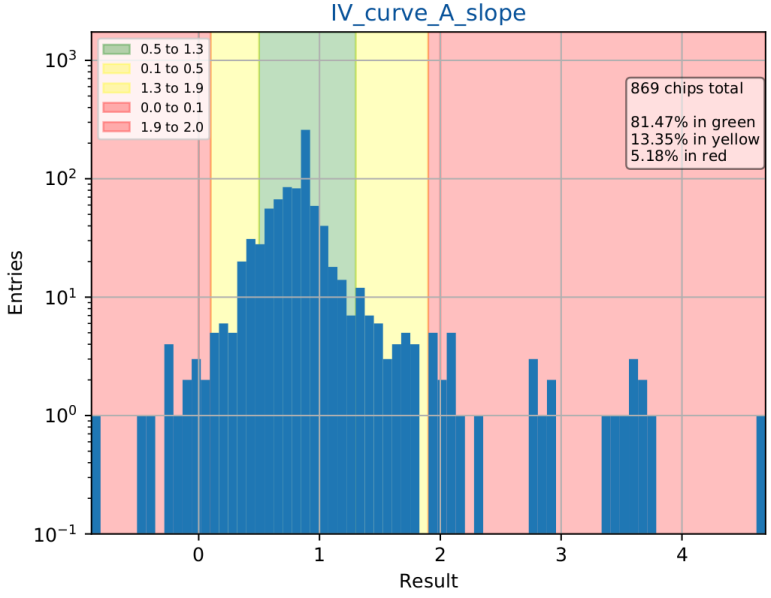
# TEST RESULT OVERVIEW

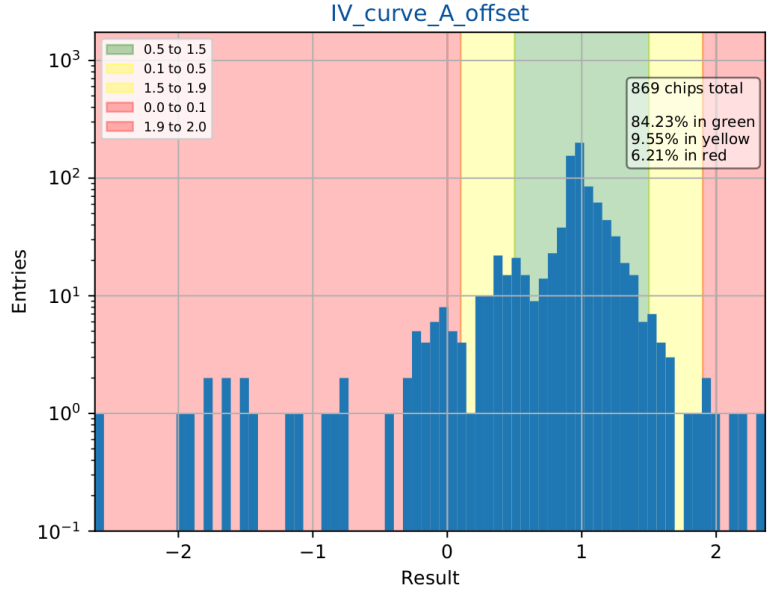
In total 870 chips tested

- Initial power-up
  - 9 (~1%) chips discarded (short)
- Overall not one single "yield killer"
- * Scans are only performed if chip has Aurora Sync

| Test | green | yellow | red |
|---|---|---|---|
| Regulator IV curves (mean) (ignored for total yield) | 84.5% | 9.6% | 5.9% |
| IREF after trimming | 94.4% | 0.5% | 5.9% |
| AURORA link | 87.1% | 2.8% | 10.1% |
| VDDA after trimming | 91.1% | 3% | 5.9% |
| VDDD after trimming | 94.8% | 3% | 2.2% |
| VREF ADC after trimming | 88% | 6.8% | 5.2% |
| Total power consumption* | 98.8% | 1.1% | 0.1% |
| Noise occupancy scan* (ignored for total yield) | 87.4% | 5.1% | 7.5% |
| Digital scan* | 95.2% | 1% | 3.8% |
| Analog scan* | 85.5% | 1.8% | 12.7% |
| Threshold scan* | 90.7% | 2.3% | 7% |

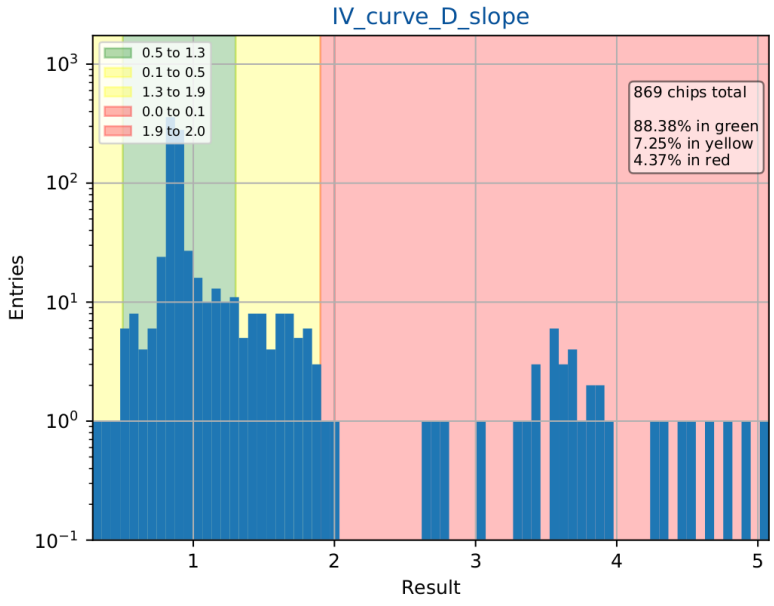
# ANALOG REGULATOR IV CURVE

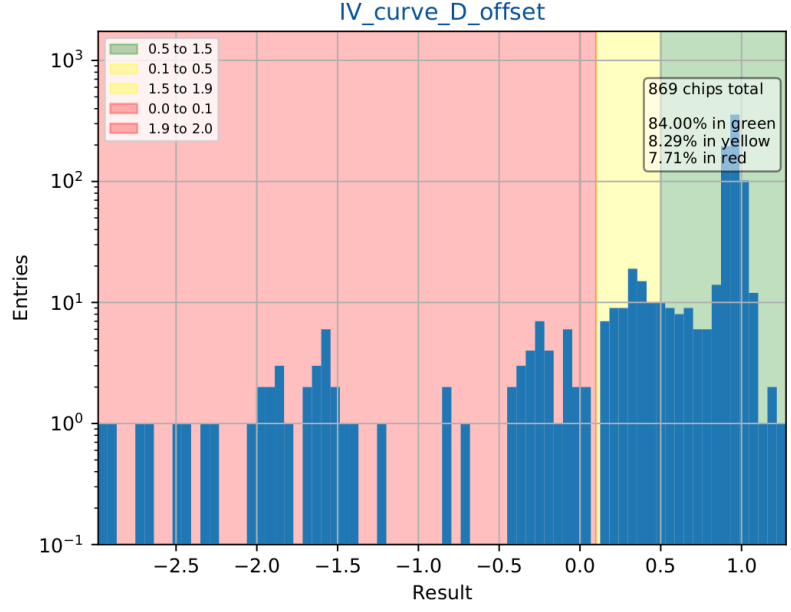



- Overall rather broad distribution
- So far ignored for total yield

# DIGITAL REGULATOR IV CURVE



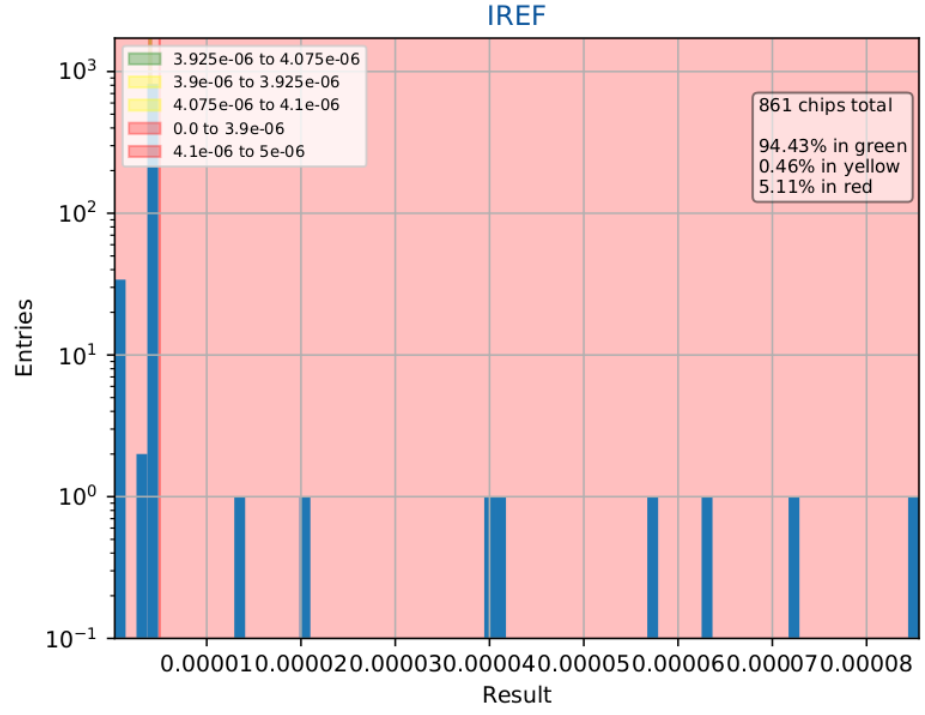




- Like analog regulators: very broad distribution
- So far ignored for total yield

# IREF AFTER TRIMMING

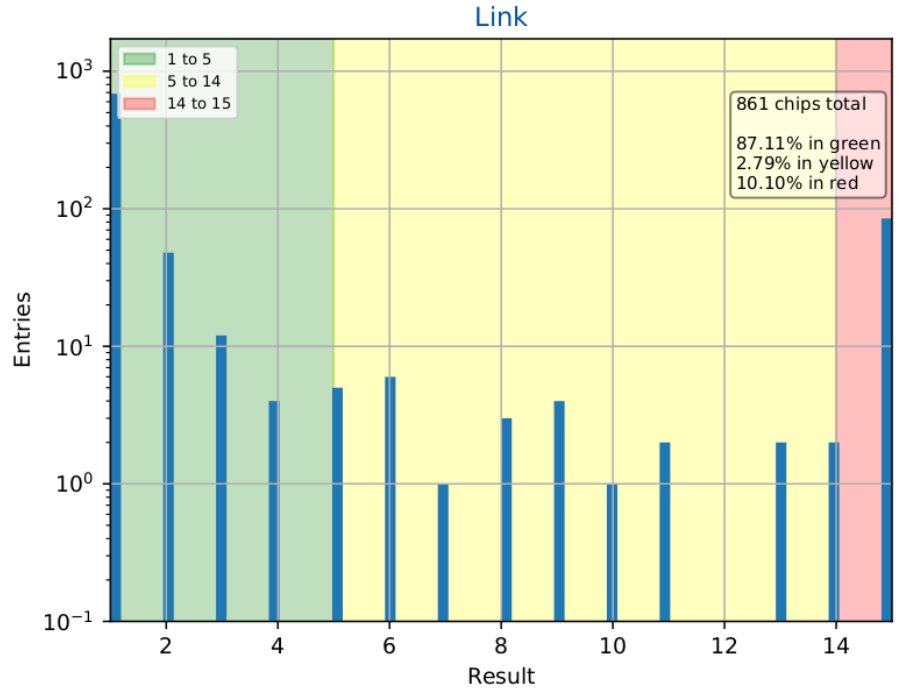
- Set every trim bit and measure IREF
- Choose closest to 4uA
- Measure resulting IREF

- Hard cut
- Still 94% in green category



# AURORA LINK

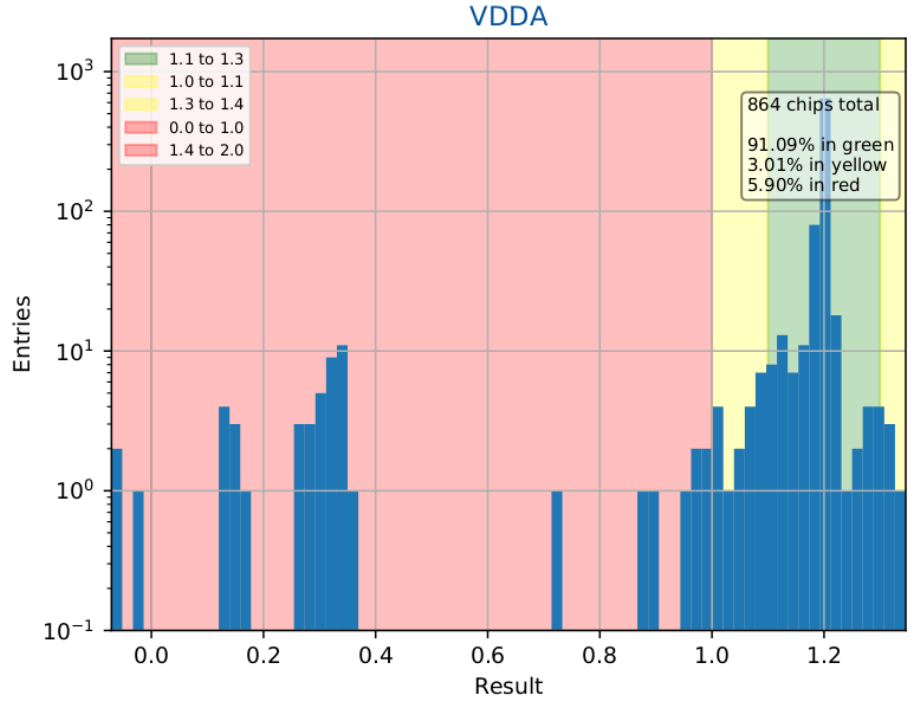
- Try to establish AURORA link
  - VDD_PLL/_CML = VDDA before trimming
- If no link, powercycle chip and retry
- If no link after 5 tries, set VDD_PLL /_CML to 1.2V
- Try another 5 times
- If still no link, set VDD_PLL /_CML to 1.3V
- Try another 5 times
- If still no link -> red



# VDDA AFTER TRIMMING

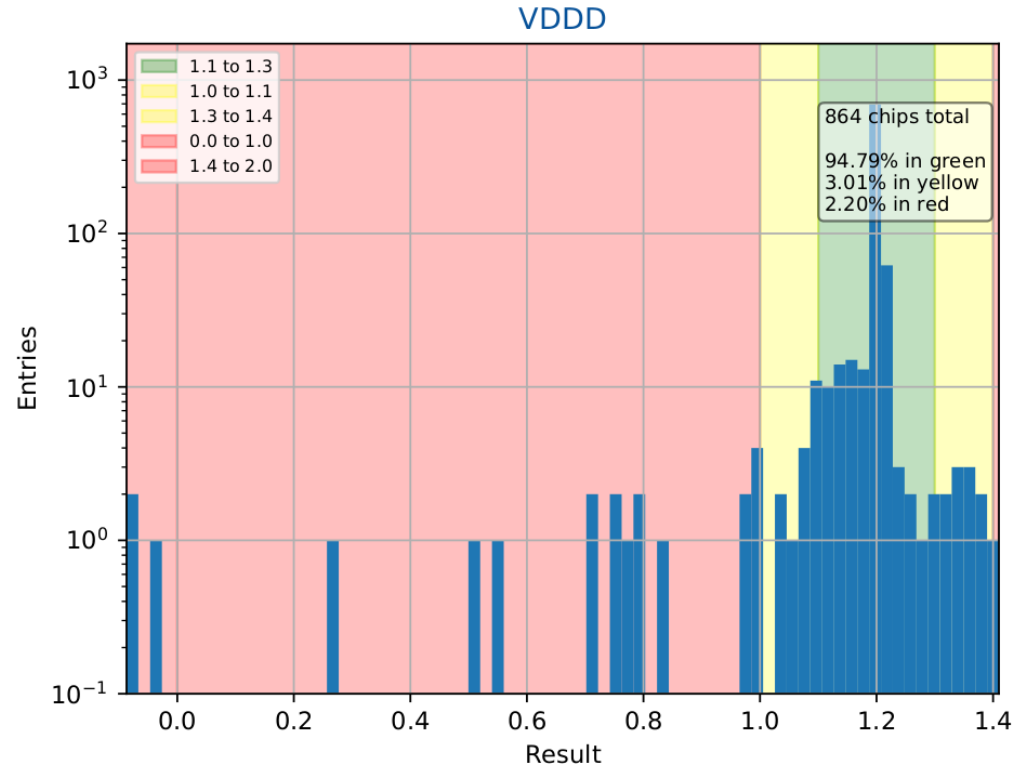
- Trim through all VOLTAGE_TRIM bits
- Select the one where VDDA is closest to 1.2V
- Measure VDDA

- TODO: Start green category at 1.15V
  - Green chips should definitely work in LDO mode



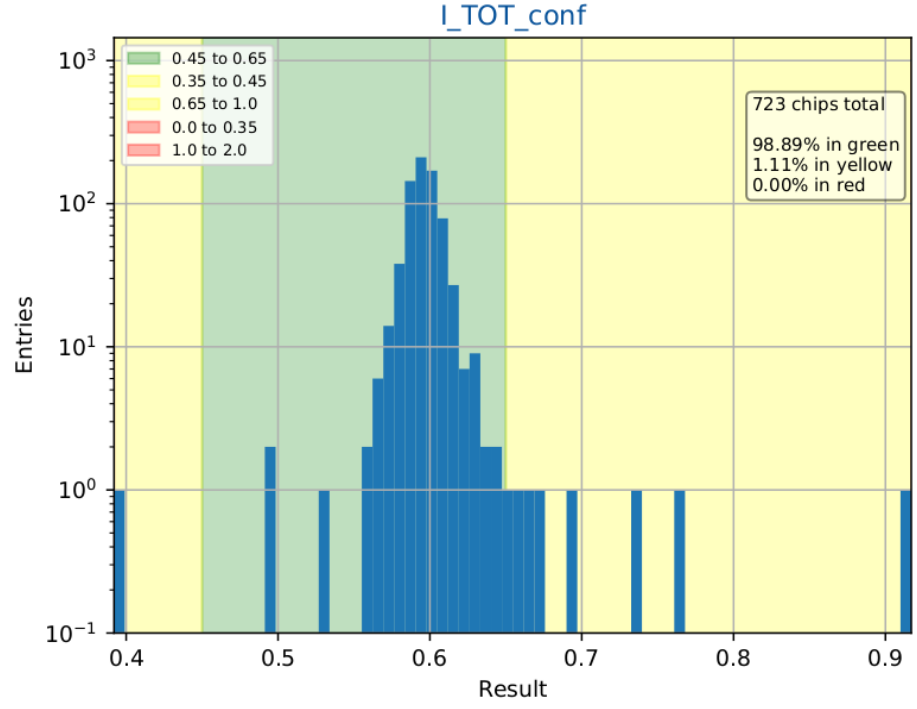
# VDDD AFTER TRIMMING

- Trim through all VOLTAGE_TRIM bits
- Select the one where VDDD is closest to 1.2V
- Measure VDDD



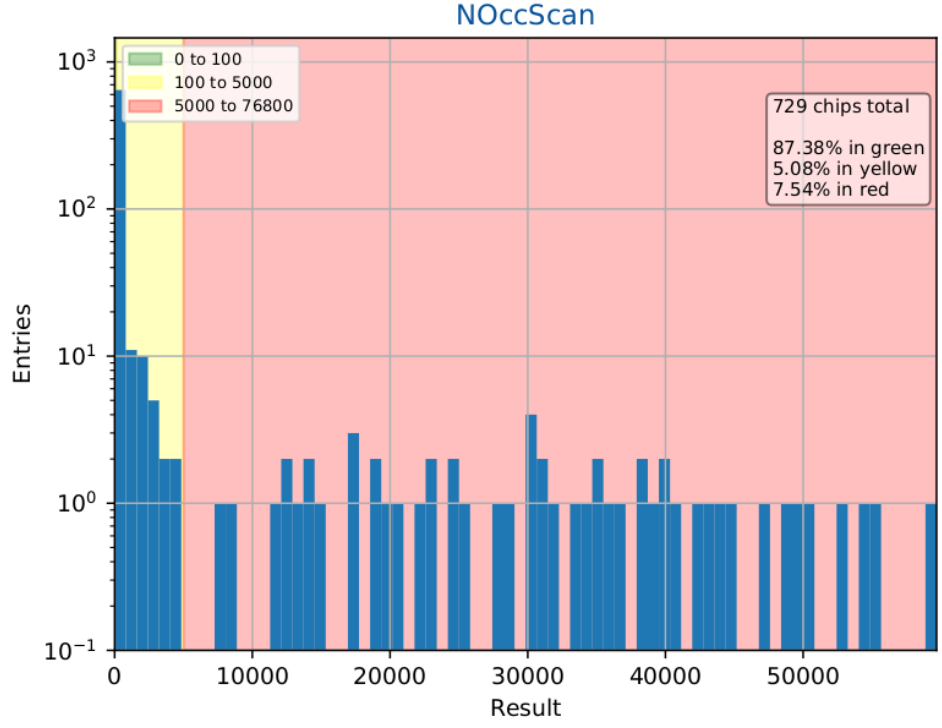
# POWER CONSUMPTION*

- Configure chip
  - Only chips that have AURORA link get results
- Measure analog and digital current consumption in LDO mode from powersupply
- V_IN = 1.7V
- Sum is proportional to total power consumption



# NOISE OCCUPANCY SCAN*

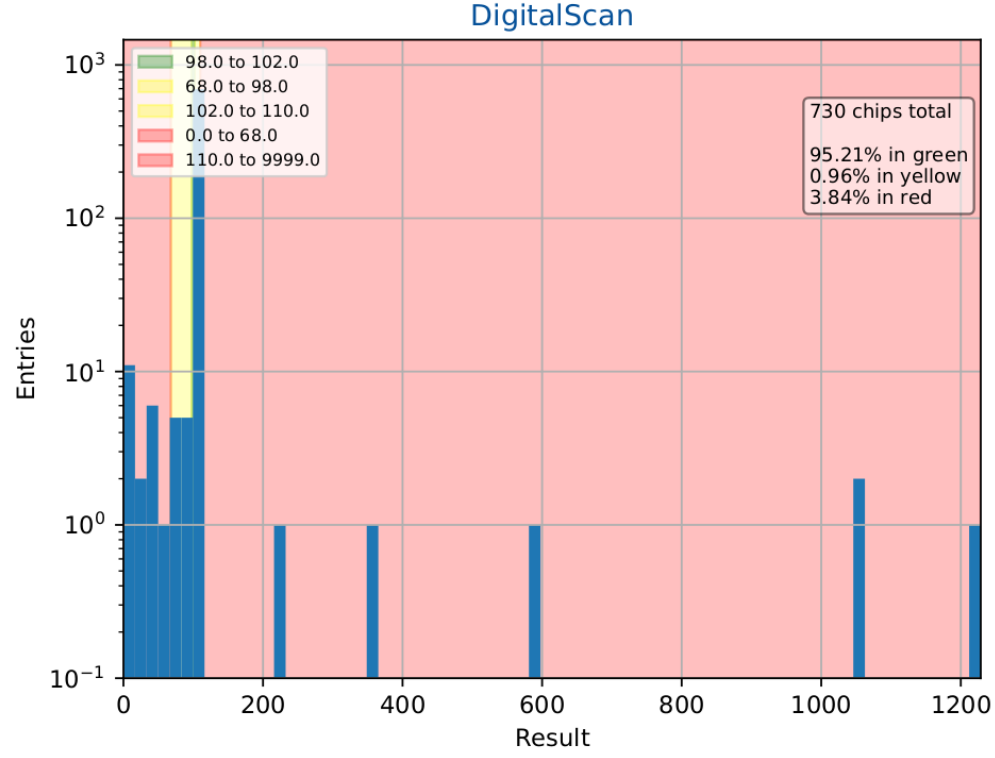
- Run noise occupancy scan over full matrix
- Cut on amount of noisy pixels
- So far ignored for total yield



# DIGITAL SCAN*

- Run digital scan over full matrix
- Cut on percentage
  occupancy / expected occupancy

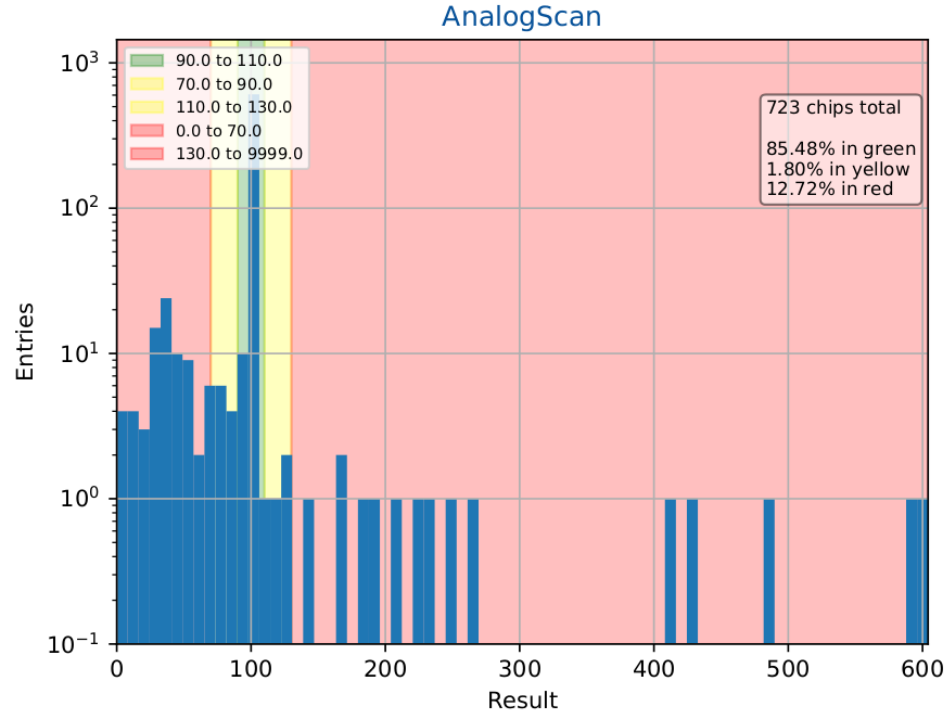
- Improvement:
  - Analyze per pixel
  - Cut on amount of good pixels



# ANALOG SCAN*

- Run analog scan over full matrix
- Cut on percentage
  occupancy / expected occupancy

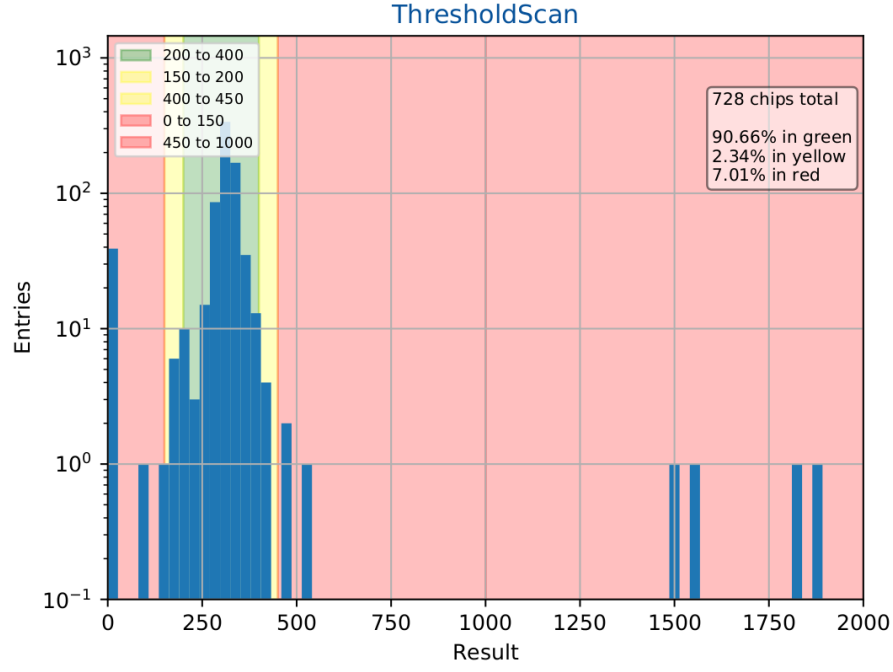
- Improvement:
  - Analyze per pixel
  - Cut on amount of good pixels



# THRESHOLD SCAN*

- Run threshold scan over full matrix
- All FEs set to ~ 3500e threshold
- Untuned
- Cut on reconstructed mean threshold

- Improvement:
  - Analyze per pixel
  - Cut on amount of good pixels



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# STATUS AND OUTLOOK

- Mean total yield as expected
- Rather high variance between wafers
- Distribute wafers in sets of 5 that have expected mean yield (?)

Still to do:

- Some improvements in analysis still to be done
- More wafers to probe
- Test and ship out other needle cards
- Integration into ITk Production Database

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# Thank you!

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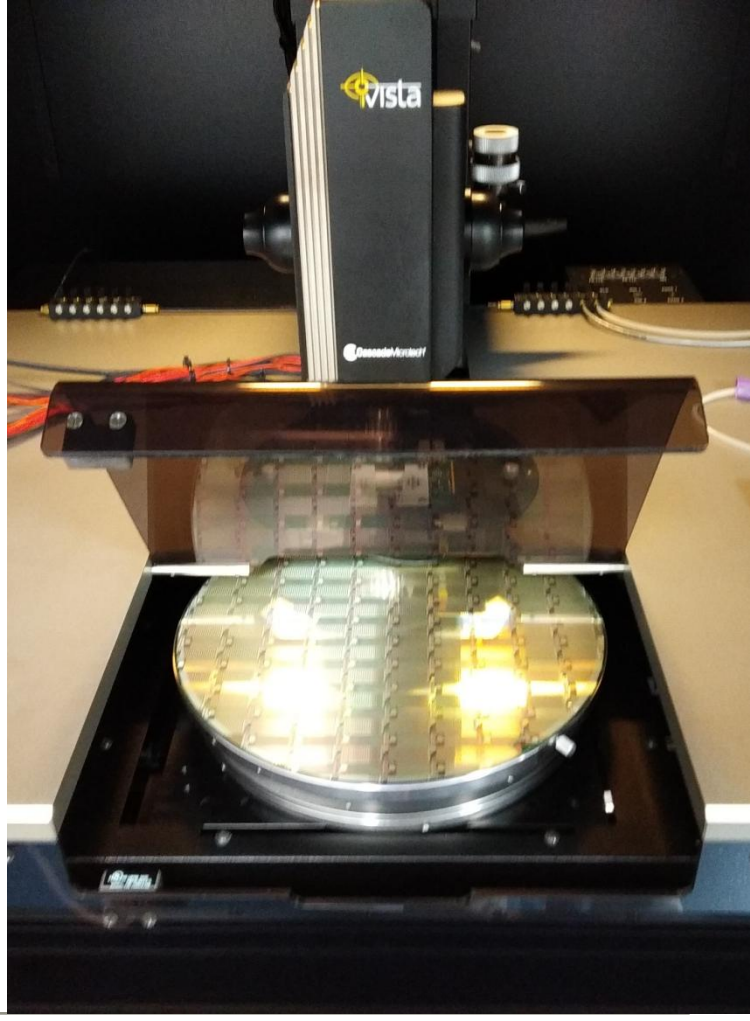
# OVERVIEW

- Test procedure finalized
- Script seems sufficiently stable now
- Probing all available wafers:
  - 10 + 14 wafers from Lot 1
  - 1 wafer from Lot 2
- First results look as expected

- Working on interface to ITk Production Database



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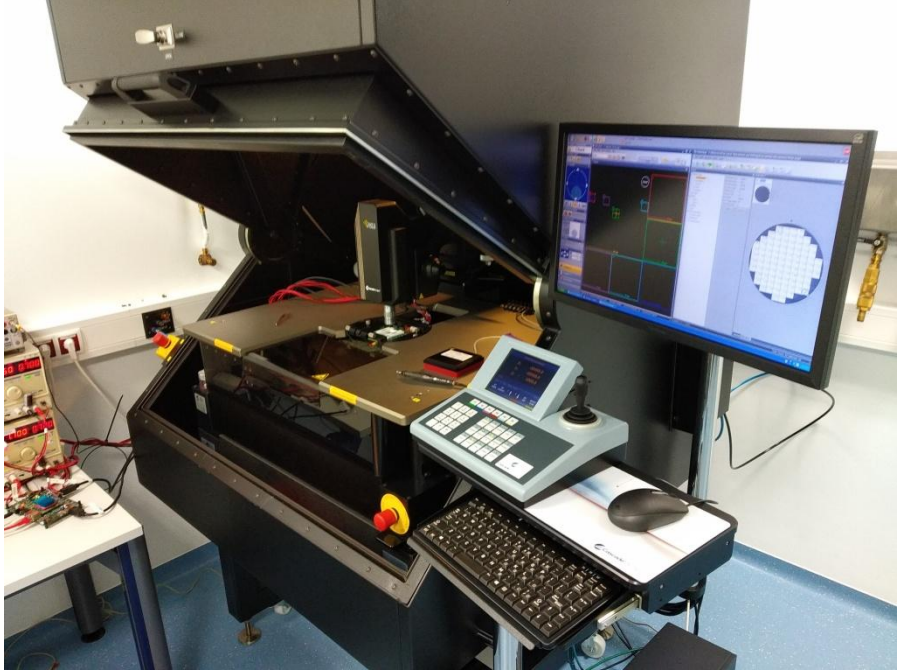
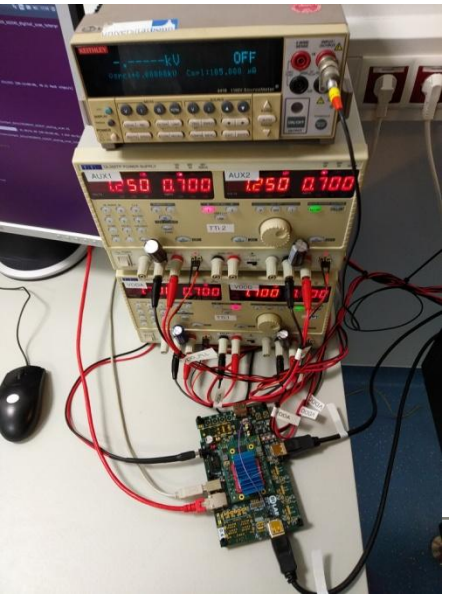
# SETUP

- Cascade Microtech (formerly Karl Suss)
  PA-300-II semi-automatic 300mm probe station
- Generic LV power supplies (TTi)
- Keithley SMU for analog measurements





- Probe card connected to BDAQ53 readout system
- Connection to BDAQ53 on one lane at 640 Mbit/s
- BDAQ53 software (v0.10.0, to be released shortly)
- Communication with hardware based on basil
  - Easy to implement / add different devices (Power supplies, SMUs, probe stations) as long as it has some kind of documented interface

# PROBE CARD

- Probe card modifications fixed
  - Standard SCC mods: PLL_RESET – POR
  - Two additional transistors to switch between Shunt- and LDO modes

- 11 cards produced, about ready to be distributed
  - 3 for CERN, one already received
  - 2 for Glasgow
  - 2 for Torino
  - 1 for LBNL

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# TIME

- Minimum goal: Keep total time for wafer < 24h to be able to probe 1 wafer / day
- Right now, a working chip takes about 14min (Shunt mode)
  - 14 min * 89 chips = 21h
  - Broken chips can take anything between 1min (short) or up to 17 min (retry communication)
- **Total time from experience ≈ 19h**

- Still potential for speedup
  - Faster scans in BDAQ53 (some ideas)
  - Analyze asynchronously
    - Analysis of scans (stuck pixel-, digital-, analog-, threshold) still done within probing script
    - Could skip and do when analyzing wafer

# EXAMPLE RESULT: VDDA