Institute of Cosmos Sciences

EXCELENCIA
MARÍA
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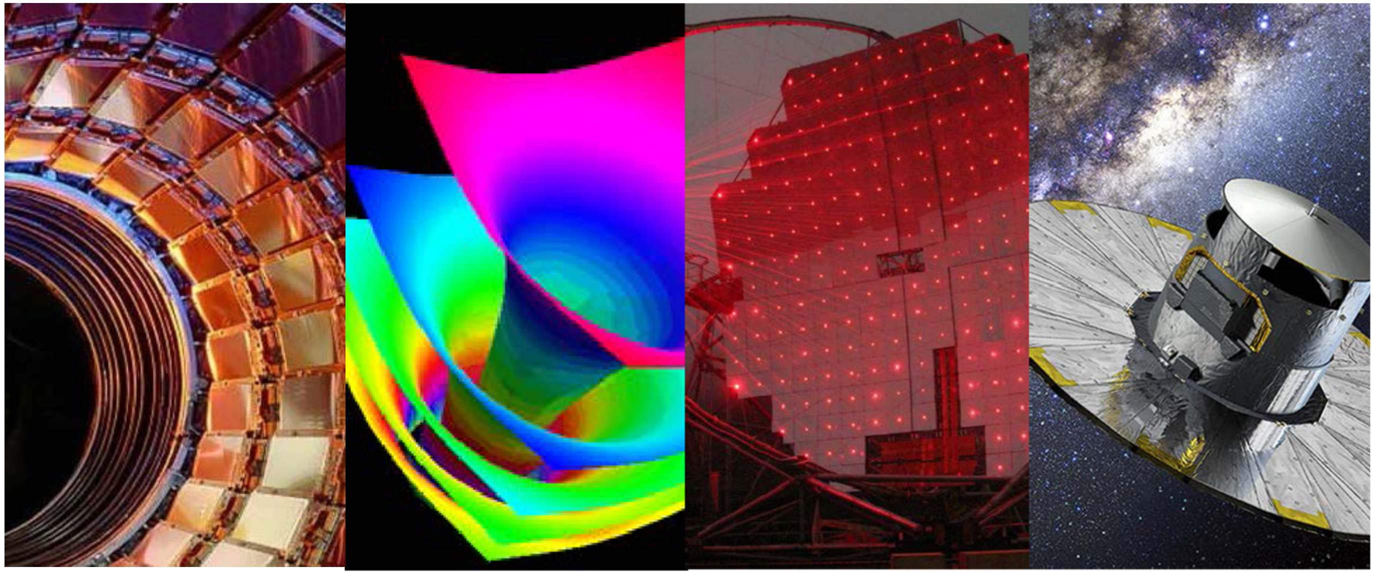

Signal processing and associated electronics

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Sense Detector School
21/06/2019

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Outlook

I. **SiPM signal**
II. Front End
III. Digitization
IV. Digital Sensors

I. The signal: SiPM electrical model

Vacuum Photomultipliers

G = 10^5 – 10^7

Cd ~ 10 pF

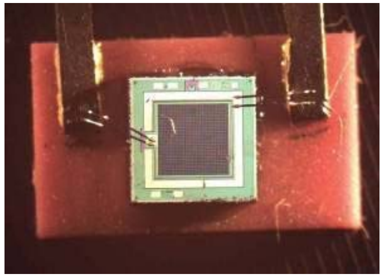
L ~ 10 nH

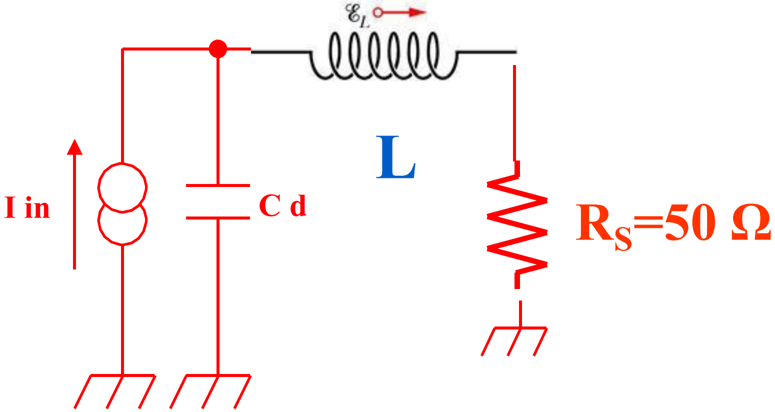
Silicon Photomultipliers

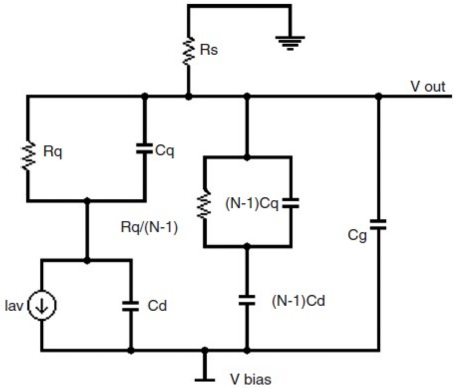
G = 10^5 – 10^7

C = 10 - 400 pF

L = 1 – 10 nH

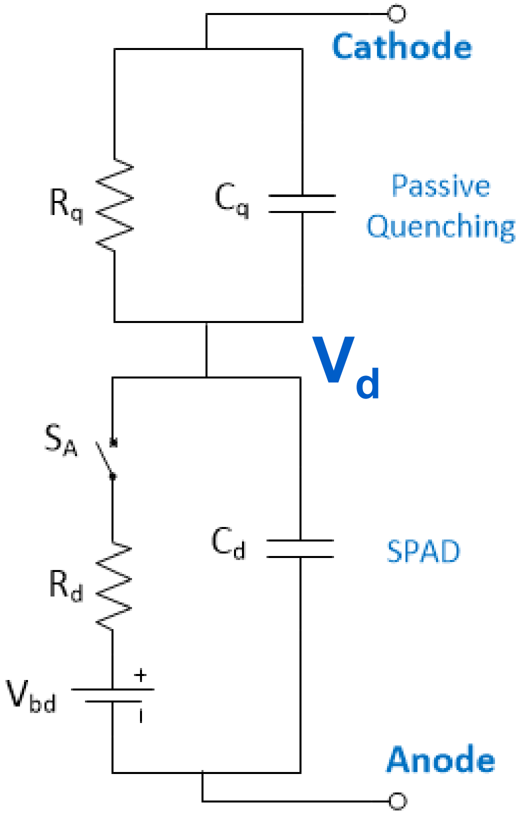






C. De LaTaille, Photodet conference, 2012

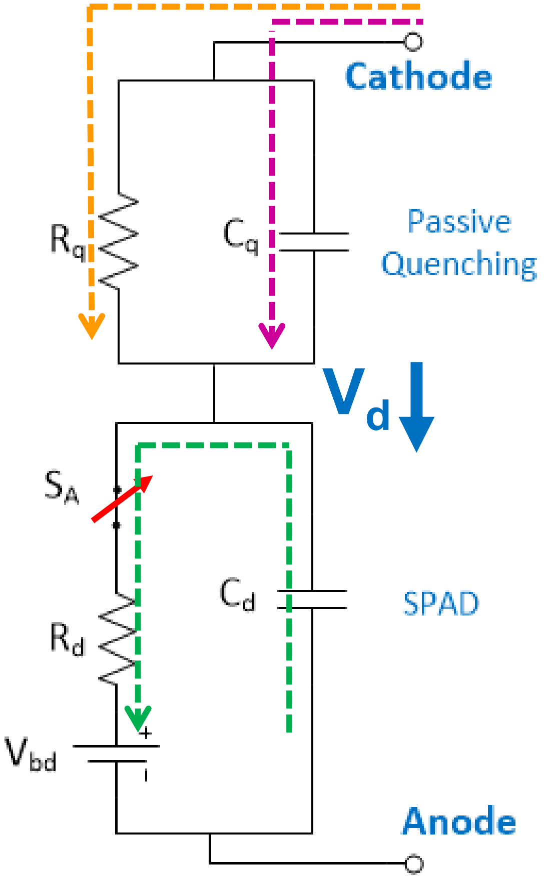
I. The signal: model of a micro-cell



- Model of a passively quenching micro-cell
  - Junction (Single-Photon Avalanche Diode, SPAD)
    - Cd: diode capacitance (Vd is the voltage across the diode)
    - Rd: junction resitance limiting avalanche current
      - Determined by the electric field in the junction and the mobility of the charge carriers
    - Vbd: breakdown voltage
    - S_A: switch modeling the avalanche (closes). Quenches (opens) when:
      - Electric field in the avalanche not large enough
        - Active quenching: lowering voltage
      - Insufficient amount of free charge carriers inside the junction at any given time
        - Passive quenching: limiting current (uA)
  - Quenching resistor
    - Rq: quenching resistance
    - Cq: parasitic capacitance of the quenching resistor

N. Otte et alt., “Silicon Photomultiplier Handbook," *Under Preparation*

I. The signal: model of a micro-cell: avalanche



1) When avalanche starts S_A closes

2) Cd discharges through Rd

- Current limited by Rd

3) Vd decreases

- I_{Rd} decreases

4) Cq is charged

- Potential cathode to anode is fixed (V_{bias})
- During avalanche micro-cell signal (current flowing into cell) is due to Cq charging
- Time constant is $\tau_d = Rd \cdot (Cq + Cd)$

4) Current also flowing through Rq

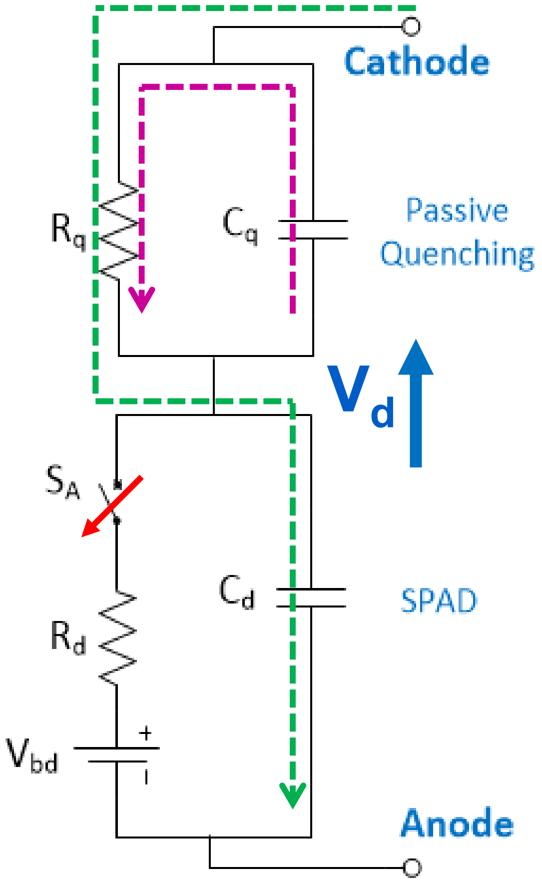
- $I_{Rq}=(V_{bias}-Vd)/Rq$

5) Avalanche stops at t_q when I_{Rd} is low enough

- If Rq is not high enough: no quenching !!!

N. Otte et alt., "Silicon Photomultiplier Handbook," *Under Preparation*

I. The signal: model of a micro-cell: recharge



1) When avalanche is quenched S_A opens

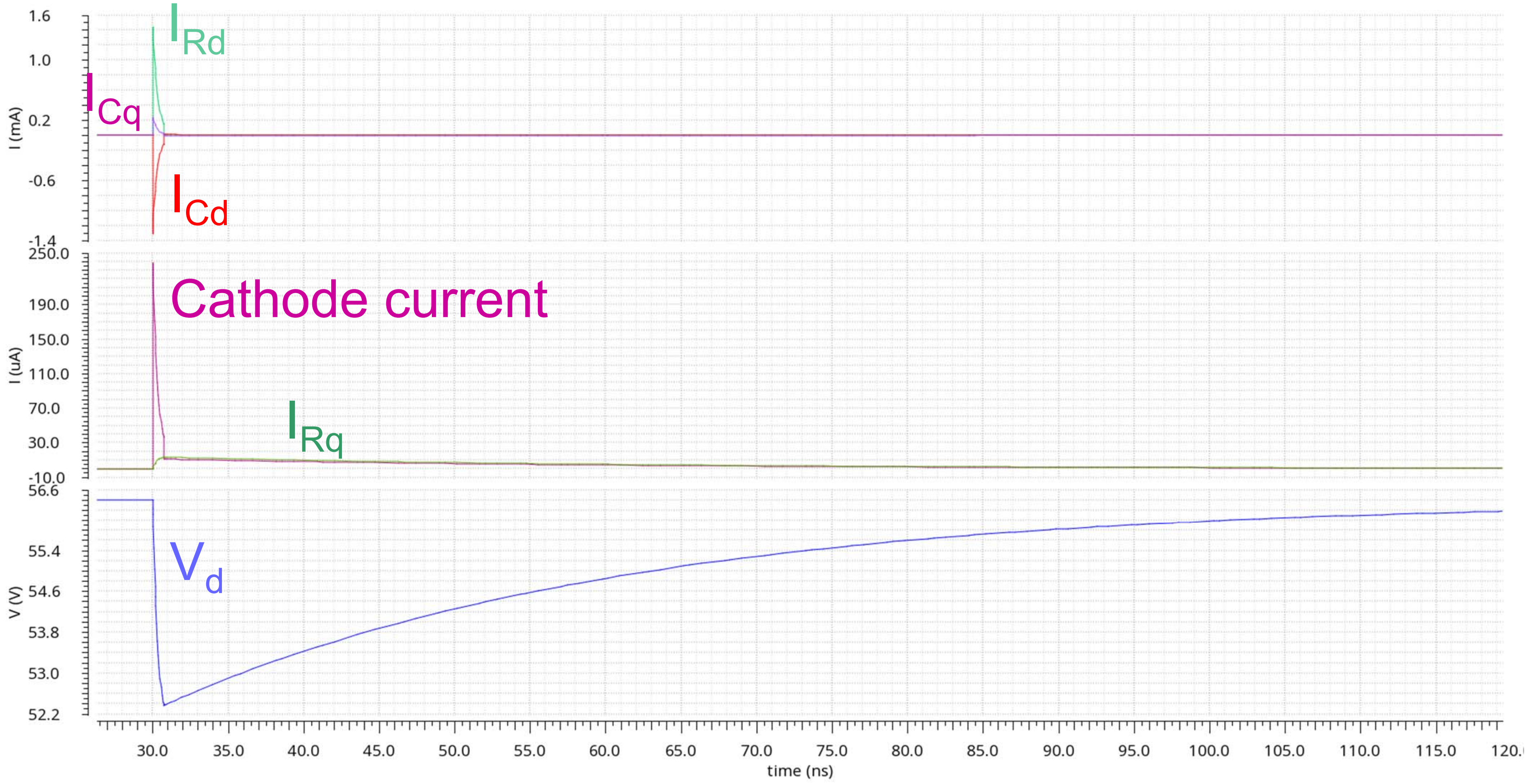
2) Cd is recharged through Rq
   - Time constant is $\tau_r = Rq \cdot (Cq + Cd)$

3) Vd increases
   - I_{Rq} decreases

4) Cq is discharged through Rq

5) Recharge ends when $Vd = V_{bias}$
   - At this point all currents are null

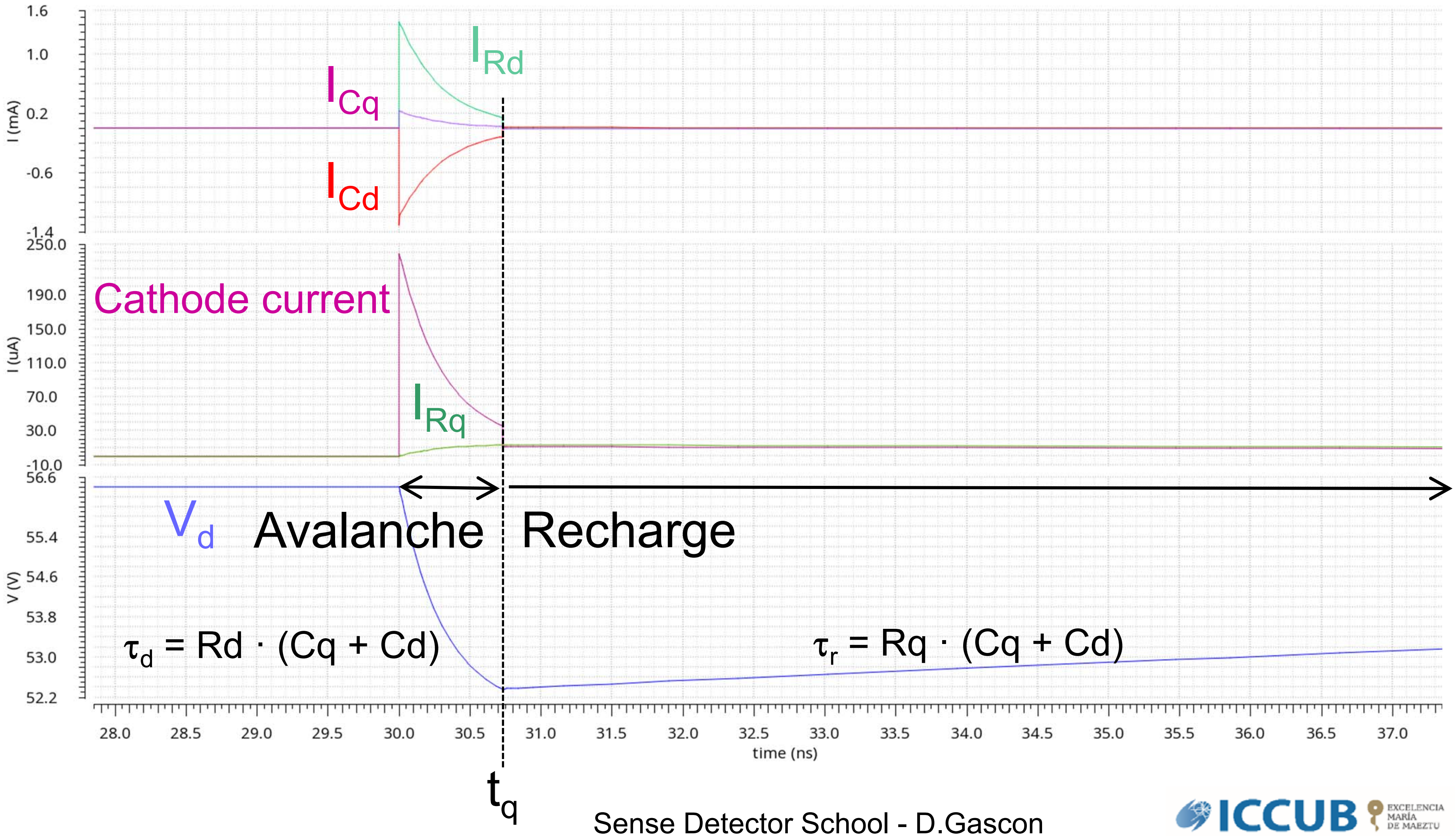
I. The signal: model of a micro-cell: simulation



- Simulation parameters: Cd=84.5 fF, Cq=16.8 fF, Rq=300.8 KΩ, Rd= 3 KΩ, Vbd=51.9 V, Vbias=Vbd+4.5V, S_A quenching current: 40 uA

I. The signal: model of a micro-cell: simulation

- Let’s zoom around quenching time t_q:

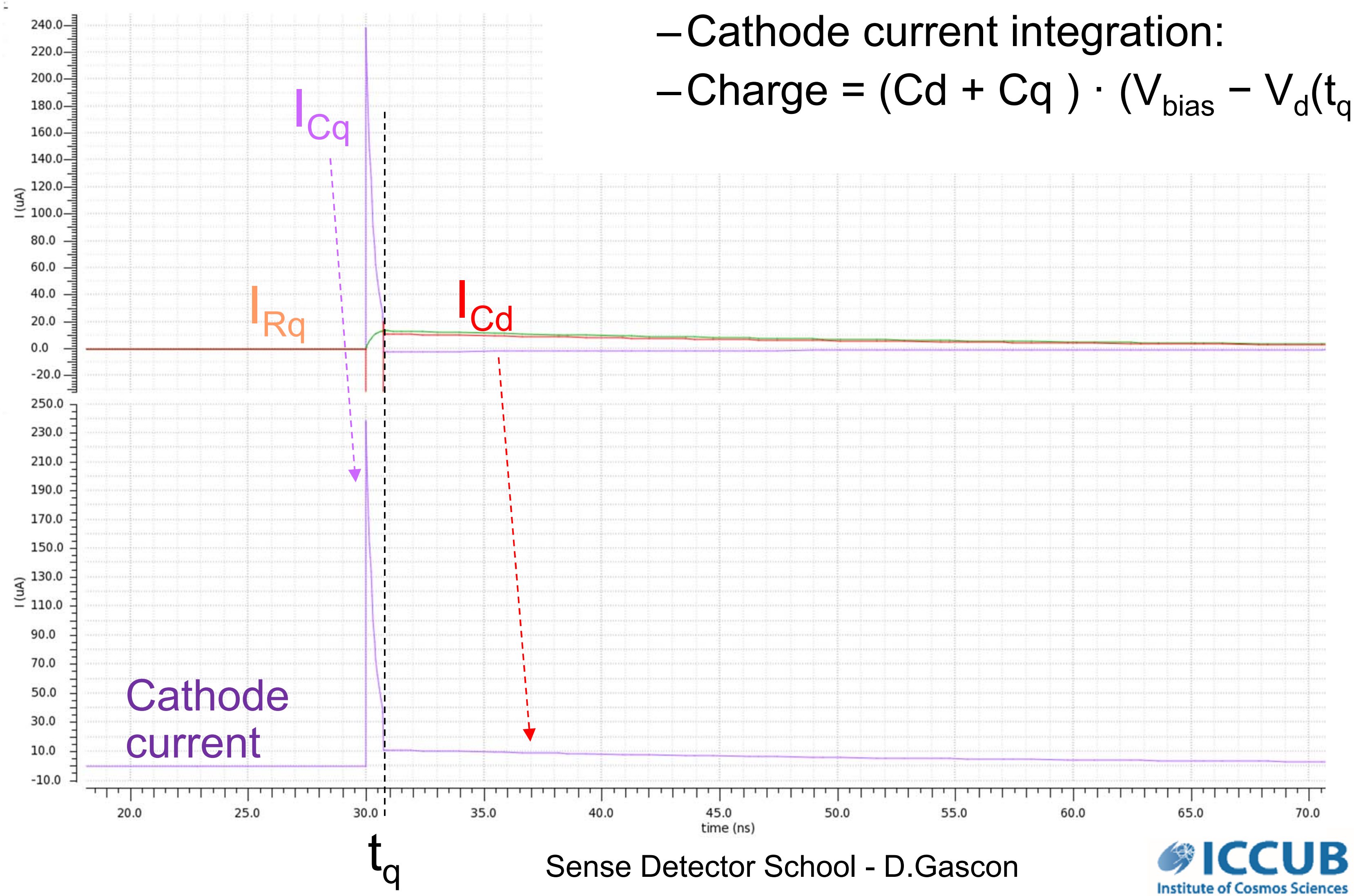


$\tau_d = Rd \cdot (Cq + Cd)$

$\tau_r = Rq \cdot (Cq + Cd)$

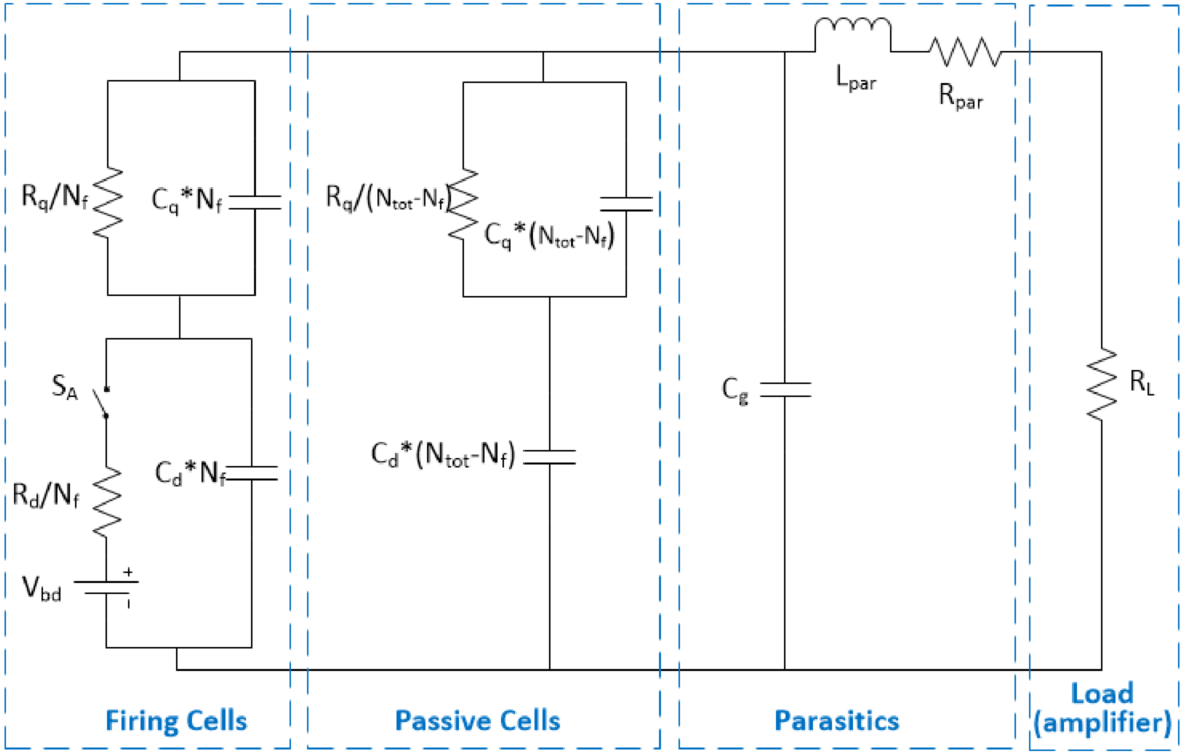
I. The signal: model of a micro-cell: simulation

- Signal-charge (gain):
  - Cathode current integration:
  - Charge = (Cd + Cq) · (V_{bias} − $V_d(t_q)$)



I. The signal: model of a complete SiPM

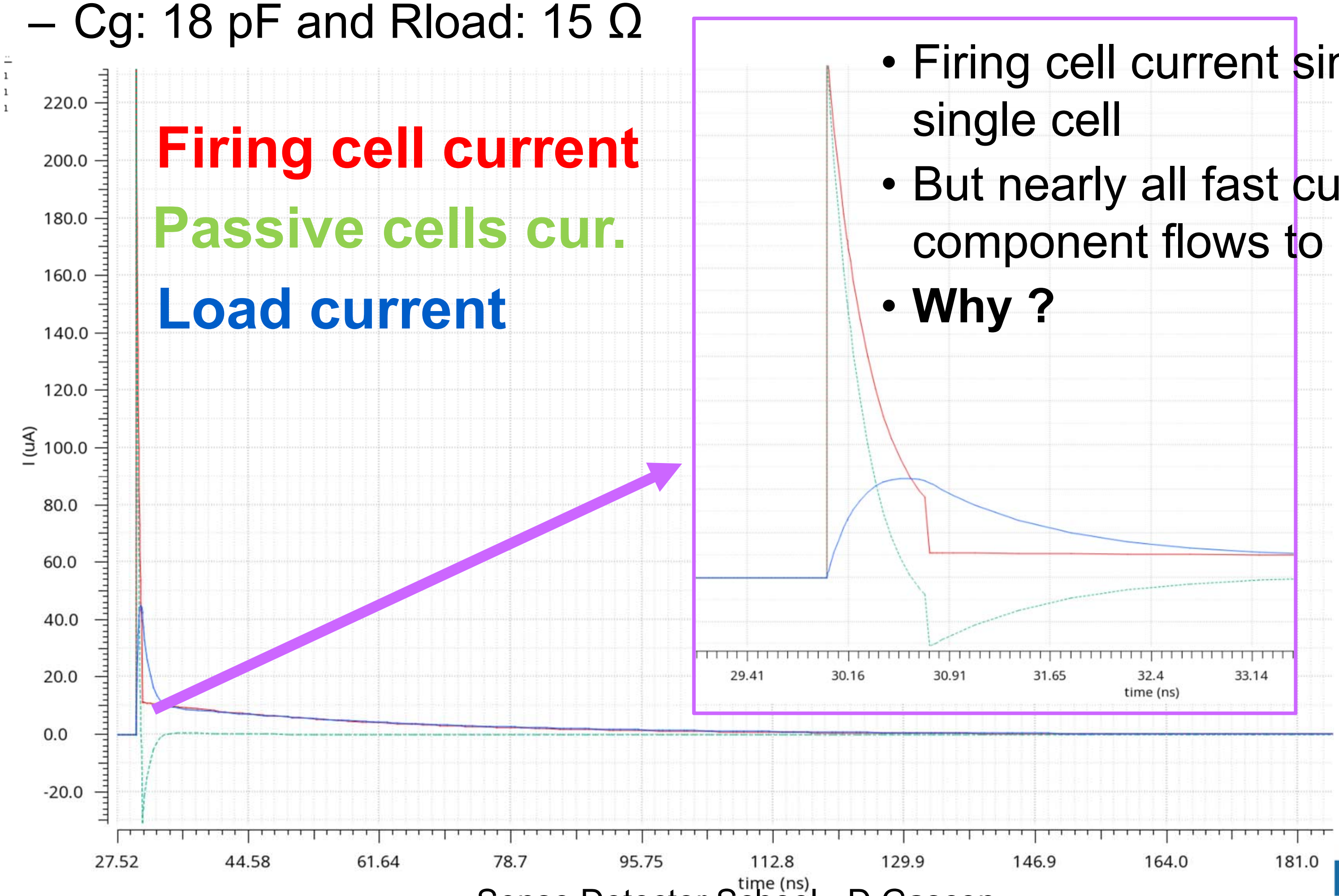
- Complete model of SiPM with N_{tot} cells:
  - Active (firing) cells (N_f)
  - Passive (not firing) cells ($N_{tot} – N_f$)
  - Parasitic components
  - Load impedance



- Parasitic elements:
  - *Cg*: interconnection parasitic capacitance
  - *Rpar*: interconnection parasitic resistance
  - *Lpar*: interconnection parasitic inductance
- Load:
  - Usually the input impedance of the front end amplifier
  - Or just a resistor
    - For instance a 50 Ω scope

I. The signal: model of a complete SiPM

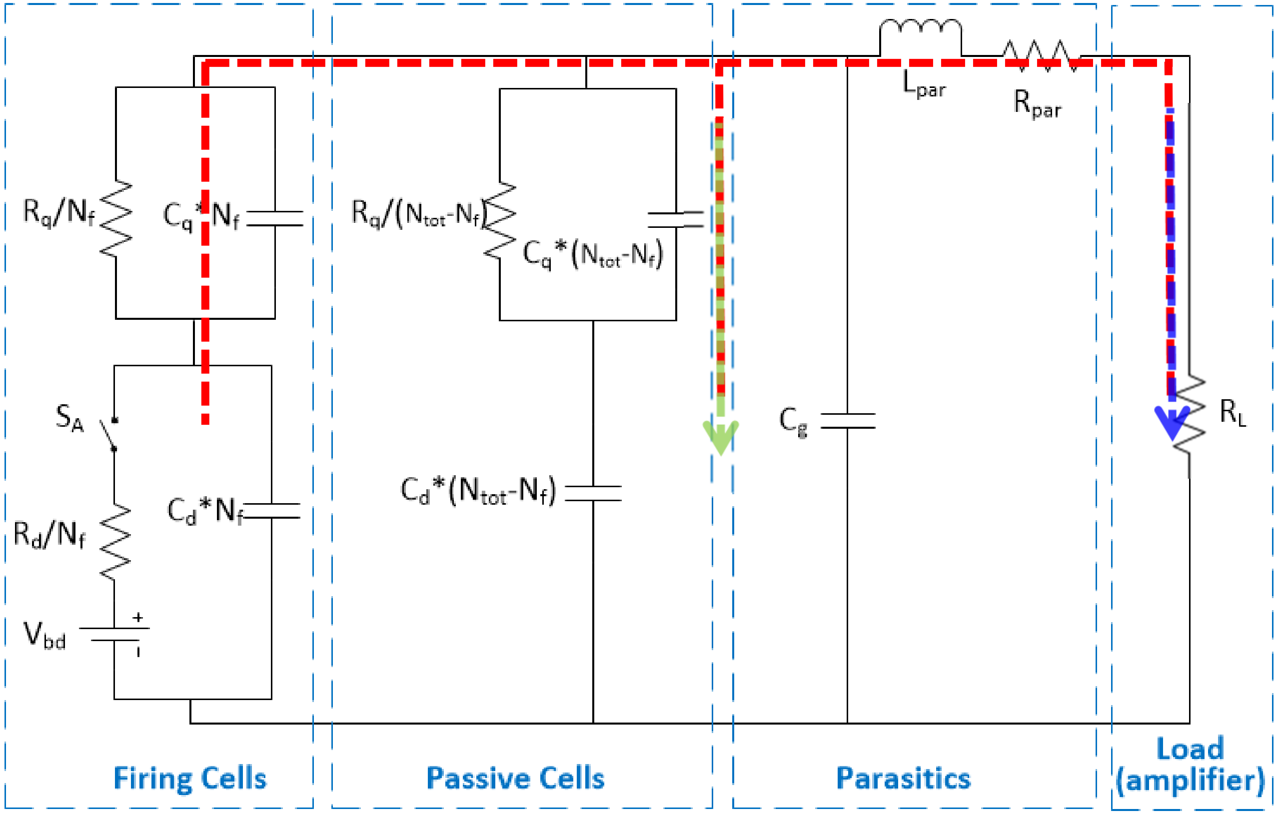
- Simulation for a typical 3x3 mm^2 SiPM with 3600 cells:
  - 1 firing cell. Size: 50 µm similar parameters as previous simulations
  - Cg: 18 pF and Rload: 15 Ω



- Firing cell current similar as for single cell
- But nearly all fast current component flows to passive cells
- **Why ?**

I. The signal: model of a complete SiPM

- Passive cells and load impedance form a low pass filter !
  - We are sensing the current or the voltage on R_L
  - Passive cells and parasitic capacitances create a current divider with R_L
  - Peak signal goes with $Cpar^{-1}$



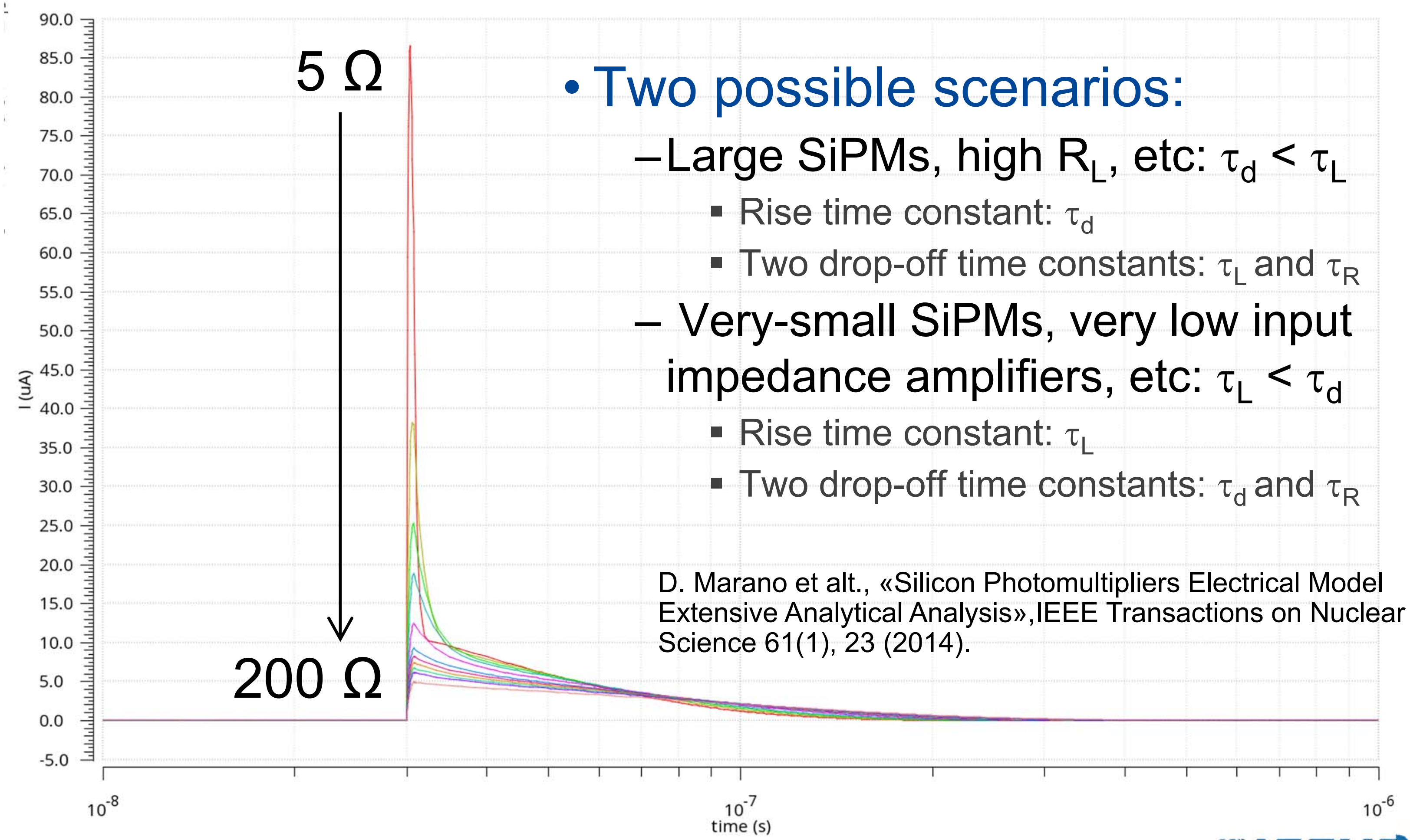
Low pass filter time constant:

$$\tau_L \approx R_L \cdot N_{tot} \cdot (Cq \,//\, Cd)$$

* *Approximate: we should include also Cg here*

I. The signal: model of a complete SiPM

- The signal (load current) shape and amplitude depends on R_L
  - Peak current signal is inversely proportional to R_L

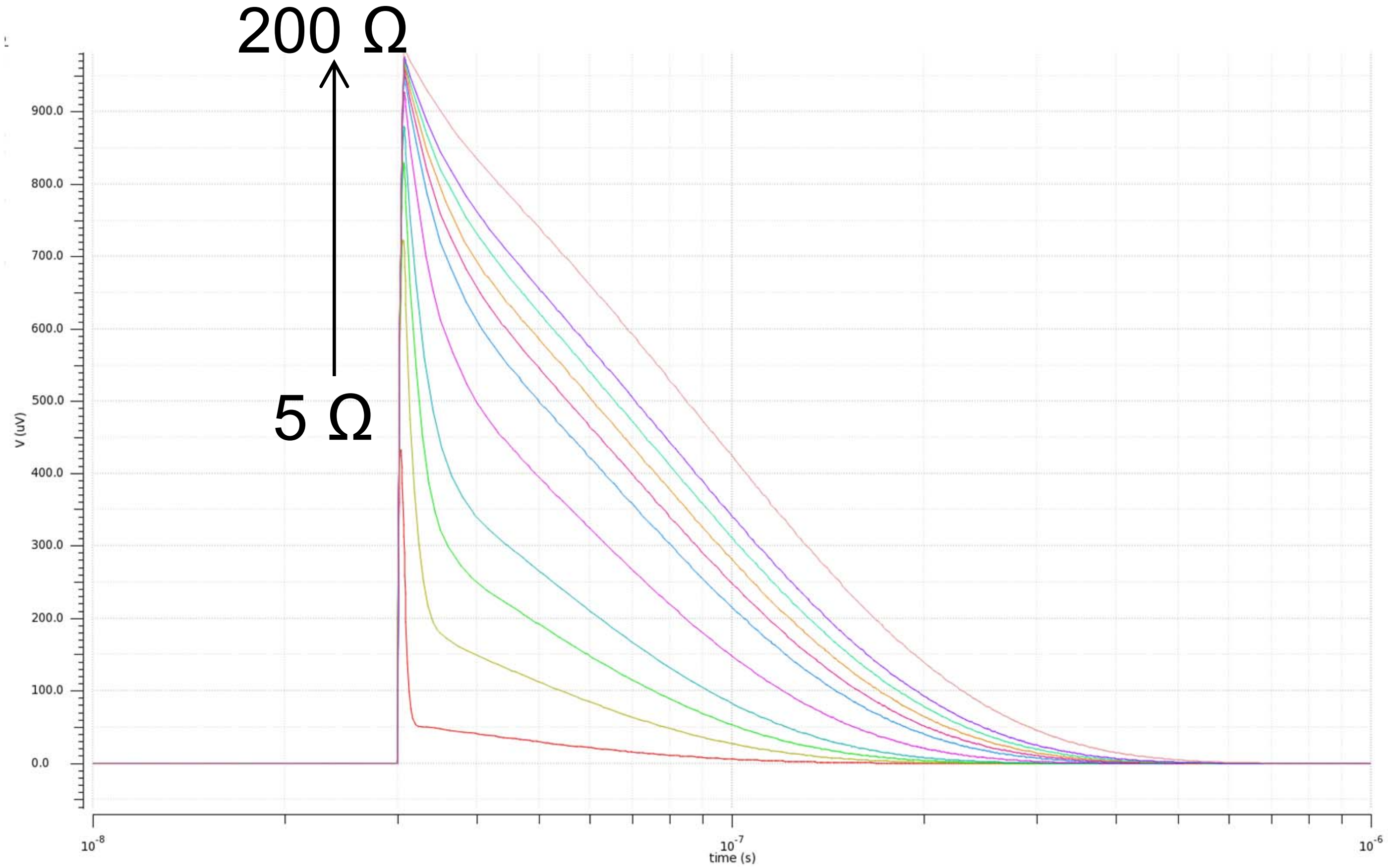


- Two possible scenarios:
  - Large SiPMs, high R_L, etc: $\tau_d < \tau_L$
    - Rise time constant: τ_d
    - Two drop-off time constants: τ_L and τ_R
  - Very-small SiPMs, very low input impedance amplifiers, etc: $\tau_L < \tau_d$
    - Rise time constant: τ_L
    - Two drop-off time constants: τ_d and τ_R

D. Marano et alt., «Silicon Photomultipliers Electrical Model Extensive Analytical Analysis»,IEEE Transactions on Nuclear Science 61(1), 23 (2014).

I. The signal: model of a complete SiPM

- If we sense the load voltage the situation is a little bit different:
  - Shape also depends on R_L (long recovery times for large R_L)
  - But the amplitude is now proportional to R_L



I. The signal: analytical model (large SiPM)

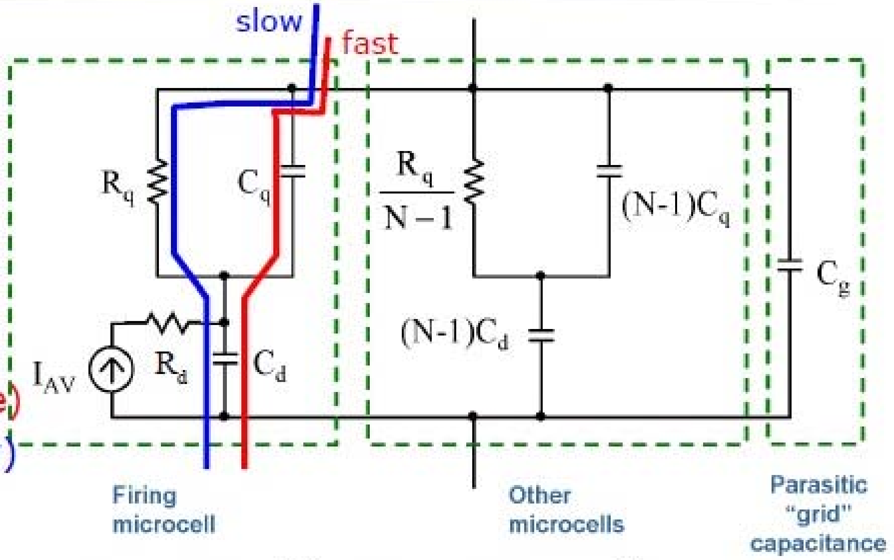
Single cell model → $(R_d||C_d)+(R_q||C_q)$

SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

Signal = slow pulse ($\tau_{d\ (rise)}, \tau_{q\text{-}slow\ (fall)}$) +

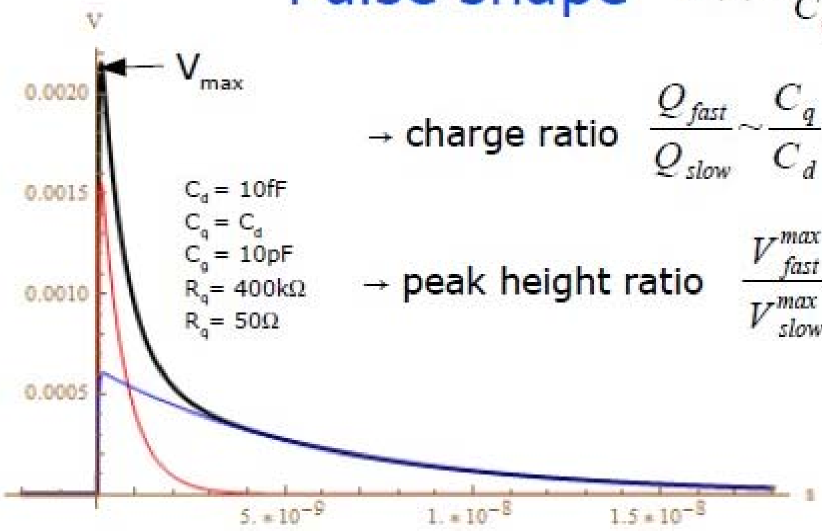
+ fast pulse ($\tau_{d\ (rise)}, \tau_{q\text{-}fast\ (fall)}$)

- $\tau_{d\ (rise)} \sim R_d(C_q+C_d)$
- $\tau_{q\text{-}fast\ (fall)} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{q\text{-}slow\ (fall)} = R_q\ (C_q+C_d)$ (slow; cell recovery)



Pulse shape

$$V(t) \simeq \frac{Q}{C_q+C_d}\left(\frac{C_q}{C_{tot}} e^{\frac{-t}{\tau_{FAST}}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q+C_d} e^{\frac{-t}{\tau_{SLOW}}}\right)$$



→ charge ratio $\frac{Q_{fast}}{Q_{slow}} \sim \frac{C_q}{C_d}$

→ peak height ratio $\frac{V^{max}_{fast}}{V^{max}_{slow}} \sim \frac{C_q^2 R_q}{C_d C_{tot} R_{load}}$

increasing with Rq and $1/R_{load}$

(and Cq of course)

1) Peak V or I signal goes with C^{-1}

2) Peak I signal goes with R^{-1}

Increasing C_q/C_d or/and R_q/R_{load}

→ spike enhancement

→ better timing

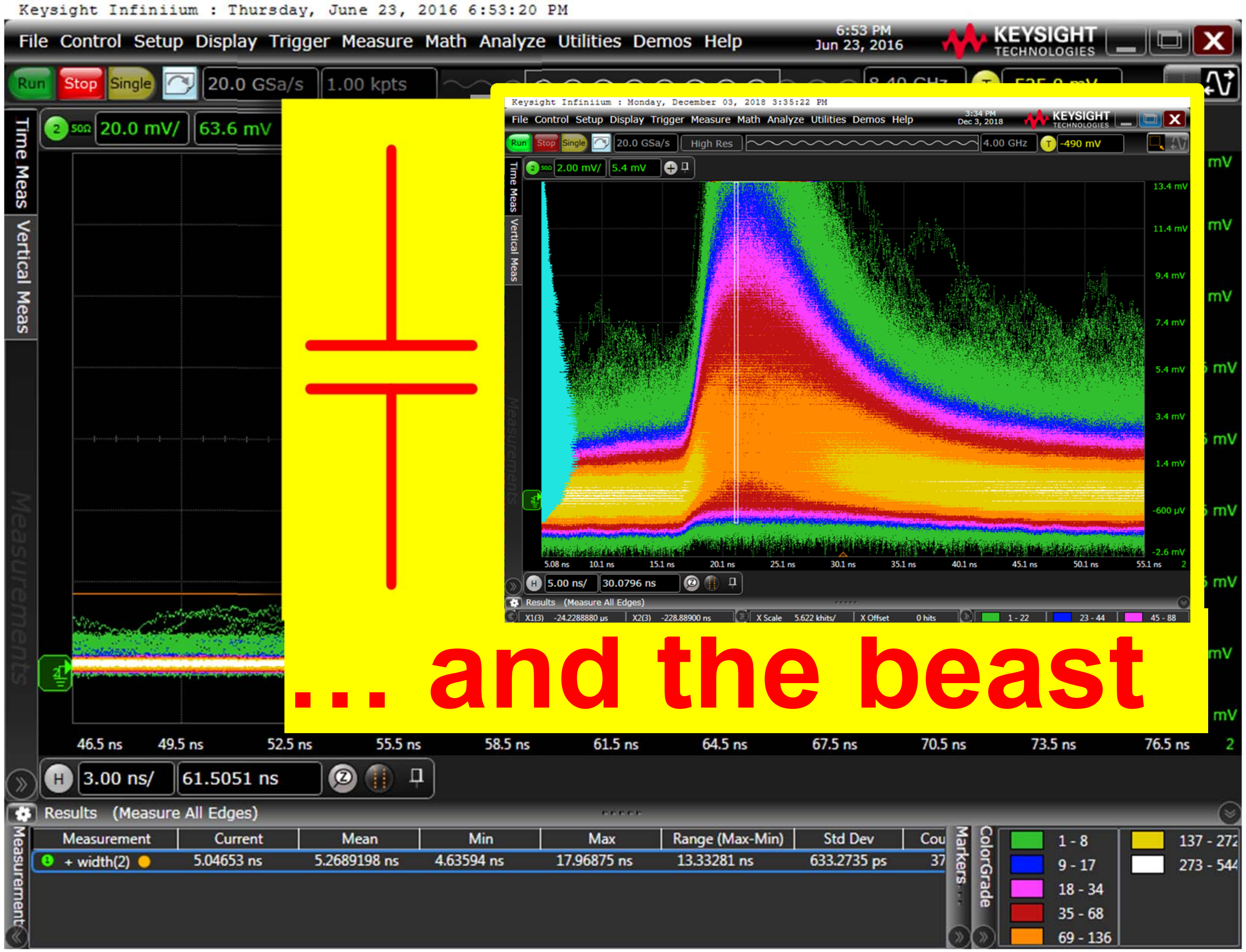
3) Fast vs slow component

G.Collazuol - PhotoDet 2012

I. References on SiPM modelling and FE electronics

- D. Marano, M. Belluso, G. Bonanno et alt., «Silicon Photomultipliers Electrical Model Extensive Analytical Analysis»,IEEE Transactions on Nuclear Science 61(1), 23 (2014). DOI 10.1109/TNS.2013.2283231
- G. Collazoul,” The SiPM Physics and Technology”, Photodet 2012, https://indico.cern.ch/event/164917/contributions/1417121/attachments/198512/278663/PhotoDet12_-_collazuol_-_v3.pdf
- S. Seifert, "Simulation of silicon photomultiplier signals", IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3726-3733, Dec. 2009.
- F. Acerbi, S. Gundacker. Understanding and simulating SiPMs (2018). DOI 10. 1016/j.nima.2018.11.118. URL https://www.sciencedirect.com/science/article/pii/S0168900218317704
- F. Corsi et al., "Modelling a Silicon Photomultiplier (SiPM) as a Signal Source for Optimum Front-End Design", Nucl. Instr. and Meth. in Phys. Res., vol. A572, pp. 416-418, 2007
- F. Ciciriello, F. Corsi, F. Licciulli, C. Marzocca, G. Matarrese et al., "Accurate Modeling of SiPM Detectors Coupled to FE Electronics for Timing Performance Analysis", Nucl. Instr. and Meth. in Phys. Res., vol. A 718, pp. 331-333.
- F. Ciciriello, F. Corsi, F. Licciulli, C. Marzocca and G. Matarrese, “Design of Current Mode Front-End Amplifiers with Optimal Timing Performance for High-gain Photodetectors,” in European Conference on Circuit Theory and Design, 2015.
- C. de la Taille, “SiPM readout electronics overview”, Photodet 2012, https://indico.cern.ch/event/164917/contributions/1417117/attachments/198508/278657/1-cdlt_Photodet2012.pdf

I. The signal: the beauty and the beast…



Keysight Infiniium : Thursday, June 23, 2016 6:53:20 PM

Keysight Infiniium : Monday, December 03, 2018 3:35:22 PM

… and the beast

Results (Measure All Edges)

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Cou
+ width(2)	5.04653 ns	5.2689198 ns	4.63594 ns	17.96875 ns	13.33281 ns	633.2735 ps	37

X1(3) -24.2288880 µs

X2(3) -228.88900 ns

X Scale 5.622 khits/

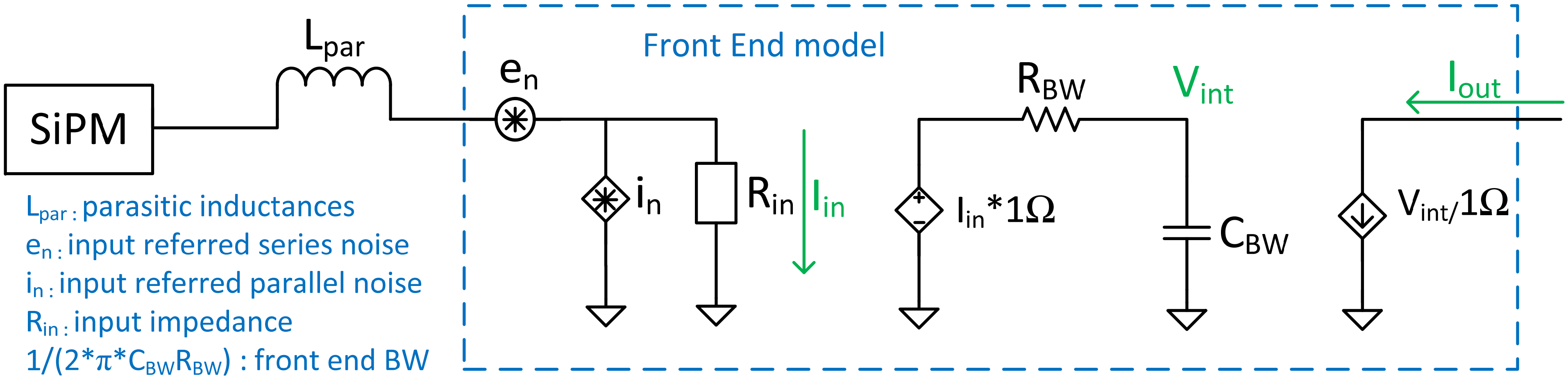
X Offset 0 hits

Outlook

I. SiPM signal
II. Front End
III. Digitization
IV. Digital Sensors

II. Front end model

- A more detailed model of the front end
  - Not just an impedance
- Need to include also noise and bandwidth to evalute resolution
  - Charge (spectrum) and time

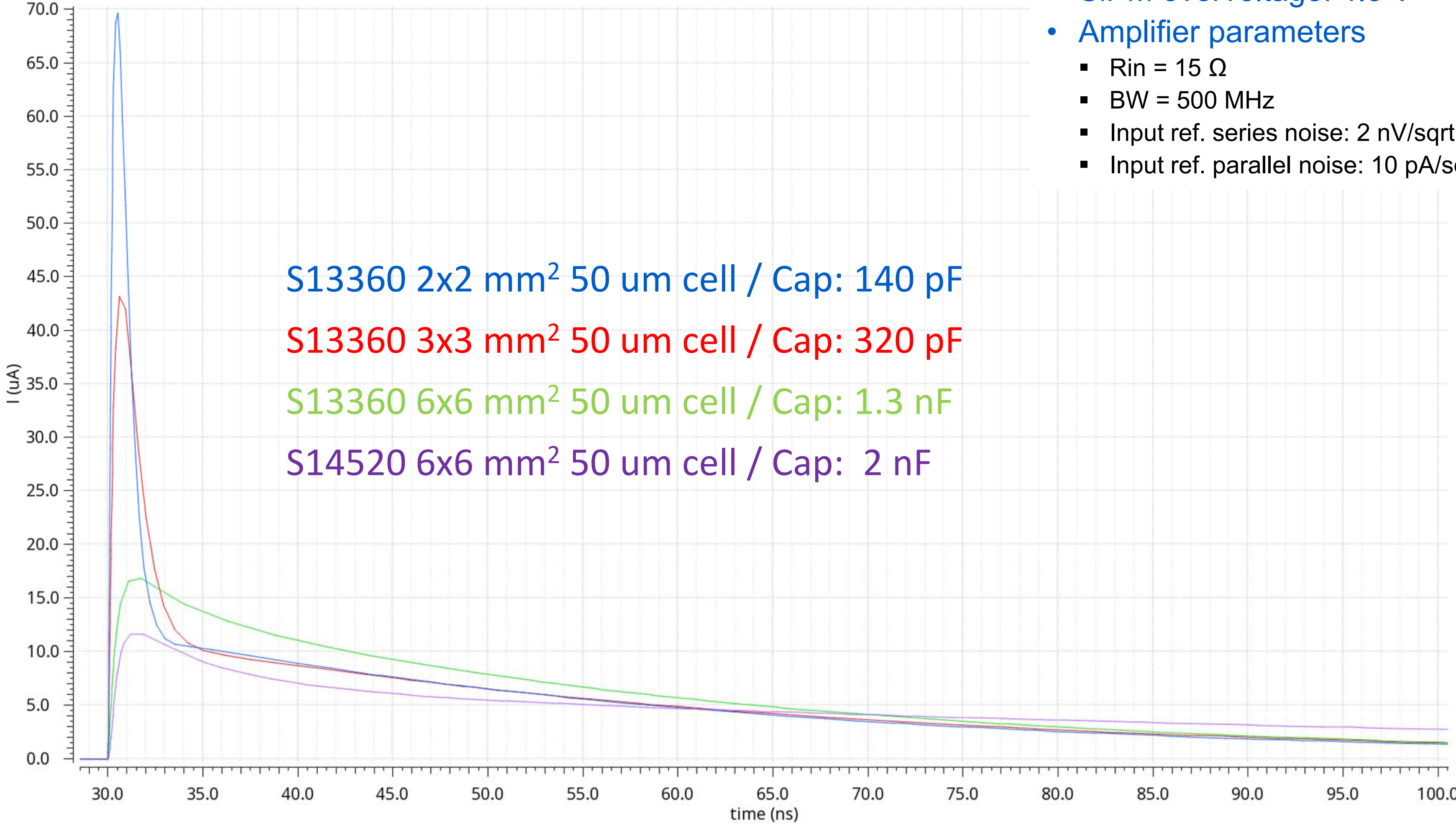


L_{par} : parasitic inductances
e_n : input referred series noise
i_n : input referred parallel noise
R_{in} : input impedance
$1/(2*\pi*C_{BW}R_{BW})$: front end BW

II. SiPM signal with FE: shape

- Single cell signal for different SiPMs
  - *Peak V or I signal goes with C^{-1}!*

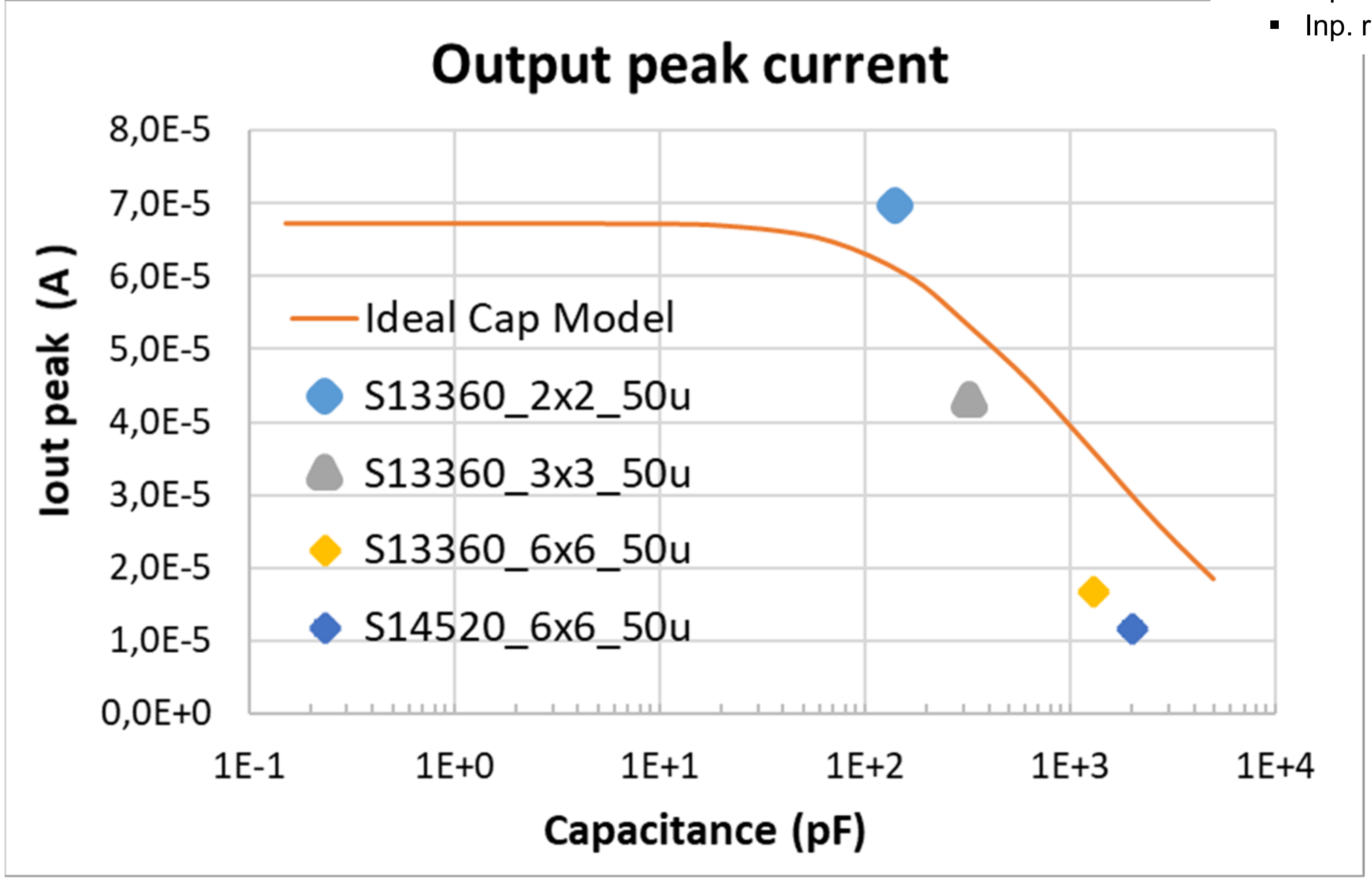
- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Input ref. series noise: 2 nV/sqrt(/Hz)
  - Input ref. parallel noise: 10 pA/sqrt(/Hz)



II. SiPM signal with FE : peak output signal

- Output peak current for several SiPMs
  - Compared to simplied ideal detector (capacitor + I source)
    - For C<100 pF (with Rin=15 Ω) current flows into amplifier
    - Trend C^{-1} well described for higher capacitances
  - SiPM capacitance assigned from datasheet ≠ effective cap

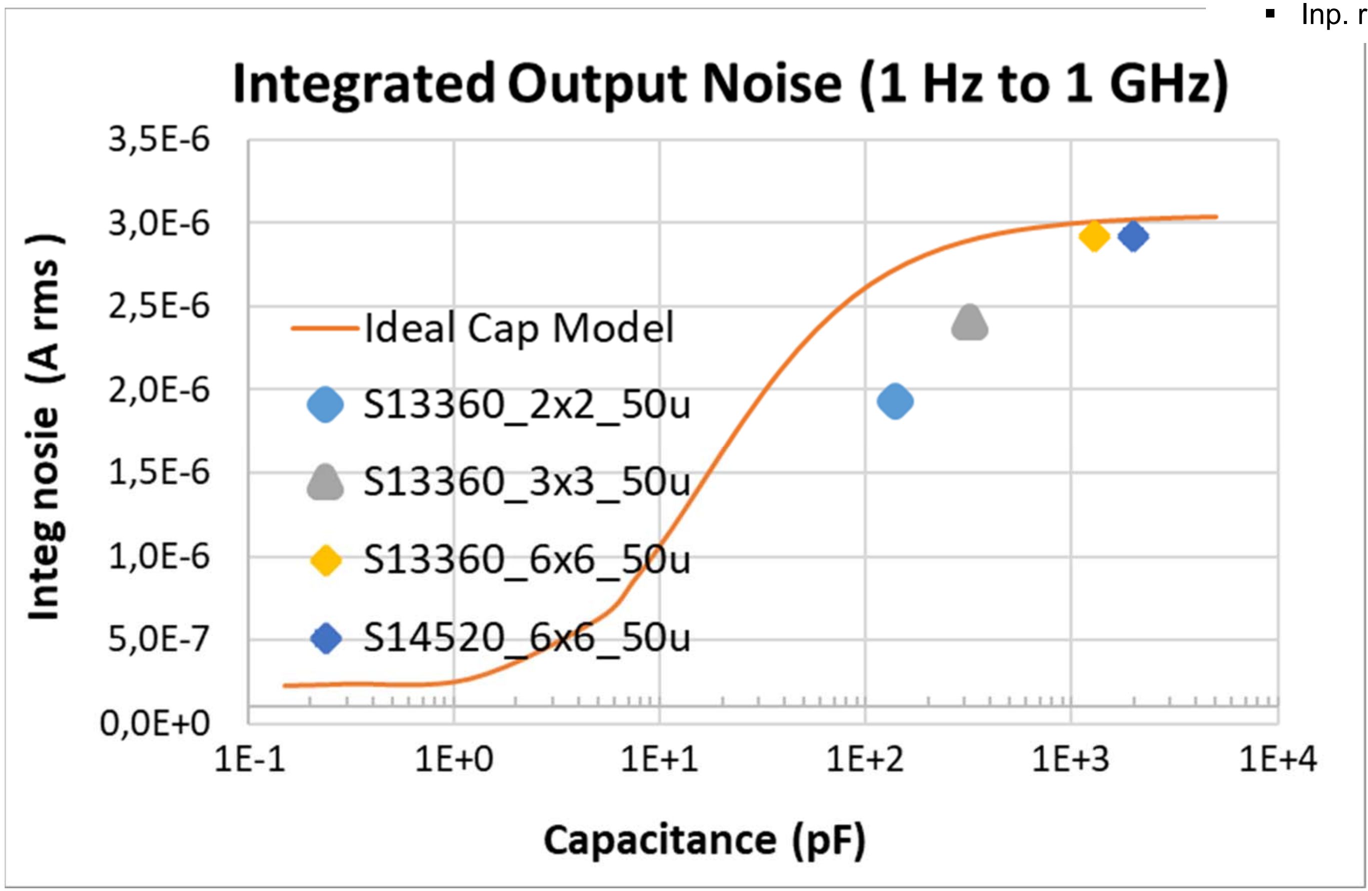
- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)



II. SiPM signal with FE : output noise

- Integrated output noise current for several SiPMs
  - Compared to simplied ideal detector (capacitor + I source)
  - SiPM capacitance assigned from datasheet ≠ effective cap
    - “Effective capacitance” (complex part of impedance at HF) is typically smaller than datasheet capacitance

- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)



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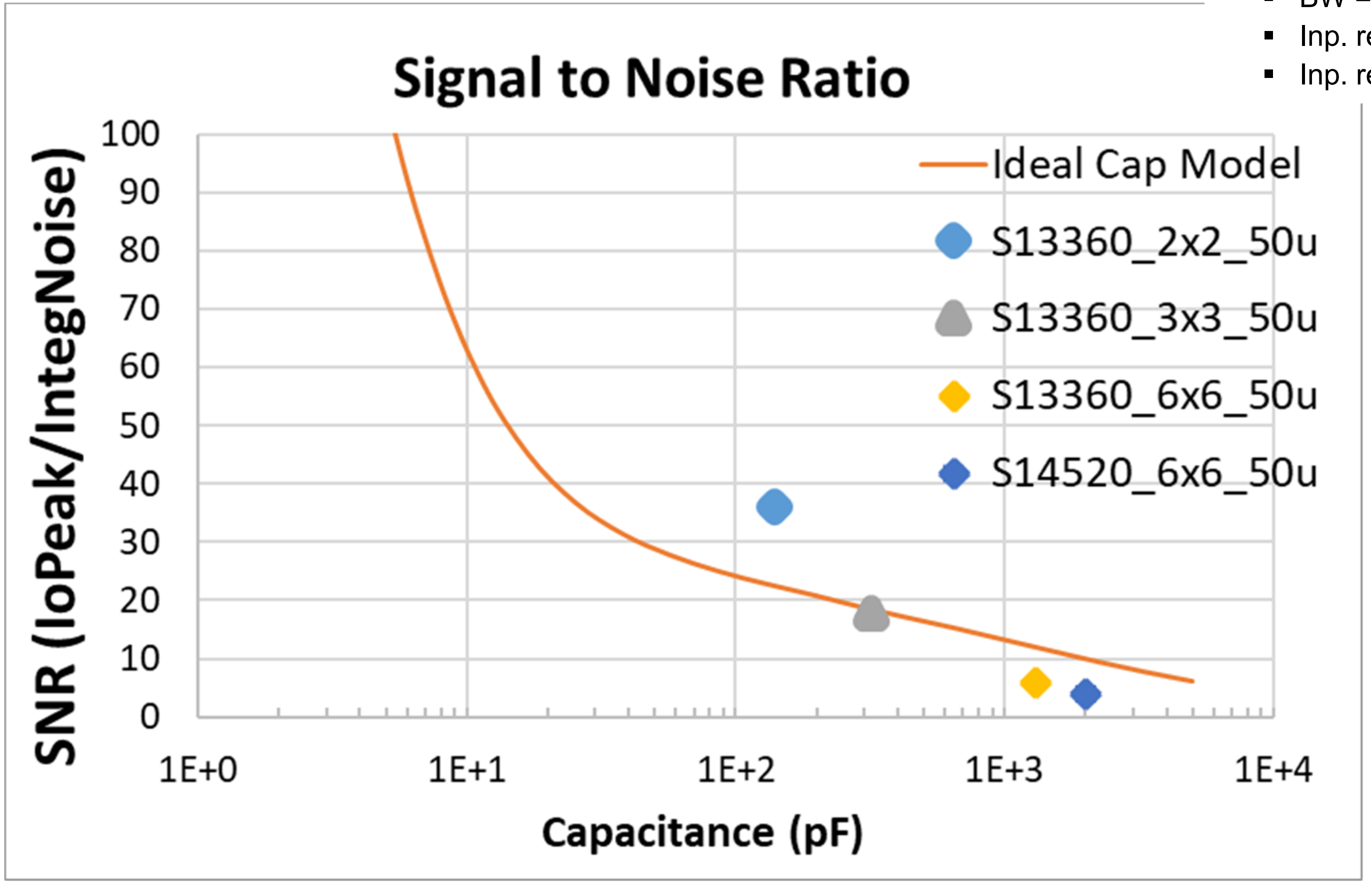
II. SiPM signal with FE : peak signal to noise ratio (SNR)

- Signal to Noise ratio can be computed as the ratio of previous results:
  - Output peak current divided by integrated output noise

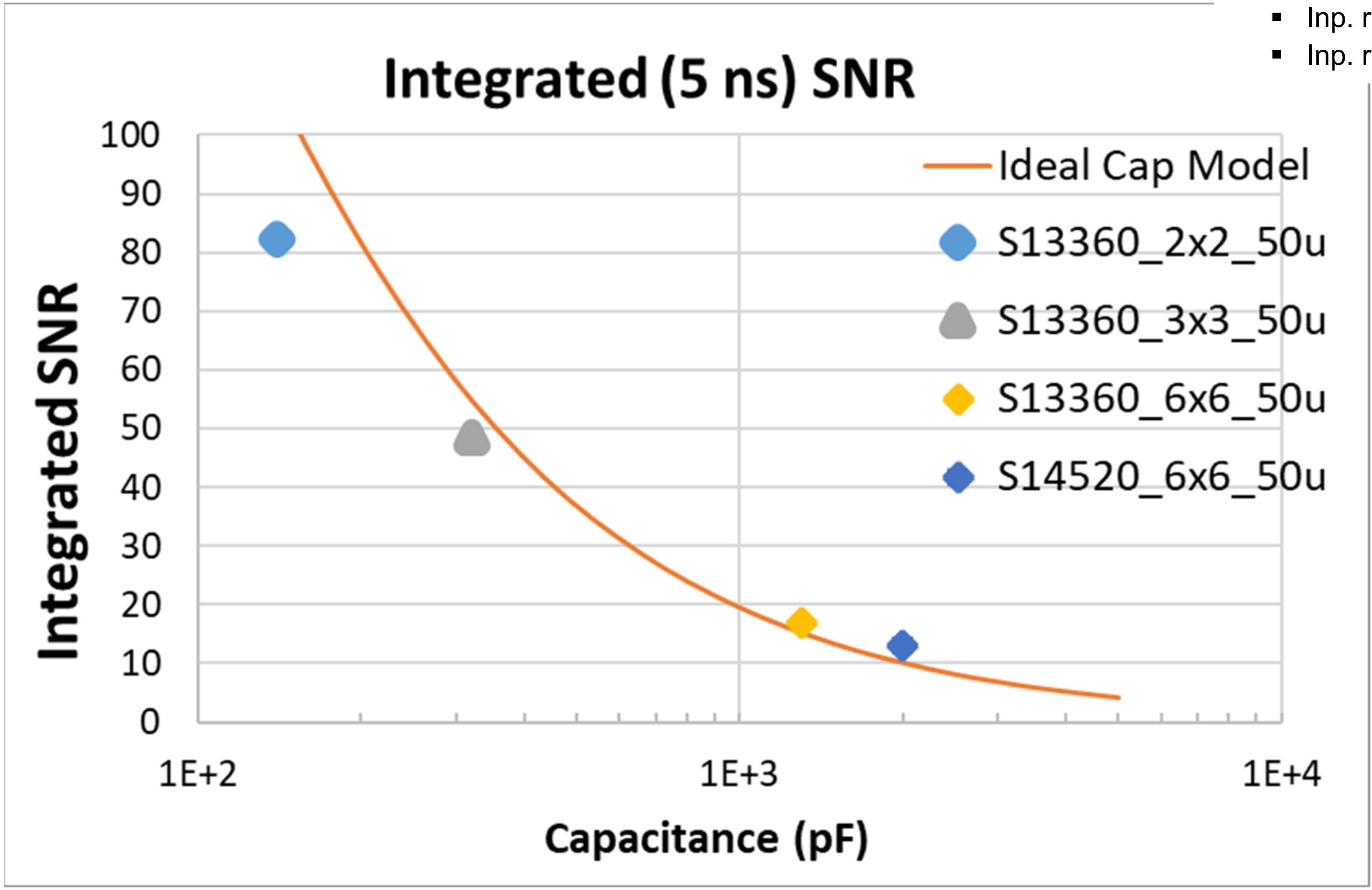
- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)



II. SiPM signal with FE : energy resolution

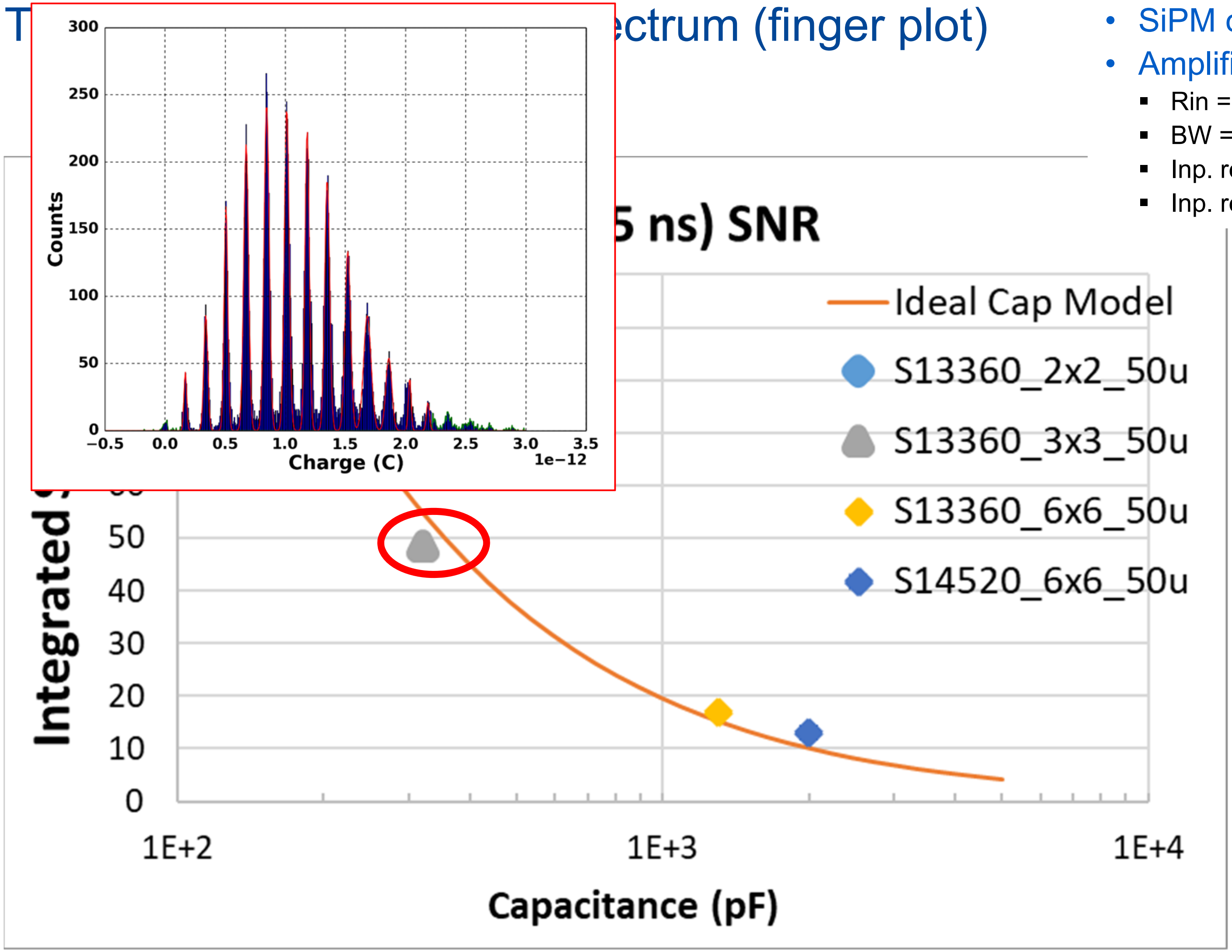
- Energy/light is typically measured by integration
  - Either analog (shaping) or digital signal processing
  - The SNR depends on the integration (shaping) time
    - For a simple 5 ns integration

- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)



II. SiPM signal with FE: energy resolution

- Energy/light is typically measured by integration
- T ectrum (finger plot)

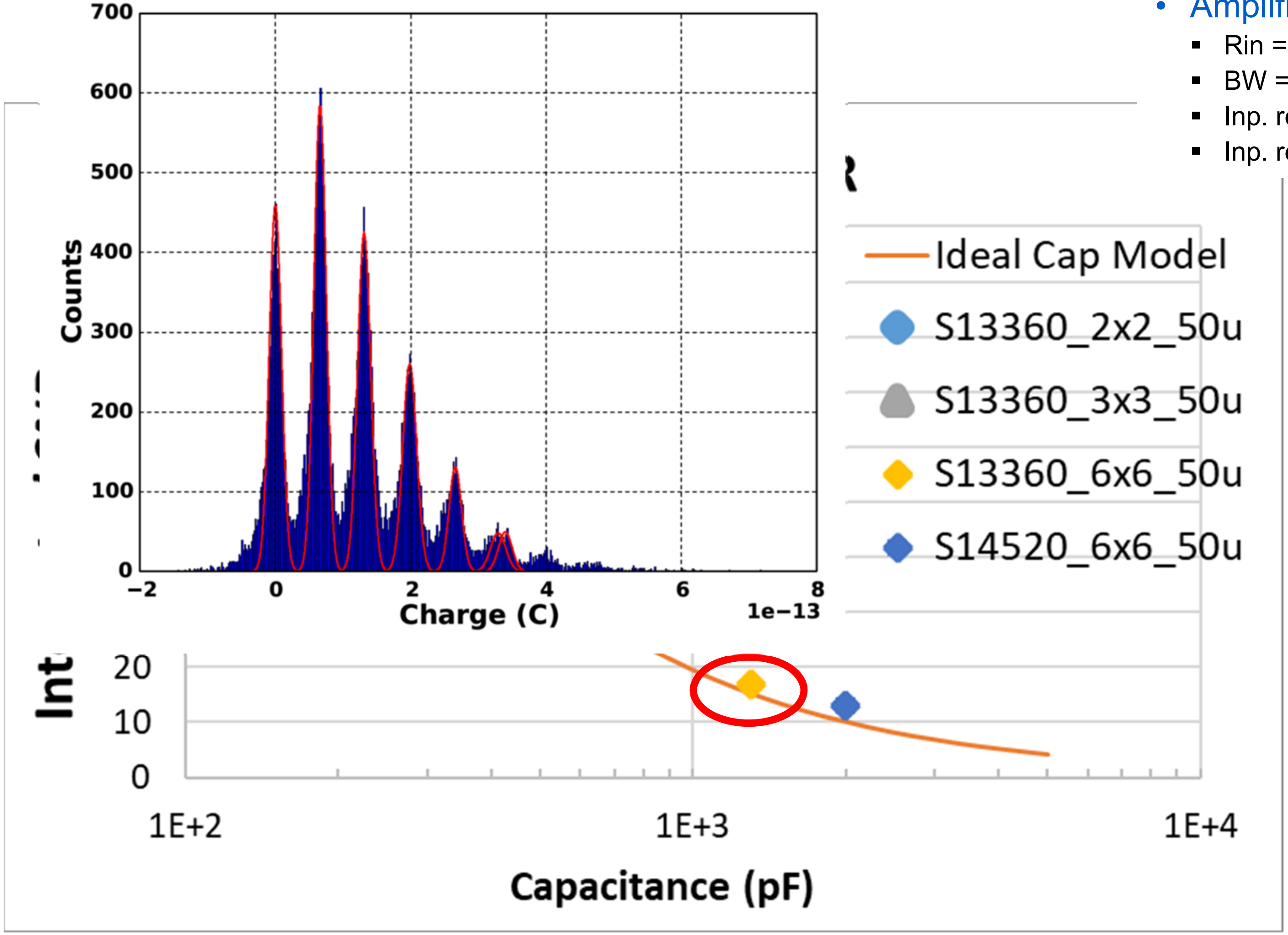


- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)

II. SiPM signal with FE : energy resolution

- Energy/light is typically measured by integration
- This is relfected in charge spectrum (finger plot)

- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)



II. SiPM signal with FE : energy resolution

- Energy/light is typically measured by integration
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- SiPM overvoltage: 4.5 V
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  - Rin = 15 Ω
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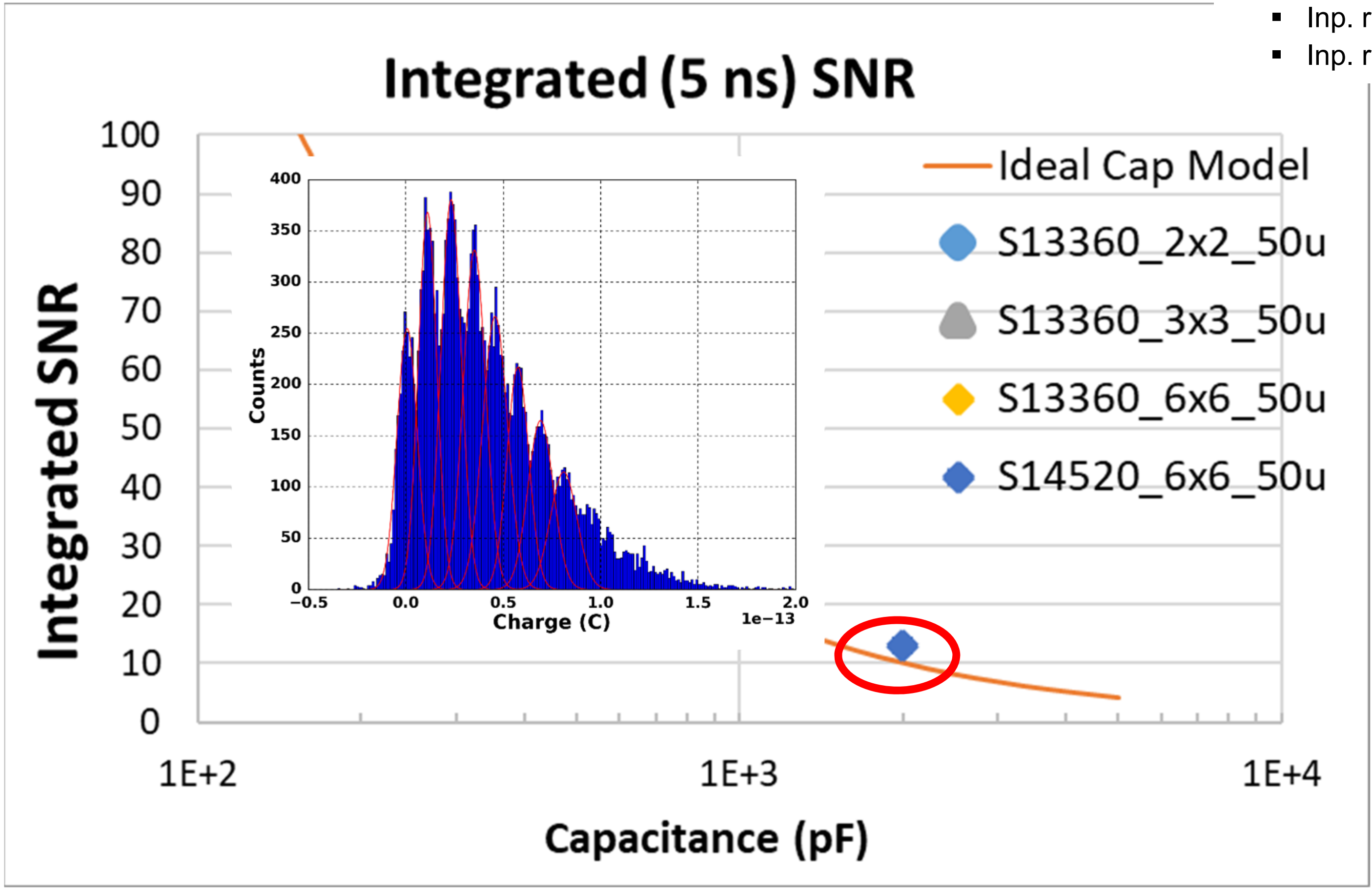
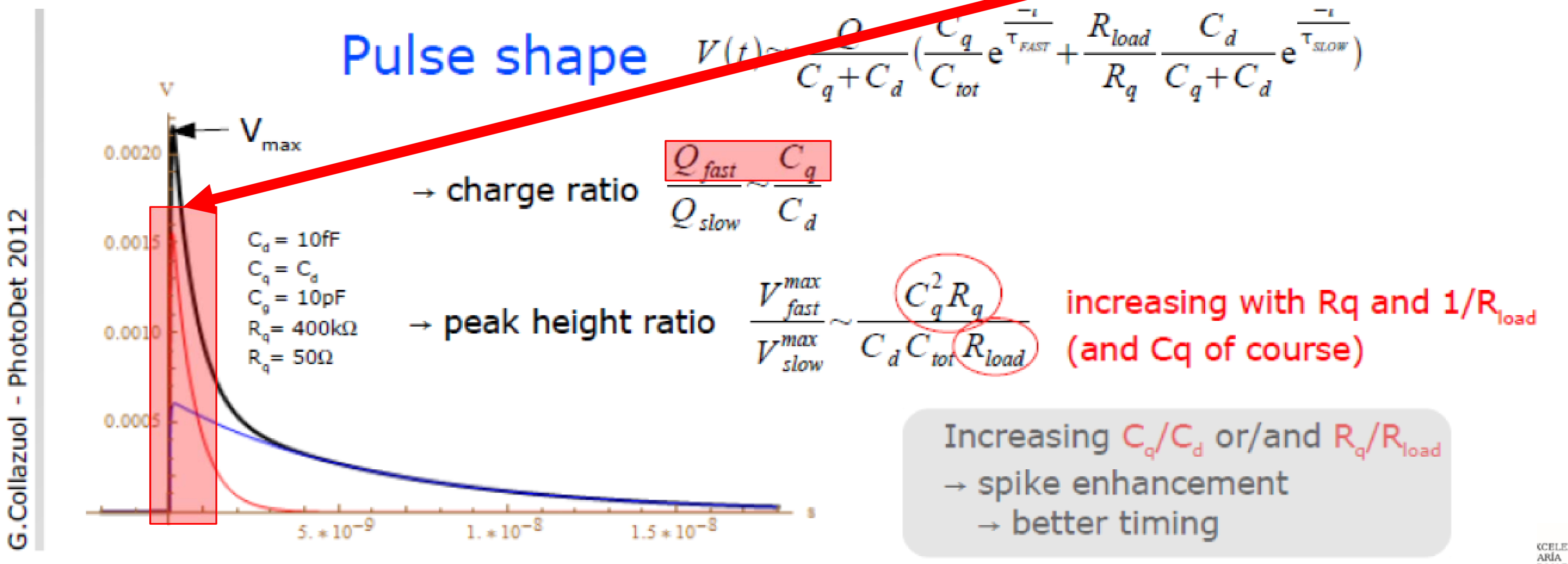


II. SiPM signal with FE : integration time

- Even if “nominal” gain is in the order of 10^6 only a fraction of the charge is used for fast read-out systems
- The “effective” gain for a fast system can be between 2 and 10 times lower than the nominal gain

Effective SiPM gain depends on the shaping time !!



G.Collazuol - PhotoDet 2012

Pulse shape $V(t) \sim \frac{Q}{C_q+C_d}\left(\frac{C_q}{C_{tot}} e^{\frac{-t}{\tau_{FAST}}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q+C_d} e^{\frac{-t}{\tau_{SLOW}}}\right)$

$C_d = 10fF$
$C_q = C_d$
$C_g = 10pF$
$R_q = 400k\Omega$
$R_q = 50\Omega$

→ charge ratio $\boxed{\frac{Q_{fast}}{Q_{slow}} \sim \frac{C_q}{C_d}}$

→ peak height ratio $\frac{V_{fast}^{max}}{V_{slow}^{max}} \sim \frac{C_q^2 R_q}{C_d C_{tot} R_{load}}$

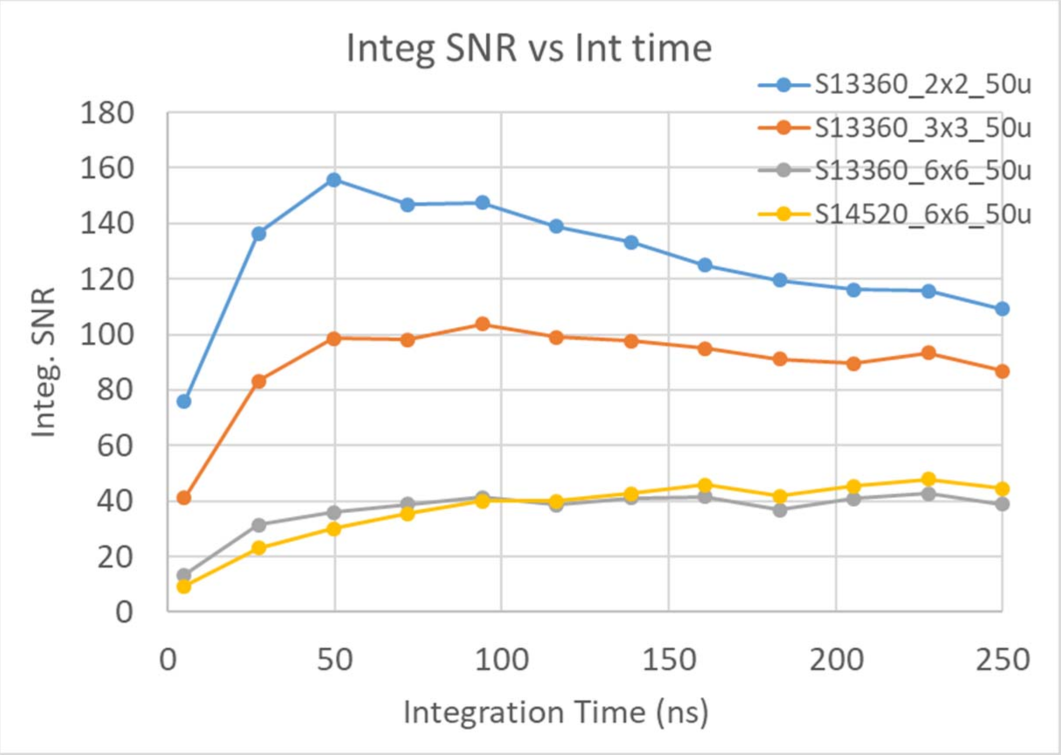
increasing with Rq and $1/R_{load}$
(and Cq of course)

Increasing C_q/C_d or/and R_q/R_{load}
→ spike enhancement
→ better timing

II. SiPM signal with FE: integration time

- Longer shaping times help to dramatically improve SNR of the charge spectrum
  - – Application dependent !
- Longer shaping times:
  - – Increase signal collection (important for large devices)
  - – Mitigates the effect of series noise
    - Warning: but increases the effect of parallel noise (important for small devices)!

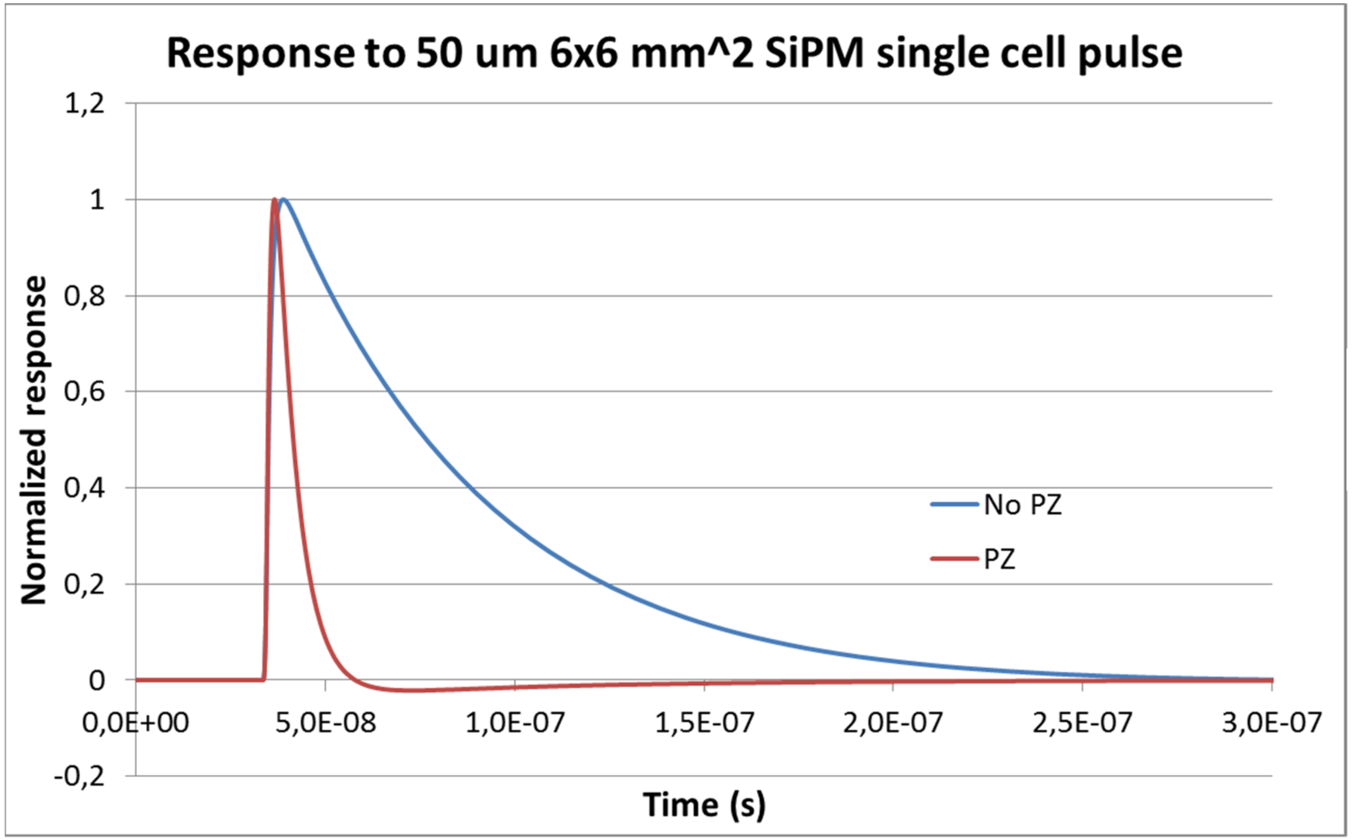
- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)



Disclaimer: increasing integration time may not work because of DCR, correlated noise, pile-up…

II. SiPM signal with FE : Pole-Zero cancellation

- Pole-Zero (PZ) cancellation of the SiPM recovery long time constant (τ_r)
  - – Used for high event rates (avoid pile-up)
- The PZ shaping has an effect in the signal to noise ratio (SNR)
  - – Similar to have short integration times



Simulation with a model obtained from 3x3 mm device

II. SiPM signal with FE: time resolution

- Jitter (Single Photon Time Resolution, SPTR):

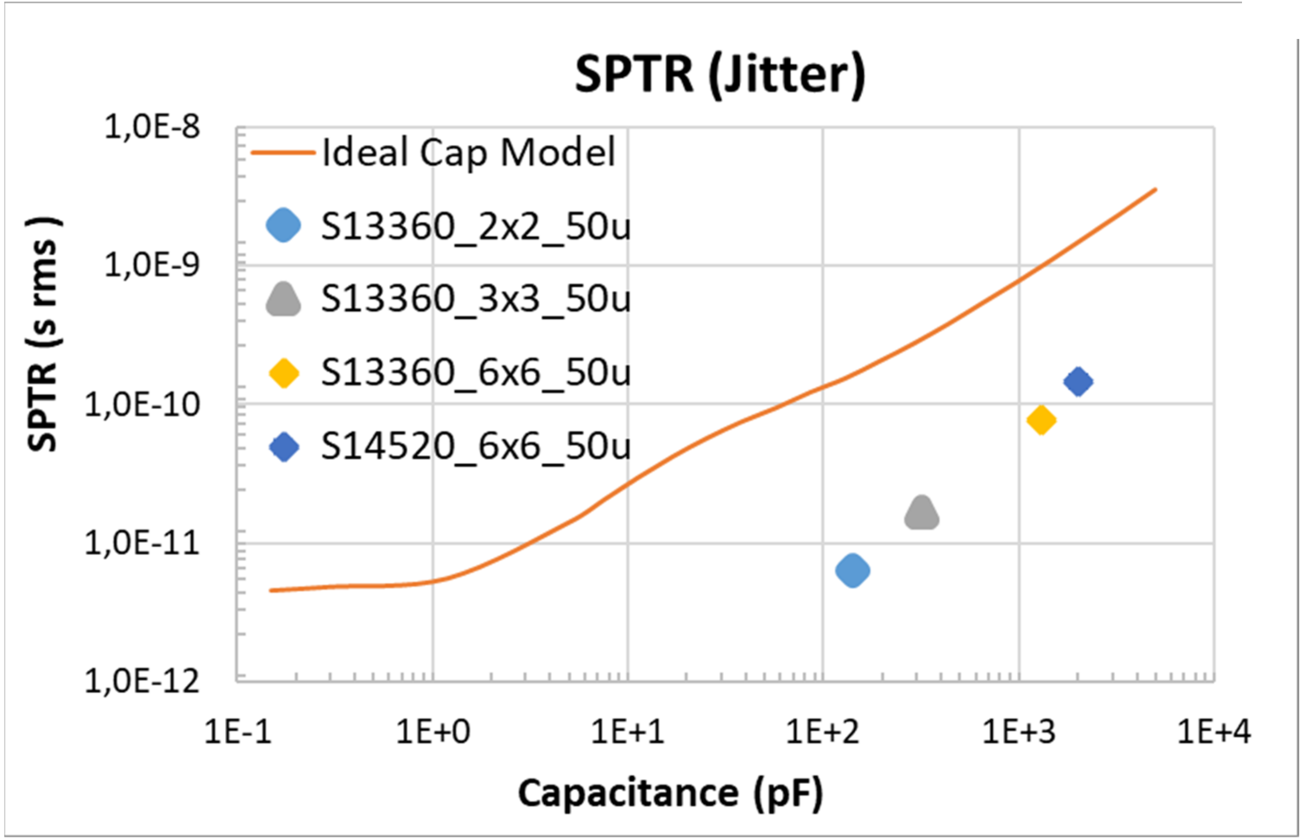
$$\mathrm{SPTR} = \frac{I_{no}}{\partial I_{o1p} / \partial t}$$

I_{no} → Integrated output noise

$\partial I_{o1p} / \partial t$ → 1 cell signal gradient

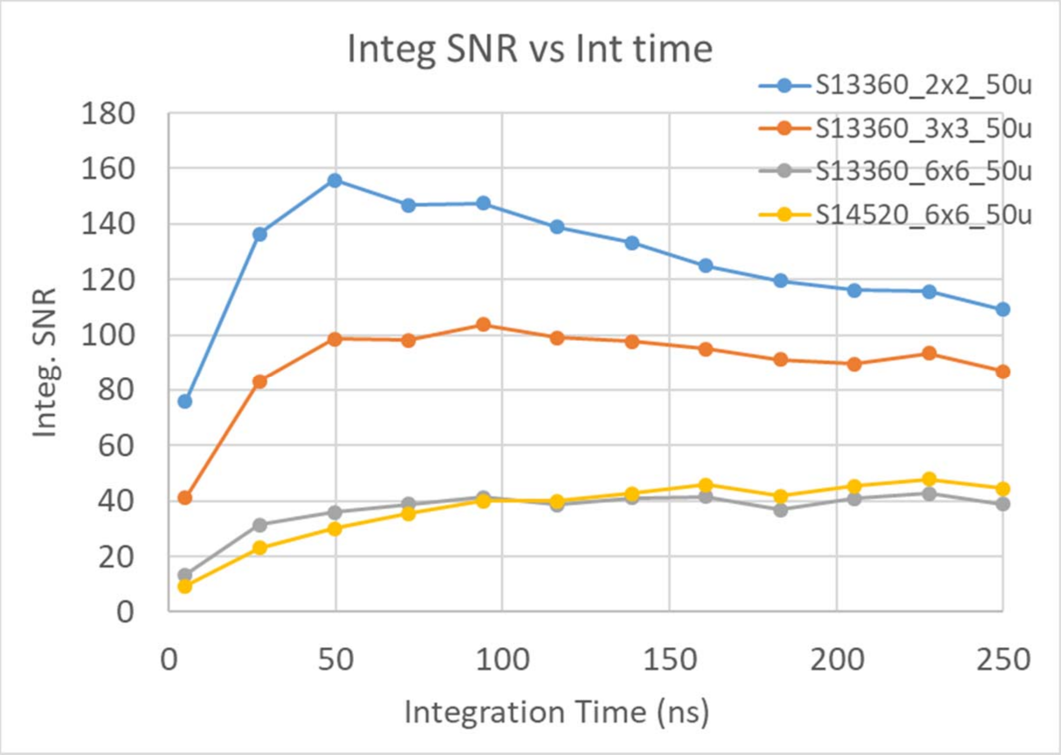
  - Only electronics contribution (no SPAD jitter or skews)

- SiPM overvoltage: 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: 2 nV/sqrt(/Hz)
  - Inp. ref. par. noise: 10 pA/sqrt(/Hz)



II. Input stage: large sensors and short shaping times

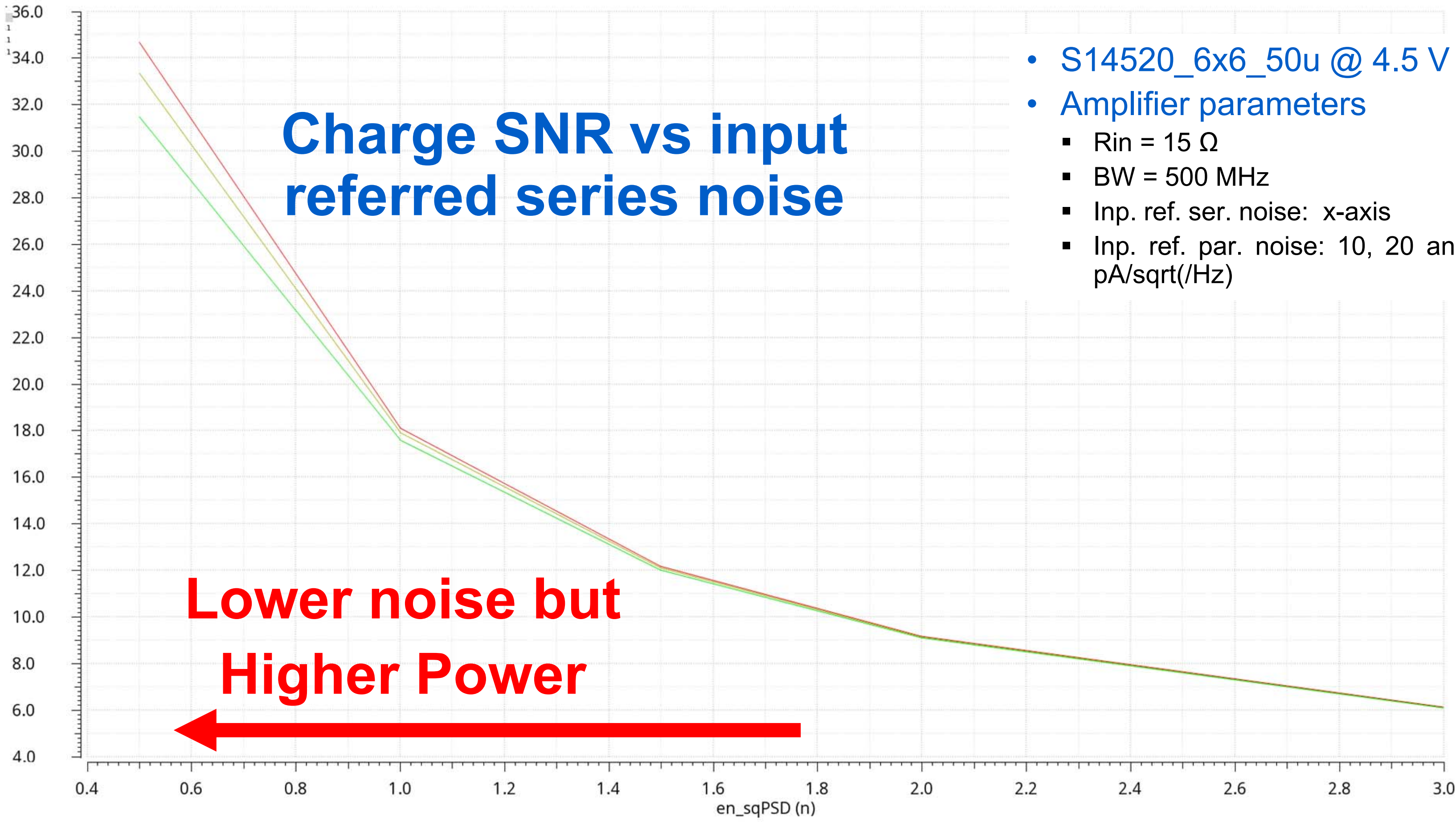
- For small SiPMs or “slow” applications: any decent preamp ...



- **Problem is with large area** (cap >> few 100s pF) <u>**and fast**</u> (<< 100ns shaping time) applications

II. Input stage: large sensors and short shaping times

- The preamp can be optimized for large sensors:
  - Increasing power to reduce input referred series noise



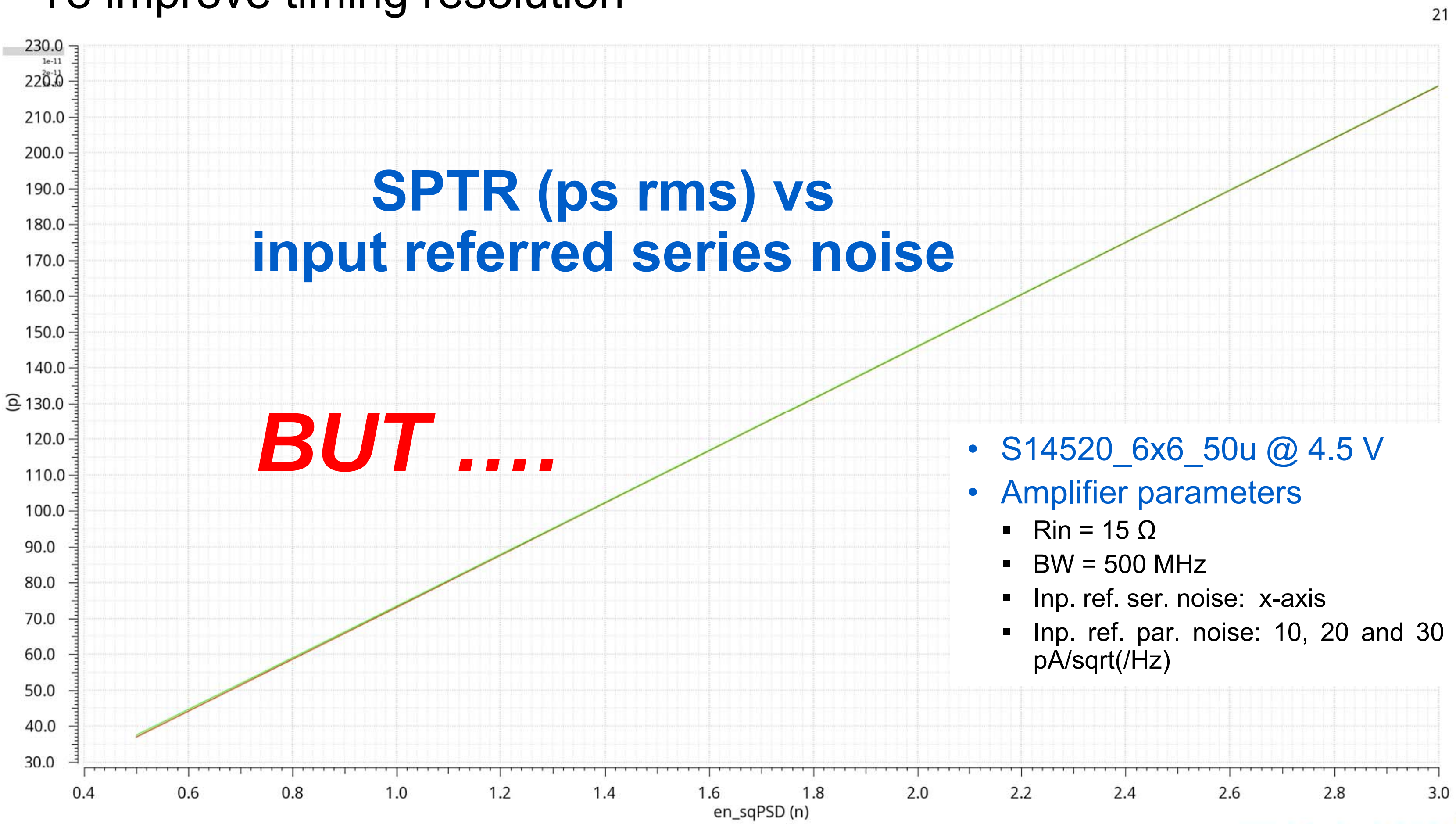
Charge SNR vs input referred series noise

- S14520_6x6_50u @ 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: x-axis
  - Inp. ref. par. noise: 10, 20 and 30 pA/sqrt(/Hz)

Lower noise but Higher Power

II. Input stage: large sensors and short shaping times

- Increasing preamp power helps:
  - To improve energy resolution in fast applications
  - To improve timing resolution



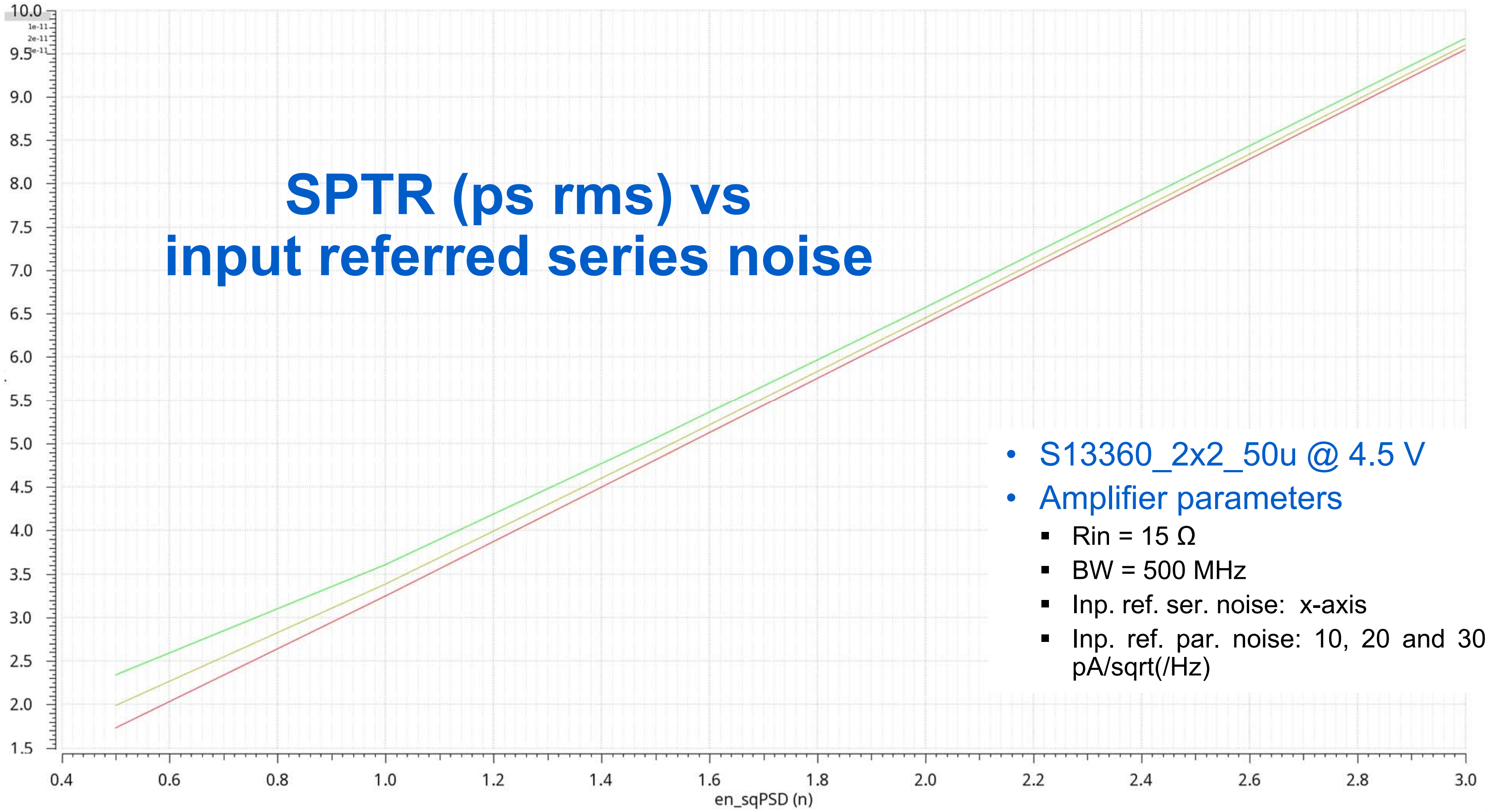
SPTR (ps rms) vs input referred series noise

BUT ….

- S14520_6x6_50u @ 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: x-axis
  - Inp. ref. par. noise: 10, 20 and 30 pA/sqrt(/Hz)

II. Input stage: large sensors and short shaping times

- The best preamplifier connected large SiPM will never beat a normal amplifier connected to a small SiPM



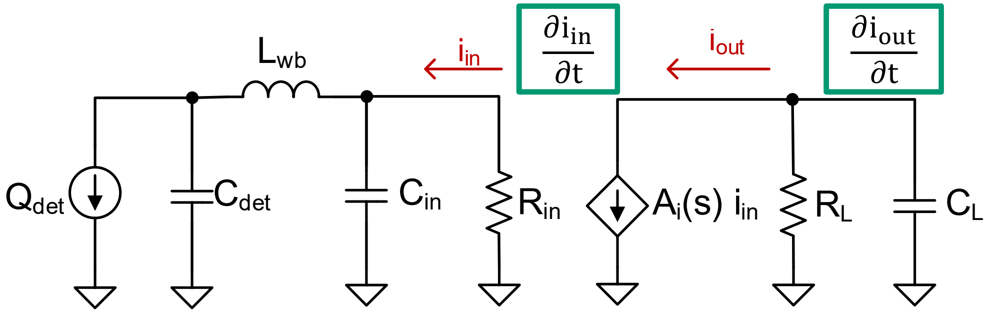
SPTR (ps rms) vs input referred series noise

- S13360_2x2_50u @ 4.5 V
- Amplifier parameters
  - Rin = 15 Ω
  - BW = 500 MHz
  - Inp. ref. ser. noise: x-axis
  - Inp. ref. par. noise: 10, 20 and 30 pA/sqrt(/Hz)

II. Effect of interconnects (inductance)

Convolution between the input slope and the electronics bandwidth (time domain):

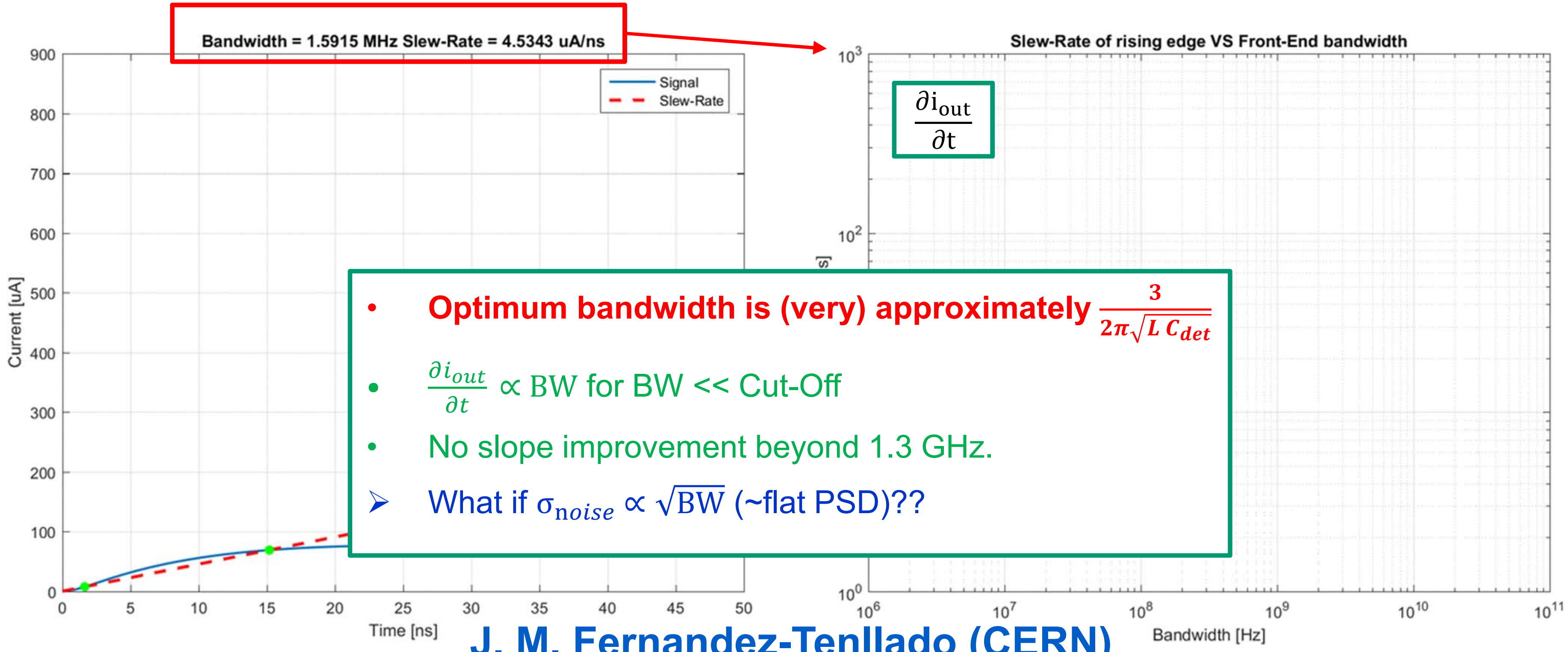
$$SR = \frac{\partial i_{out}}{\partial t} \propto \left(\frac{\partial i_{in}}{\partial t}\right) * \left(BW \cdot e^{-t \cdot BW}\right)$$



Optimum bandwidth for connecting inductances 5 nH – 25 nH and Cdet = 10 pF – 1 nF

Lwb / Cdet

5 nH / 10 pF	5 nH / 1 nF	25 nH / 10 pF	25 nH / 1 nF
1.3 GHz	270 MHz	560 MHz	81 MHz

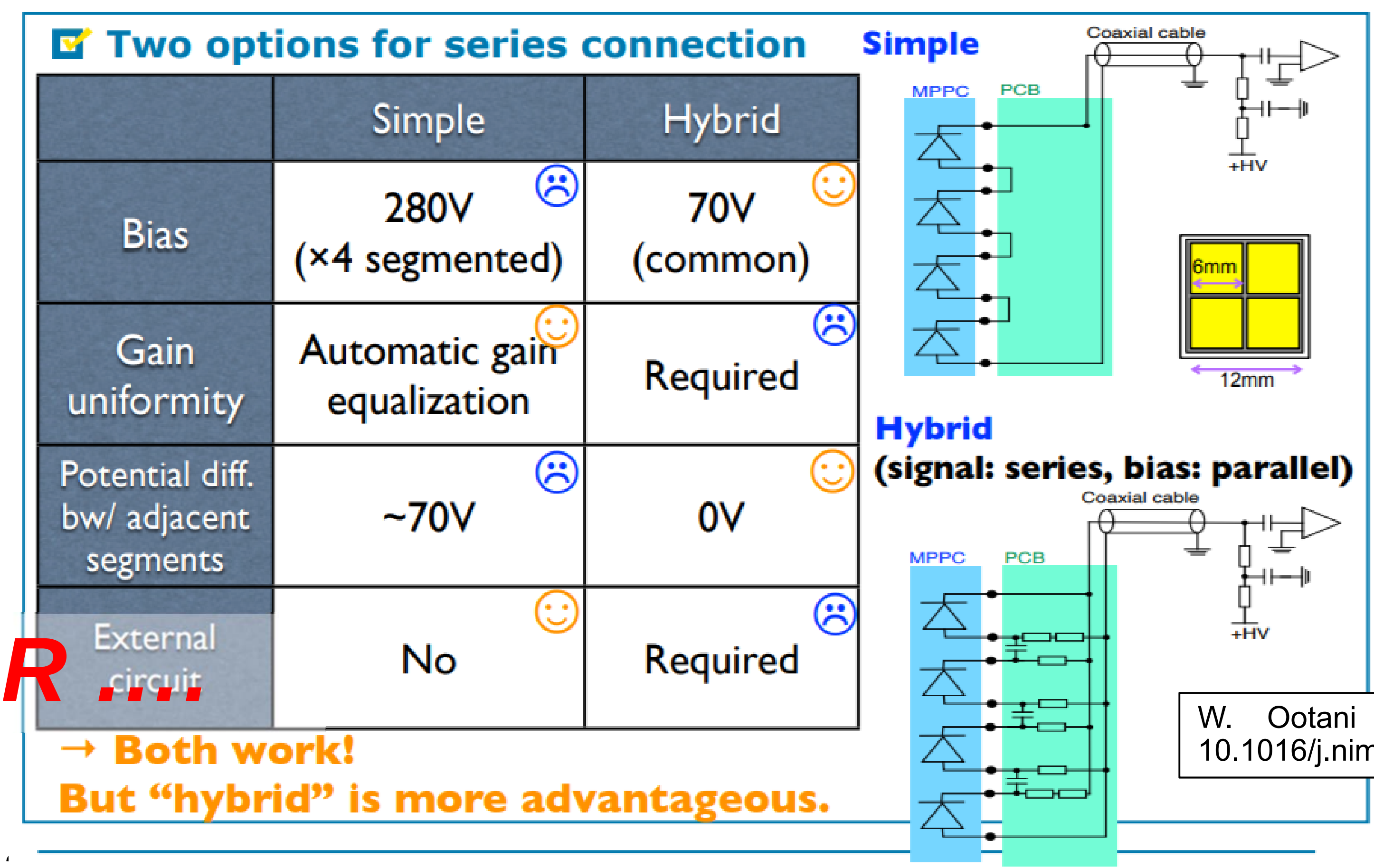


- **Optimum bandwidth is (very) approximately $\frac{3}{2\pi\sqrt{L\, C_{det}}}$**
- $\frac{\partial i_{out}}{\partial t} \propto \mathrm{BW}$ for BW << Cut-Off
- No slope improvement beyond 1.3 GHz.
- ➢ What if $\sigma_{noise} \propto \sqrt{\mathrm{BW}}$ (~flat PSD)??

J. M. Fernandez-Tenllado (CERN)

II. Input stage: combining smaller sensors (passive)

- To obtain large area sensors:
  - Parallel connection: large capacitance !
  - Series (simple or hybrid) connection: lower capacitance (but lower signal):
    - Useful for reducing sensor recovery time not so clear for SNR (depends on amplifier Zin)



☑ **Two options for series connection**

	Simple	Hybrid
Bias	280V (×4 segmented) ☹	70V (common) ☺
Gain uniformity	Automatic gain equalization ☺	Required ☹
Potential diff. bw/ adjacent segments	~70V ☹	0V ☺
External circuit	No ☺	Required ☹

OR ….

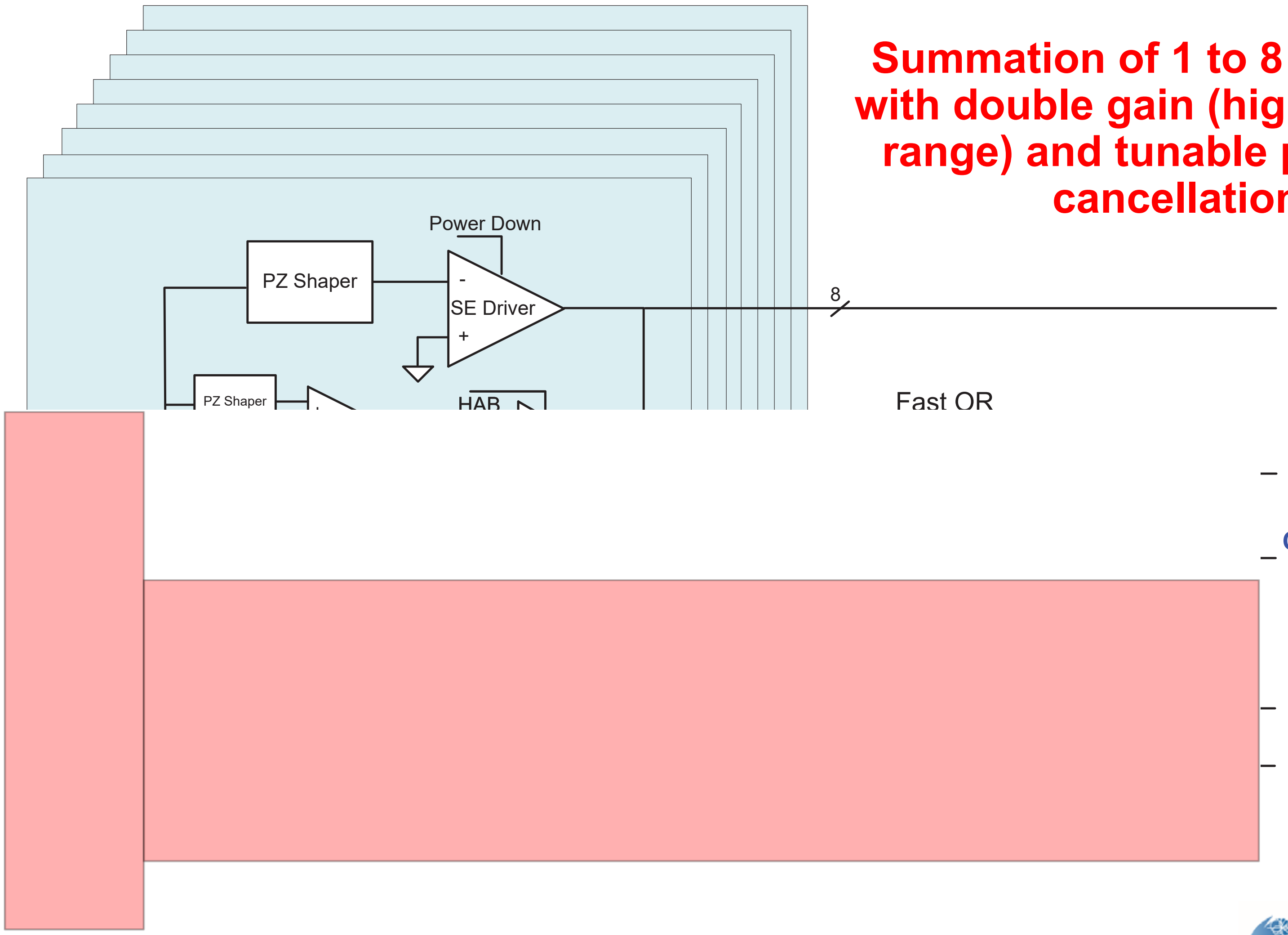
→ Both work!
But "hybrid" is more advantageous.

W. Ootani et al., DOI 10.1016/j.nima.2013.07.043

II. Input stage: combining smaller sensors (active)

- MUSIC 8 ch ASIC performs single ch or summation

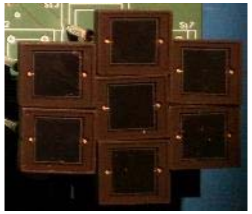
Summation of 1 to 8 channels with double gain (high dynamic range) and tunable pole-zero cancellation



II. Input stage: combining smaller sensors (active)

- Active summation to build large area detectors
- Why active summation?
  - Total noise for active and passive summation can be similar
    - If series noise dominates…
  - But signal (peak) is much higher !
    - Provided high summation BW

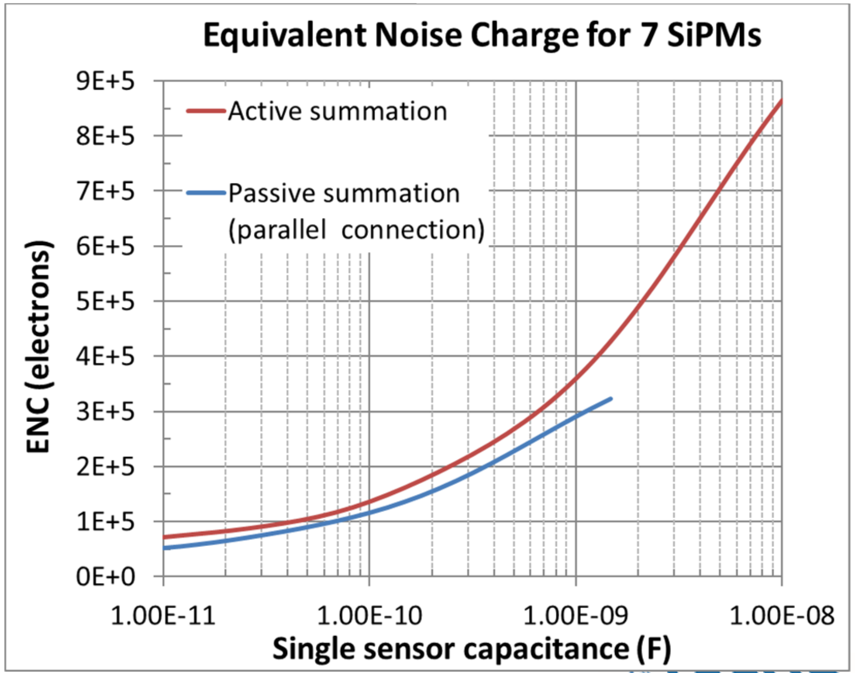
7 x SIPM
6x6 mm^2 each



≈

1 x PMT
18 mm diameter

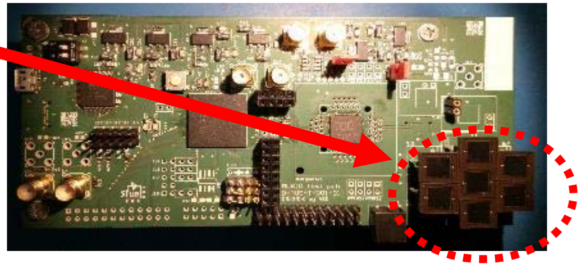
Series noise < 2 nV/sqrt(Hz)
Parallel noise < 20 pA/sqrt(Hz)

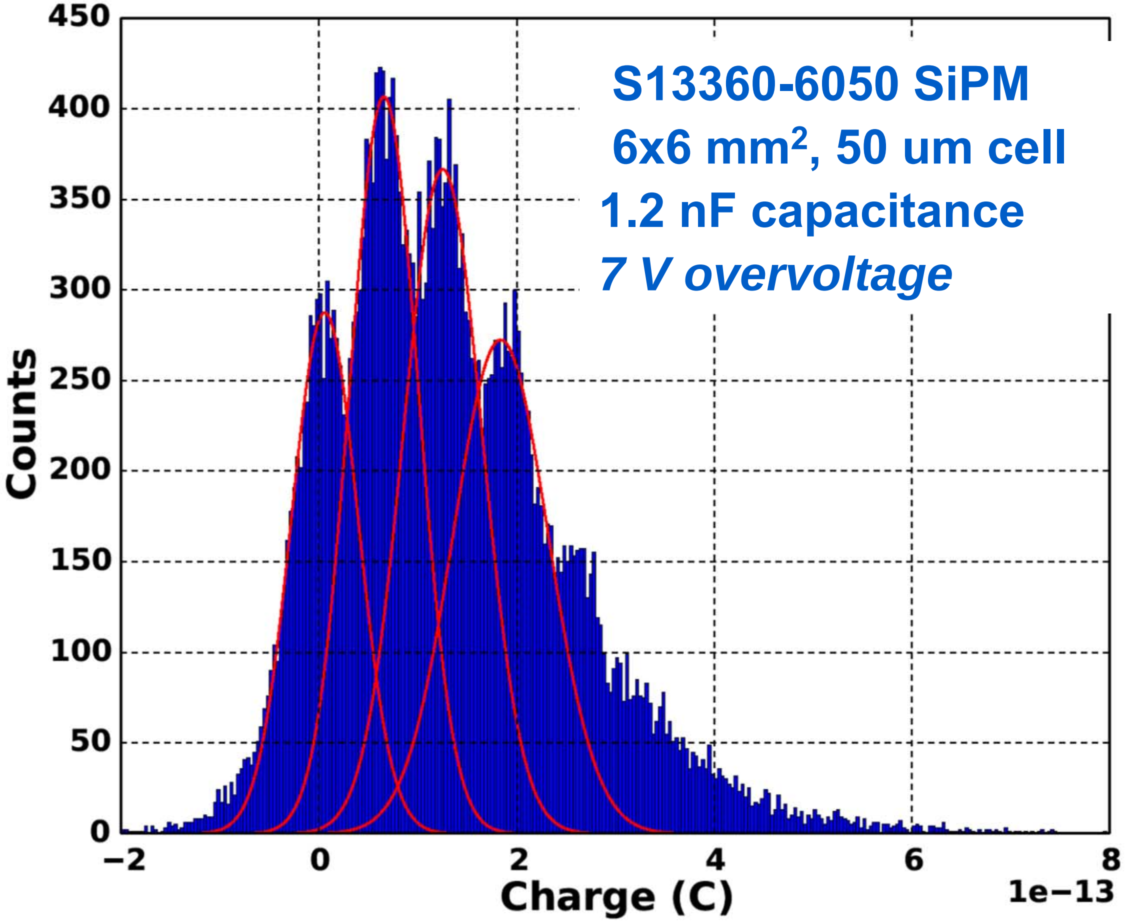


*7x7mm^2 and some custom larger SiPMs exist

II. Input stage: combining smaller sensors (active)

- MUSIC configuration: the adder takes 7 channels
  - Noise is much higher (sqtr(7))
  - But pe (cell) peaks can still be identified
  - Channels have been equalized by MUSIC anode ctrl voltage





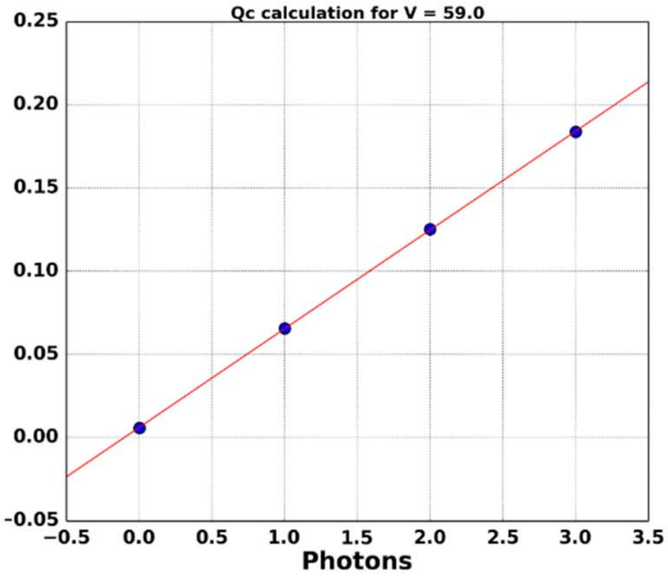
S13360-6050 SiPM

6x6 mm^2, 50 um cell

1.2 nF capacitance

7 V overvoltage

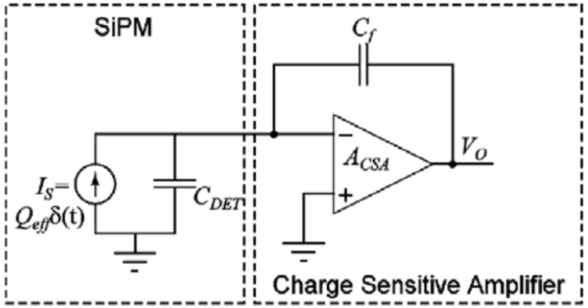
1 x PMT
18 mm diameter ≈ **7 x SIPM**
6x6 mm^2
each



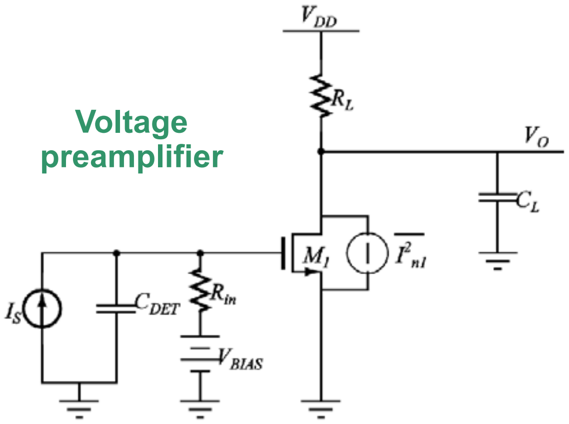
II. Input stage: current versus voltage mode

- Typical photo-sensor front end circuit configurations:

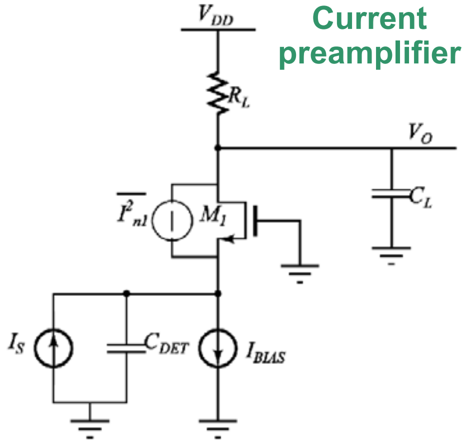
Charge preamplifier



Voltage preamplifier



Current preamplifier



- Best noise performance
- Best with short signals
  - Long tails: pile-up!
  - Need to discharge Cf
- Best with small capacitance
  - BW=Cf/Cdet*GBW, with Cf<<Cdet typically…

- E.g. common-emitter/source configuration
- Large Zin // Large Zout
- Current conversion with Rin
- High power budget for high speed systems
- But can exploit RF technologies

- E.g. (super) common-base/gate
- Low Zin // Large Zout
- Current conversion with Rin
- Potential stability issues
- Best for high rate applications
- Good power/BW trade-offº

F. Ciciriello et alt., "Time performance of voltage-mode vs current-mode readouts for SiPM's," *IWASI*, 2015

Outlook

I. SiPM signal

II. Front End

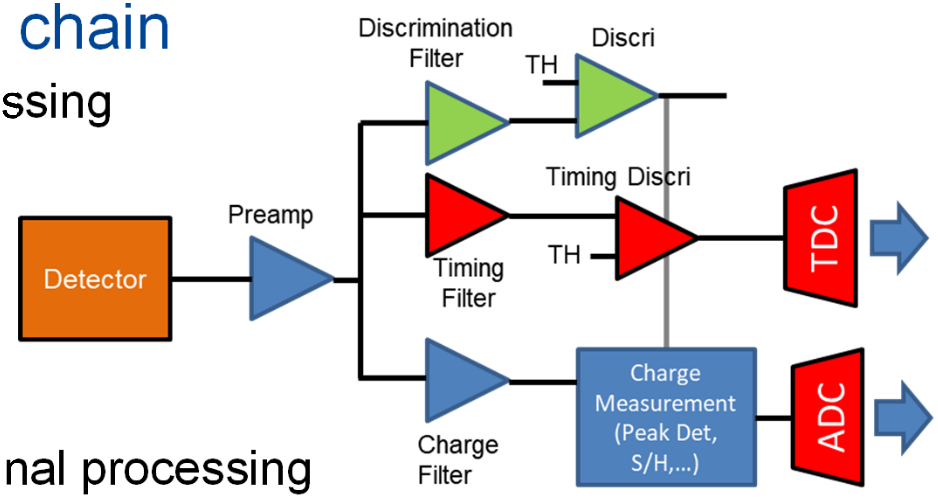
III. Digitization

IV. Digital Sensors

III. Digitization: basic options

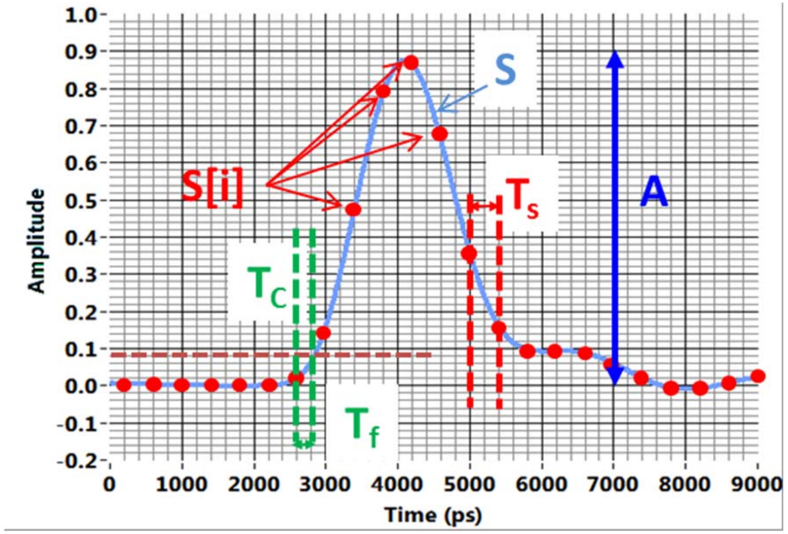
1) “Classical” signal processing chain

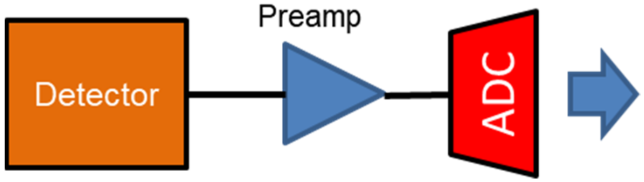
- Requires complex analogue processing
- Not so flexible
- Optimal in power for specific app.



2) Digital signal processing

- Waveform sampling and digital signal processing
- Ideally one should sample at fs > 2 x signal BW (x5)



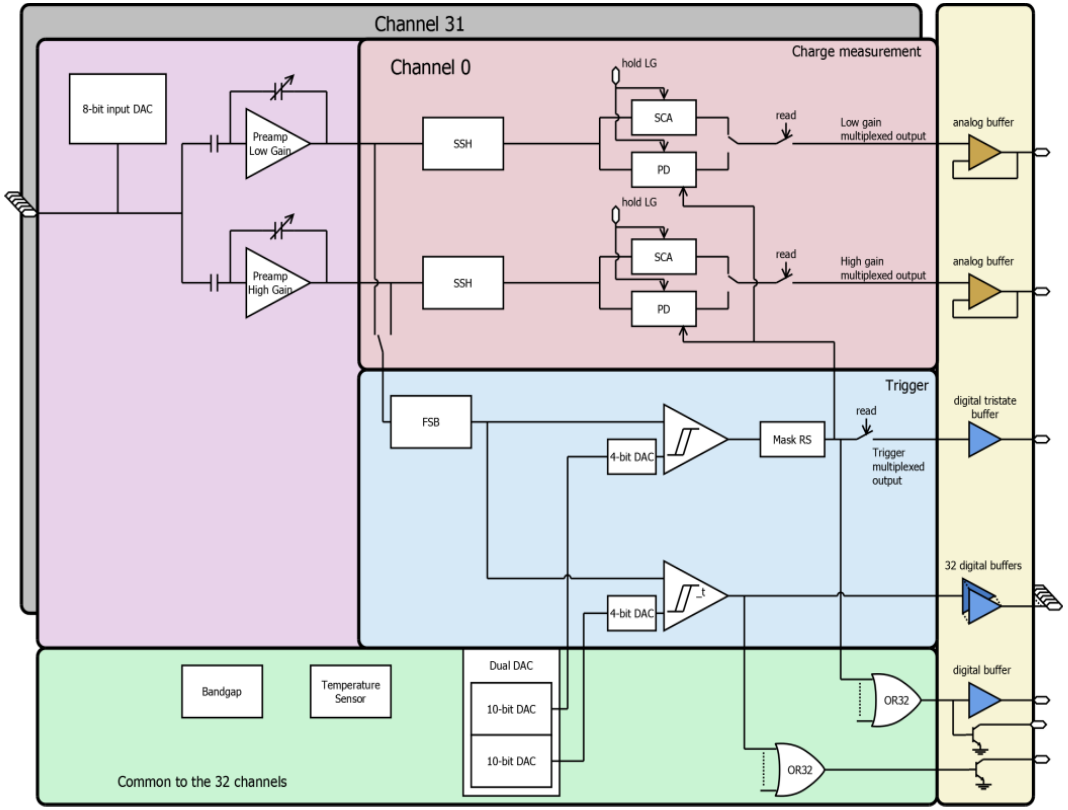


E. Delagnes, “Precise Pulse Timing based on Ultra-Fast Waveform Digitizers”, IEEE NSS 2011

III. Digitization: CITIROC

- CITIROC: voltage mode, analogue and for CTA SSTs ASTRI camera
- Part of Omega/Weeroc family: CITIROC, PETIROC, PETIROC2, TRIROC, etc

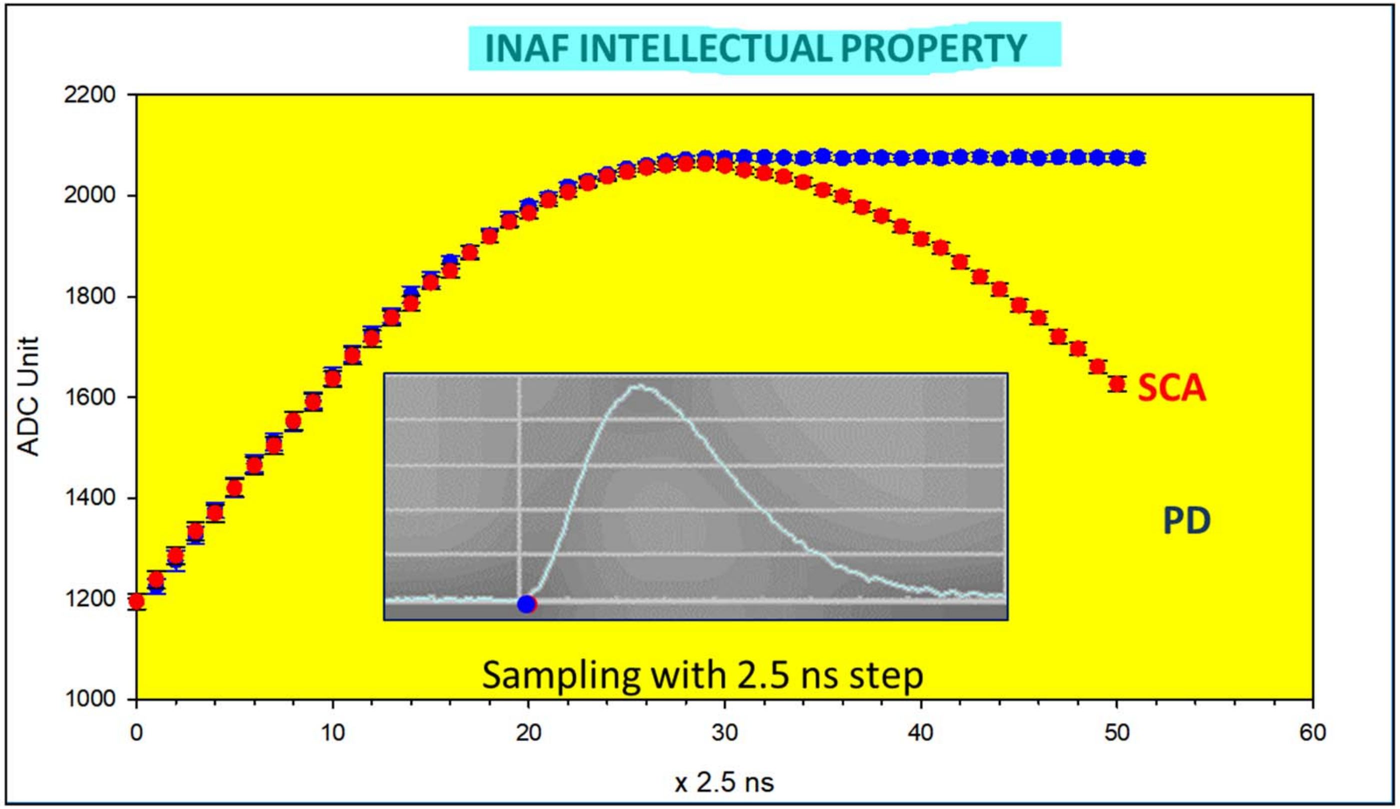
- General ASIC
  - 32 channel, charge and trigger outting
  - 6.26mW/Ch. Power pulsed
- Front-end
  - Trigger
    - Fast shaper connected to either low or high gain preamp
    - Two discriminator : one for timing, one for event validation on energy
  - Energy measurement
    - 2 voltage preamplifier (10x gain difference) followed by shaper
    - Analogue memory : track and hold or peak detector
    - Analogue multiplexer
    - ***Peaking time between 12.5 and 100 ns***
      - ***Valid only for SSTs***



https://www.weeroc.com/fr/products/citiroc-1a

III. Digitization : **CITIROC**

SAMPLING & HOLD Vs. PEAK DETECTION



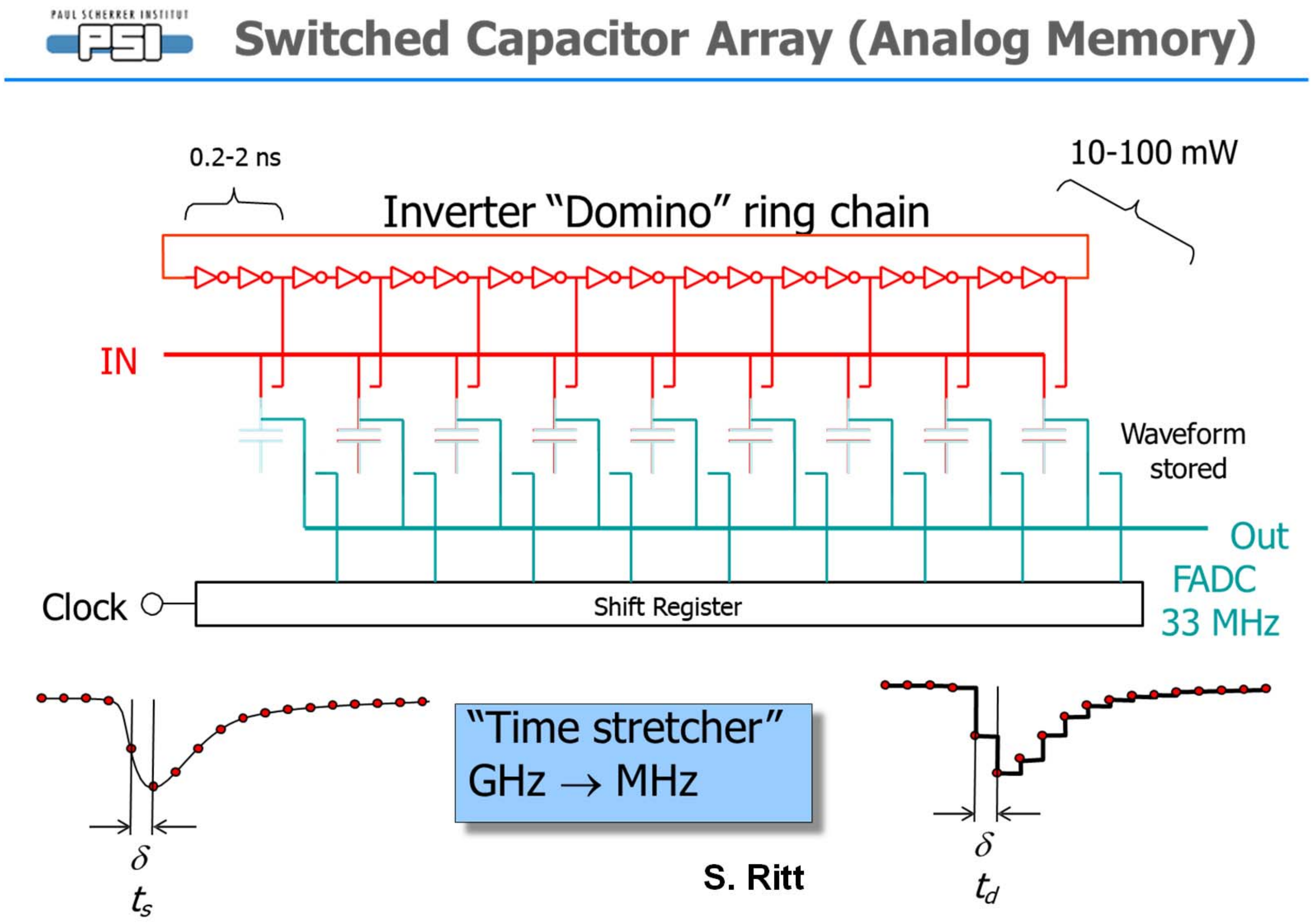
Same pulse measured in SCA and PD mode as a function of delayed HOLD

https://www.weeroc.com/fr/products/citiroc-1a

Osvaldo Catalano– 3rd SiPM Advanced Workshop- Palermo 26-28 May 2015

III. Digitization: waveform sampling

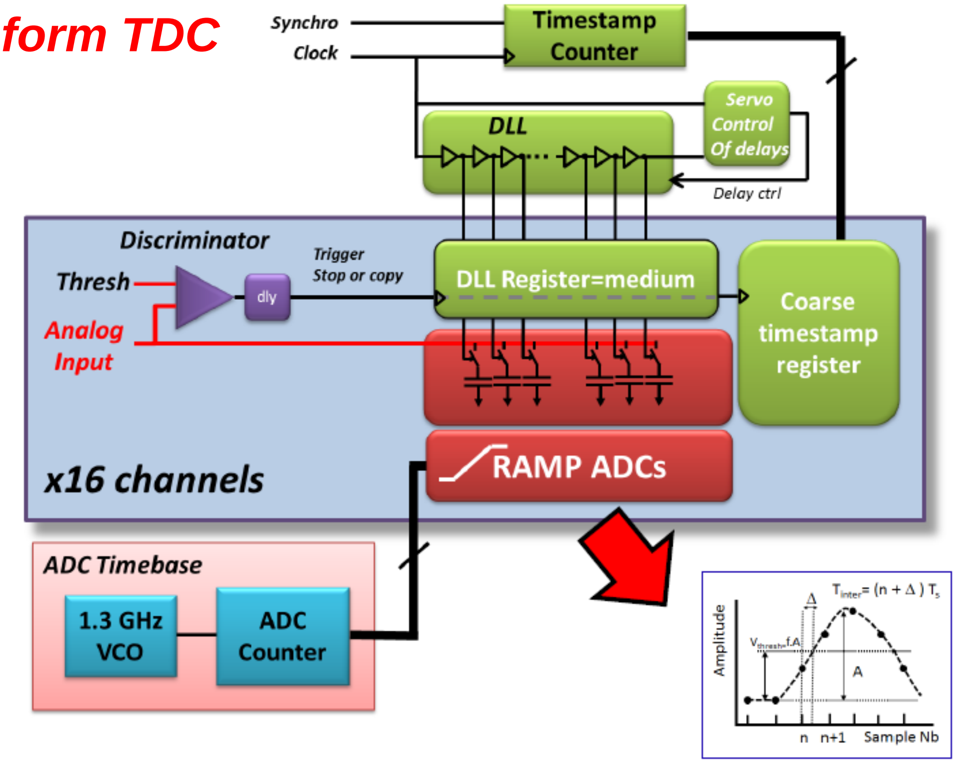
- SCAs sample the signal which is digitized at a lower speed



S. Ritt

III. Digitization : waveform sampling

SAMPIC Waveform TDC



Global time = counter (~10ns) + DLL (~100ps) + waveform(~ps)

Waveform is available for extraction of other parameters (Q, A)

- **One Common 12-bit Gray Counter** (FClk up to 160MHz) for **Coarse Timestamping**.

- **One Common servo-controlled DLL**: (from 1.6 to 10.2 GHz) used **for medium precision timing & analog sampling**

- **16 independent WTDC channels each with :**
  - ✓1 discriminator for self triggering
  - ✓Registers to store the timestamps
  - ✓64-cell deep SCA analog memory
  - ✓One 11-bit ADC/ cell

  (Total : 64 x 16 = 1024 on-chip ADCs)

- **One** common 1.3 GHz oscillator + counter used as timebase for all the Wilkinson A to D converters.

- **Read-Out interface**
- **SPI Link** for Slow Control configuration

D. Breton, 4th FAST WG3/4/5 Meeting, Ljubljana, January7/8 2018

III. Digitization : waveform sampling

SAMPIC
Waveform TDC

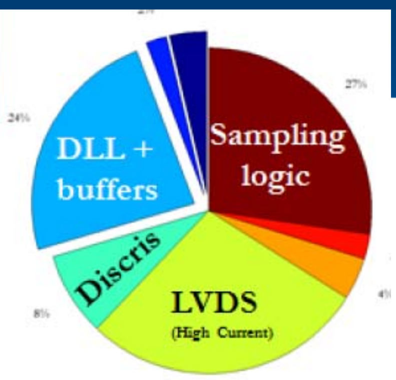
SAMPIC_V1 PERFORMANCES

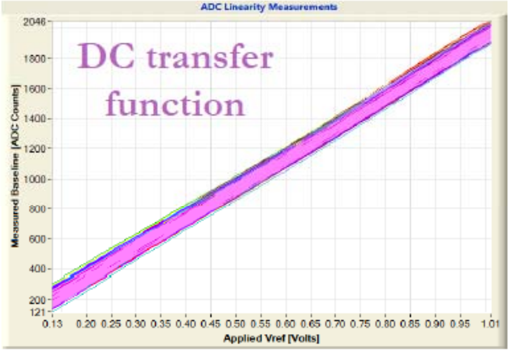
- Power consumption: **10mW/channel** →
- 3dB bandwidth > **1 GHz**
- Discriminator noise **~ 2 mV rms**
- Counting rate **> 2Mevts/s** (full chip, full waveform), **up to > 10 Mevts/s** with Region Of Interest (ROI)

- Wilkinson ADC works with internal **1.3 GHz** clock
  - ➢ Dynamic range of **1V**
  - ➢ Gain dispersion between cells ~ **1%** rms →
  - ➢ Non linearity **< 1.4 %** peak to peak
  - ➢ After correction of each cell (linear fit): noise = **0.95 mV rms**

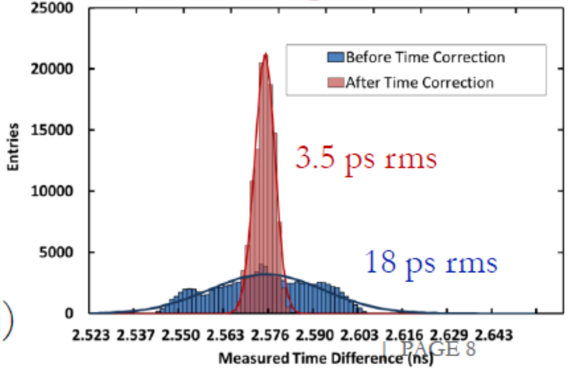
- Time Difference Resolution (TDR):
  - ➢ Raw non-gaussian sampling time distribution due to DLL non-uniformities (TINL)
  - ➢ Easily calibrated & corrected (with our sinewave crossing segments method [D. Breton&al, TWEPP 2009, p149])

Power distribution





Ex: TDR @ 6.4 GS/s

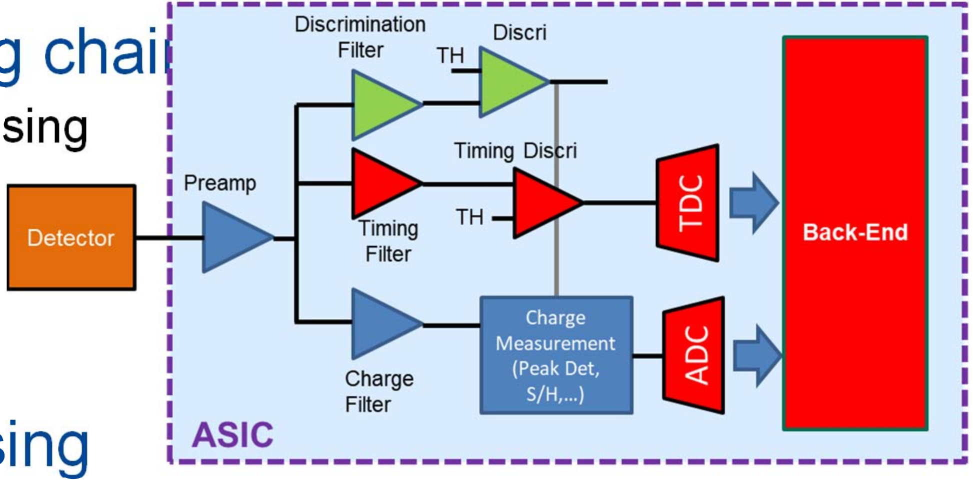


D. Breton, 4th FAST WG3/4/5 Meeting, Ljubljana, January7/8 2018

III. Digitization : a version of classical signal processing

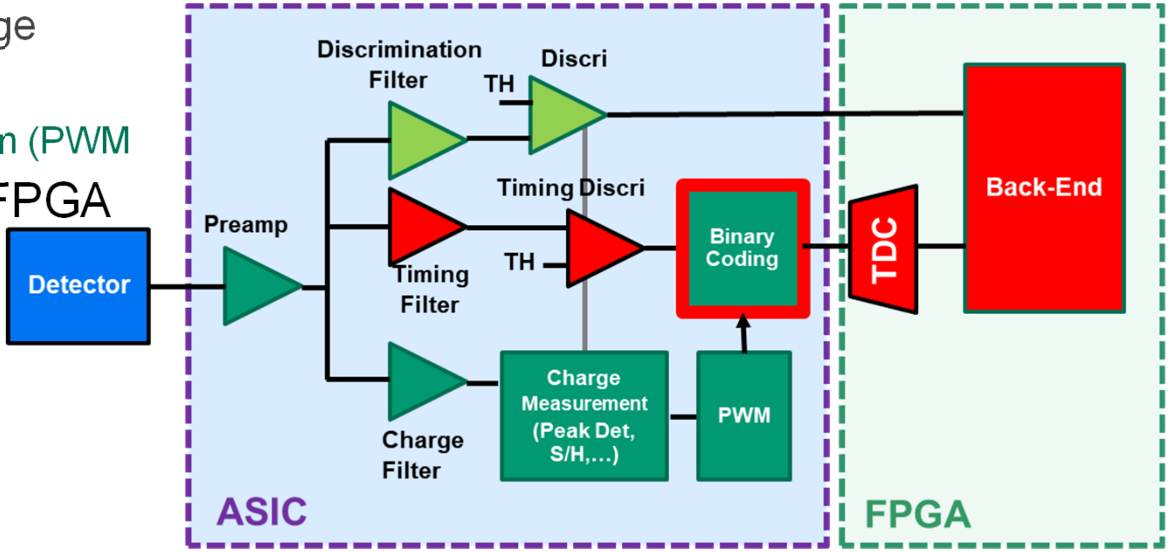
1) “Classical” signal processing chai

- Requires complex analogue processing
- Not so flexible
- Optimal in power for specific app.



2) Time based flexible processing

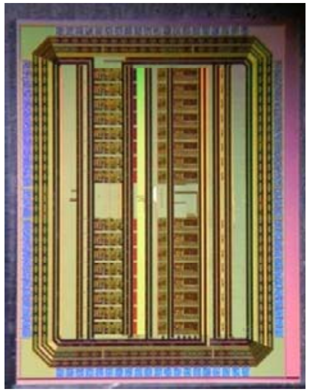
- The chip performs analog processing: codes energy & time in binary signal:
  - Timing: signal trailing edge
  - Energy: pulse width
    - Pulse Width Modulation (PWM
- TDCs and back-end in FPGA
- System on 2 Chips:
  - **It becomes flexible !**
  - Example: (HR)FlexToT



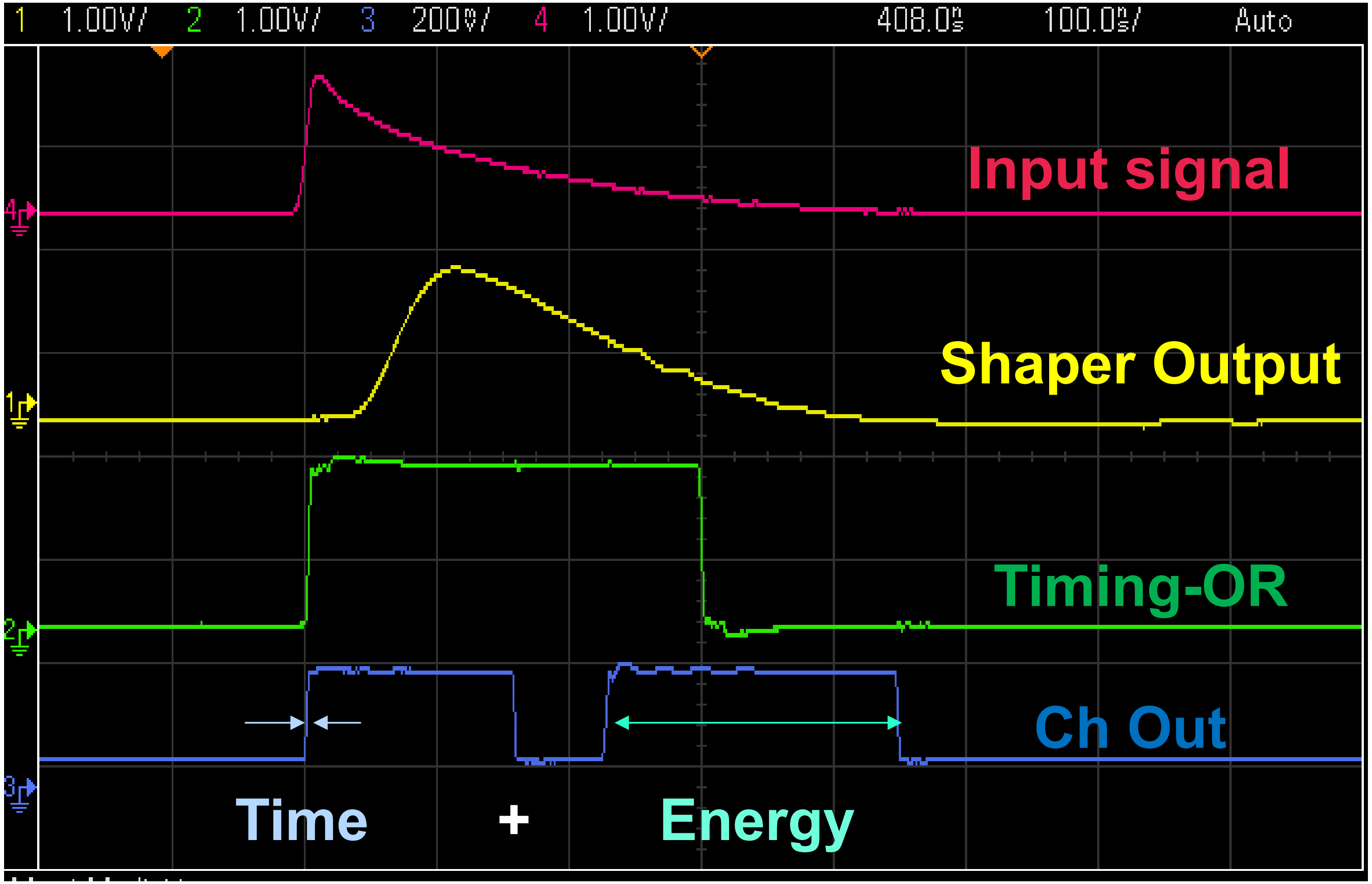
III. Digitization: HRFlexToT: linearized ToT RO chip

HRFlexToT

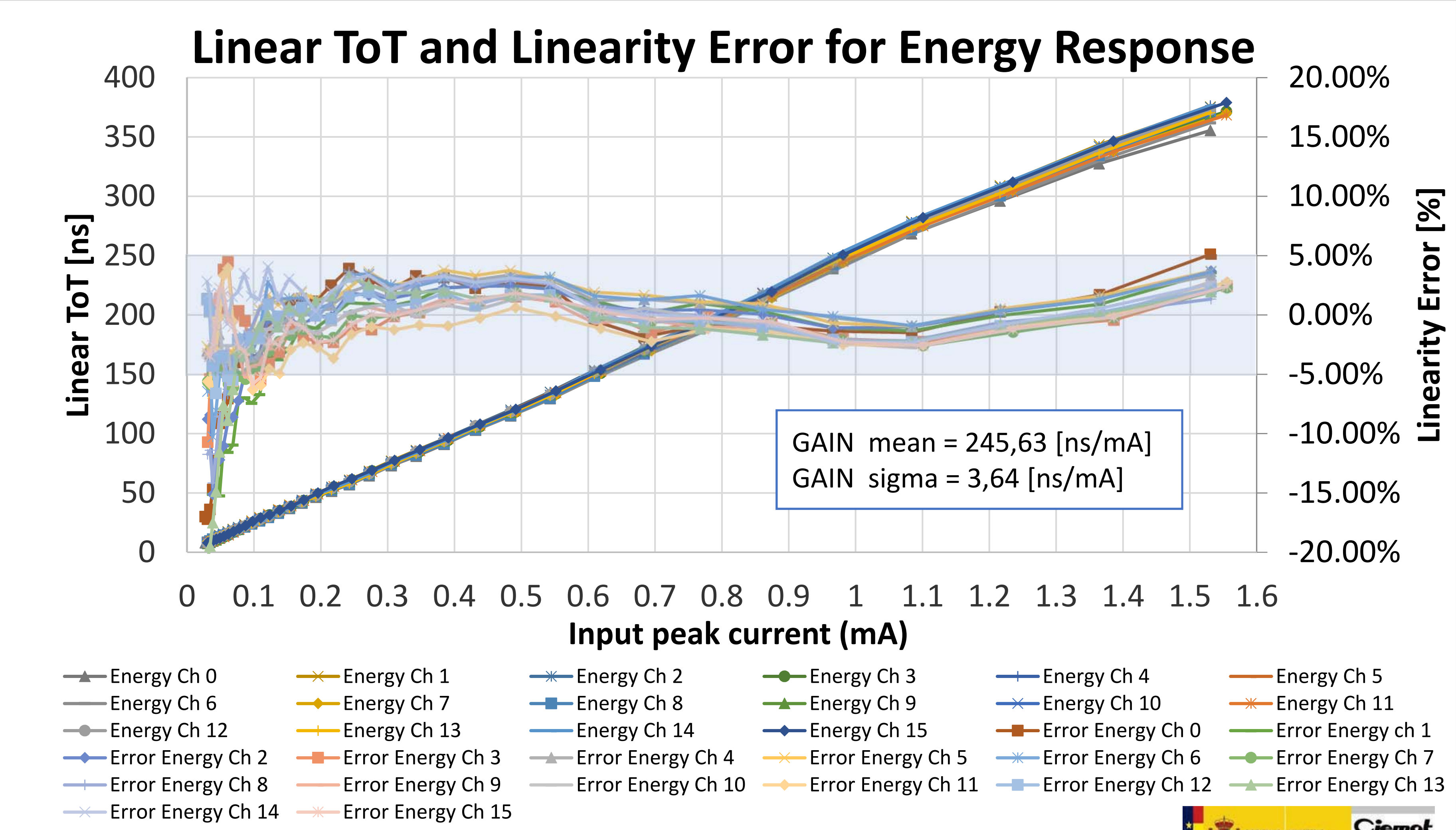
180 nm CMOS



See poster session



III. HRFlexToT: Linearity analysis: Channel Uniformity Peak Detector mode and Max Gain (G=3, RL=3)



GAIN mean = 245,63 [ns/mA]
GAIN sigma = 3,64 [ns/mA]

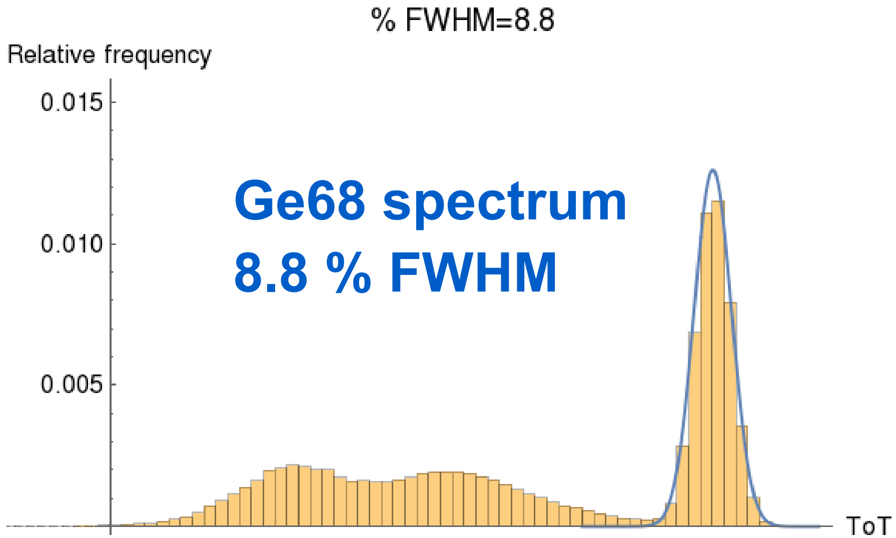
- Maximum current limited by injection system with amplifiers.

III. Digitization: FlexToT: linearized ToT RO chip

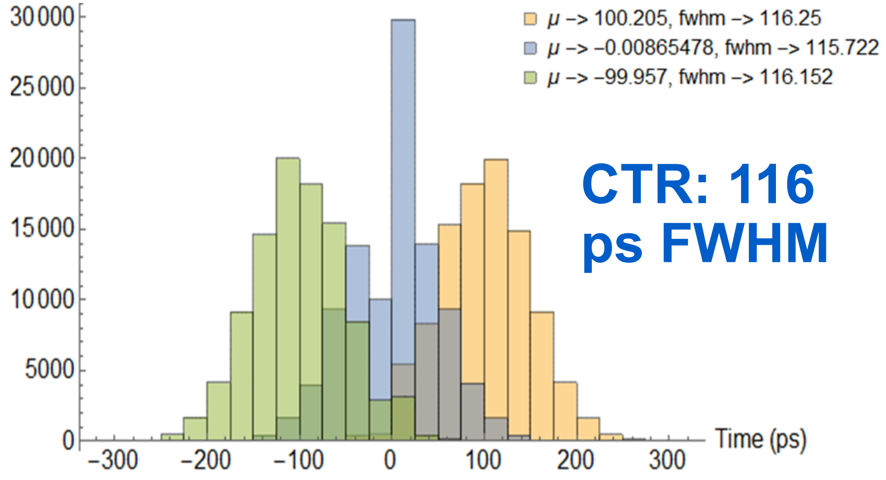
- Pisa University has develpped a FPGA based TDC readout for FlexToT
  - Based on Arria 10 FPGA
    - TDC: 38 ps resolution
  - System CTR: 116 ps FWHM !
  - Energy resolution: 8 % FWHM @ 511 KeV
  - Dead time < 5ns: event rate > 1 MHz !

P. Catra,
G. Sportelli

2 LYSO xtals 3x3x5 mm3
NUV-SiPM



Ge68 spectrum
8.8 % FWHM

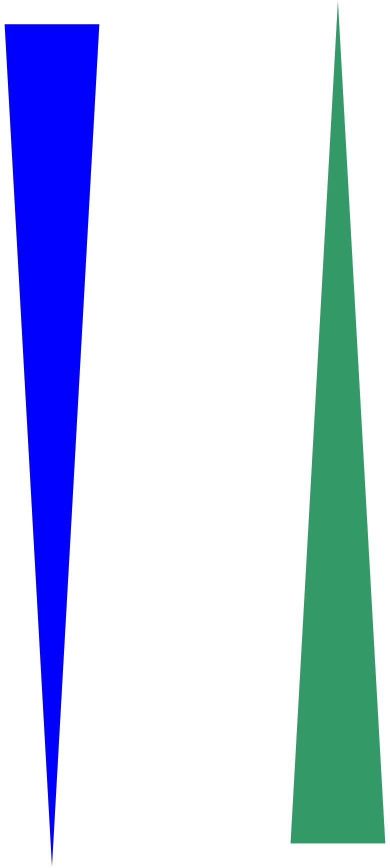


CTR: 116 ps FWHM

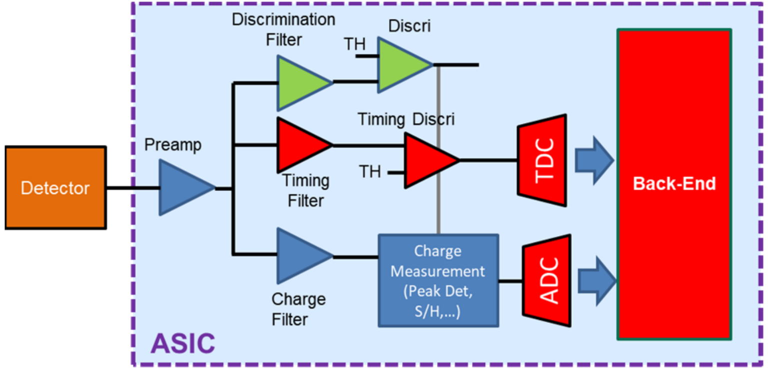
Timing distributions for different source positions

III. Digitization: summary

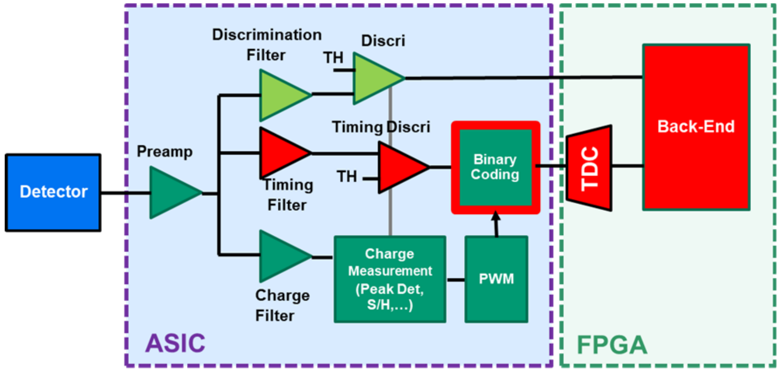
- **Fixed Costs**
- **Dev Time**



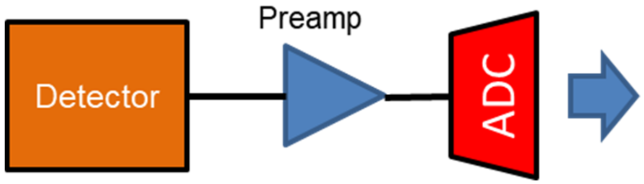
1) “Classical” signal processing



2) Time based flexible processing



3) Waveform sampling (DSP)



- **System complexity**
- **Flexibility**

III. ASIC Summary: comparison (multipurpose)

	Tech (um)	Front-End	Digitization	Ch	Power / ch (mW)	Max Rate (Hz)	Dyn. Range	Shaping Time
CITIROC (CTA)	0.35 SiGe	V, positive, shaping	Charge/Time ADC/TDC	32	6	> 1 KHz	0.1 - 400 pC	50 ns
MUSIC (CTA, SHIP, others)	0.35 SiGe	I, positive, shaping, summation	No Analog Outputs	8	20 (50Ω output drivers)	-	0.1 - 500 pC	5-100 ns
PACIFIC (LHCb-SciFi)	0.13	I, positive, gated integ	Non-linear ADC (2 bits)	64	8	40 MHz /ch	0.1 - 10 pC	25 ns
KLAUS4 (ILC-AHCAL)	0.18	I, positive, cont integ	Charge/Time ADC/TDC	7	2. 5 (2.5 uW)	-	0.1- 130 pC	100 ns
MUTRIG (Mu3e-SciFi)	0.18	I, positive, cont integ	Time based TDC	32	15	> 1 MHz/ch	3 pC – 1 nC	-
NINO (ALICE, others)	0.25	I, differential, discri	Non-Linear ToT	8	30	40 MHz /ch	0.1 – 2 pC	-

- **Non-compehensive list ! No time to talk about all:**
  - **QIE11, EASIROC, SPIROC, etc**

III. ASIC Summary: comparison (multipurpose)

	Tech (um)	Front-End	Digitization	Ch	Power / ch (mW)	Max Rate (Hz)	Dyn. Range	SPTR*1 (ps FWHM)
PETIROC2	0.35 SiGe	V, positive, shaping	Charge/Time ADC/TDC	32	6	40 KHz	0.1 - 400 pC	196
TOFPET2	0.11	I, positive, integ	Charge/Time TDC	64	8	200 KHz	0.1 - 300 pC	210
STIC3	0.18	I, pos/dif, lin ToT	Charge/Time TDC	64	25	100 KHz	0.1 - xx	Xx
PETA6	0.18	I, pos/dif, Integ	Charge/Time ADC/TDC	38	30	200 KHz	0.1-xx	Xx
HRFlexToT	0.18	I, pos, lin ToT	Charge/Time PWM+FPGA	16	3.5 + TDC	>1 MHz	0.1 - 500 pC	140
BASIC64	0.35	I, negative, shaper	Charge/Time ADC/TDC	64	10	75 KHz	0.1 – 400 pC	Xx
IDE3380 SPHIRA	-	I, pos/neg	Charge/Time ADC/TDC	16	15-30	50 KHz	0.1-400 pC	Xx
NINO	0.25	I,differential, discri	Non-Linear ToT	8	30	40 MHz /ch	0.1 – 2 pC	150

***1: SPTR:** Single Photon Time Resolution for a 3x3 mm^2 50 um SiPM

- Laser and acquisition jitter are not substracted
- All chips readout in analog mode

References on ASICs

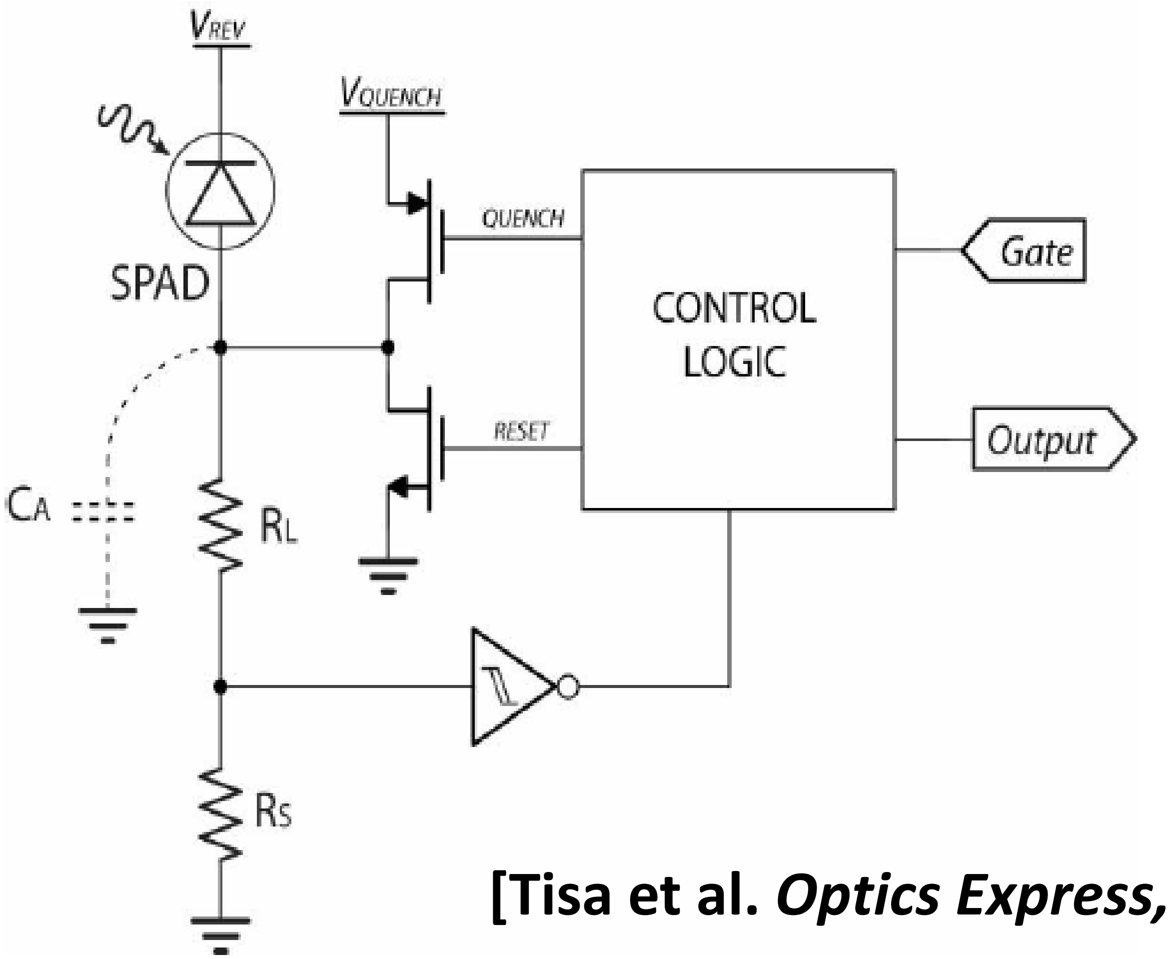
- CITIROC: D. Impiombato et alt. “Characterization and performance of the ASIC (CITIROC) front-end of the ASTRI camera, NIMA, Volume 794, 2015.
- MUSIC: S. Gomez et al., MUSIC: An 8 channel readout ASIC for SiPM arrays, in Proceedings, Optical Sensing and Detection IV, Brussels Belgium (2016) [SPIE Photonics Europe 9899 (2016) 98990G].
- PACIFIC: José Mazorra de Cos, Hervé Chanal, Albert Comerma Montells, David Gascón Fora, Sergio Gómez Fernández, Xiaoxue Han, Nicolas Pillet, Richard Vandaelle, “PACIFIC: SiPM readout ASIC for LHCb upgrade”, NIMA 2017.
- KLAUS: Z. Yuan at alt. “KLauS4: A Multi-Channel SiPM Charge Readout ASIC in 0.18µm UMC CMOS Technology”, PoS TWEPP-17 (2017) 030, SISSA (2017-12-21), DOI: 10.22323/1.313.0030
- MuTRiG: H. Chen et al., “A mixed signal Silicon Photomultiplier readout ASIC with high timing resolution and gigabit data link”, JINST 12 2017 C01043, HD-KIP 17-05
- PETIROC2: C. De La Taille et alt., “PETIROC2 : 32 ch SiGe SiPM readout ASIC for GHz time and charge measurement”, TIPP, 2014.
- TOFPET2: A. Di Francesco et alt. “A high-performance ASIC for time and amplitude measurements of SiPM signals in time-of-flight applications”, Journal of Instrumentation, Volume 11, March 2016.
- STIC3: H. Chan et al., “A dedicated readout ASIC for time-of-flight positron emission tomography using silicon photomultiplier (SiPM),” in Proc. IEEE NSS MIC Conf. Rec., Seattle, WA, USA, 2014, pp. 1–5.
- PETA6: . R. Dohle,T. Rittweg, I. Sacco, “Small form-factor, liquid-cooled SiPM module for PET/MRI applications”, EMPC 2017, DOI: 10.23919/EMPC.2017.8346828
- HRFlexToT: poster in this forum.
- SPHIRA: D. Meier, “SIPHRA 16-- Channel SiPM Readout ASIC”, NDIP 2017
- P. Calò et alt, "BASIC64: A new mixed-signal front-end ASIC for SiPM detectors," 2016 IEEE NSS/MIC/RTSD, Strasbourg, 2016, pp. 1-5.

Outlook

I. SiPM signal
II. Front End
III. Digitization
IV. Digital Sensors

IV. Digital SPADs

- Mixed passive-active quenching and reset



[Tisa et al. *Optics Express*, 2008]

IV. Digital SPADs

- Active vs. passive quenching

Passive quenching

- limits the maximum admissible photon counting rate
- Passive quenching does not allow hold-off

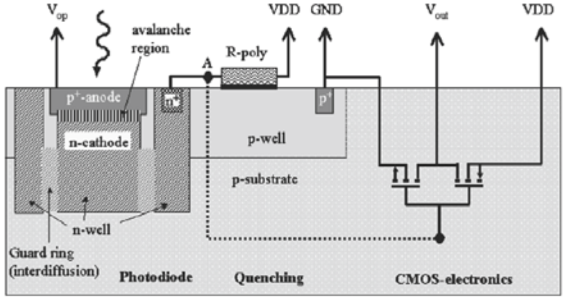
Active quenching

- Constant duration of the pulses
- Speeding up quenching → minimizes power dissipation
- Permits user defined hold-off → reduces afterpulsing
- Reduces dead-time

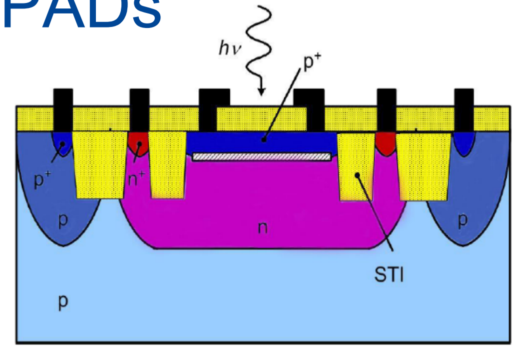
[R. Carmona, BarcelonaTechnoWeek, 2016]

IV. Digital SPADs

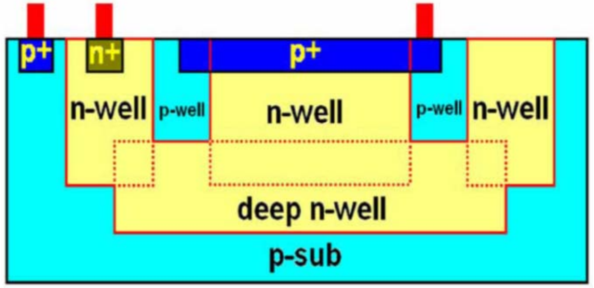
- CMOS-compatible SPADs



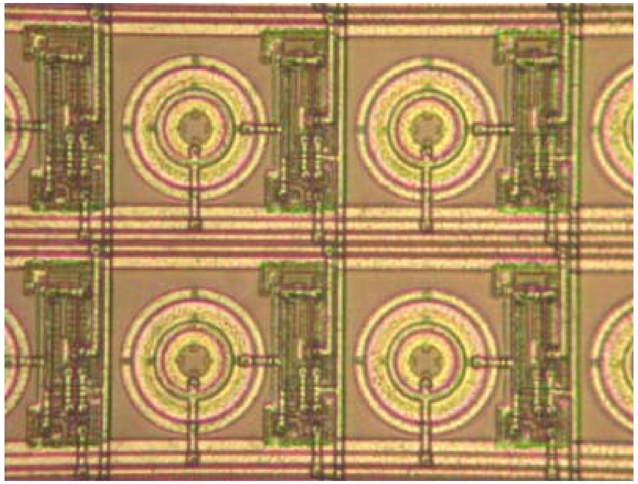
- **[Niclass, IEEE JSTQE, 2004]**
  - **SPAD array 0.8um HV CMOS**
  - **(EPFL, Switzerland, 2004)**

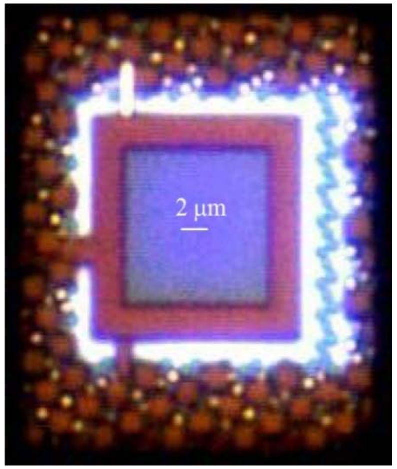


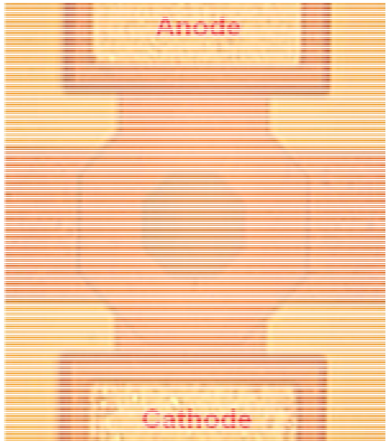
- **[Finklestein. Proc. SPIE, 2006]**
- **Single SPAD in 0.18um CMOS**
- **(UCSD, USA, 2006)**



- **[Faramarzpour. IEEE TED, 2008]**
- **Single SPAD in 0.18um CMOS**
- **(McMaster Univ., Canada, 2008)**





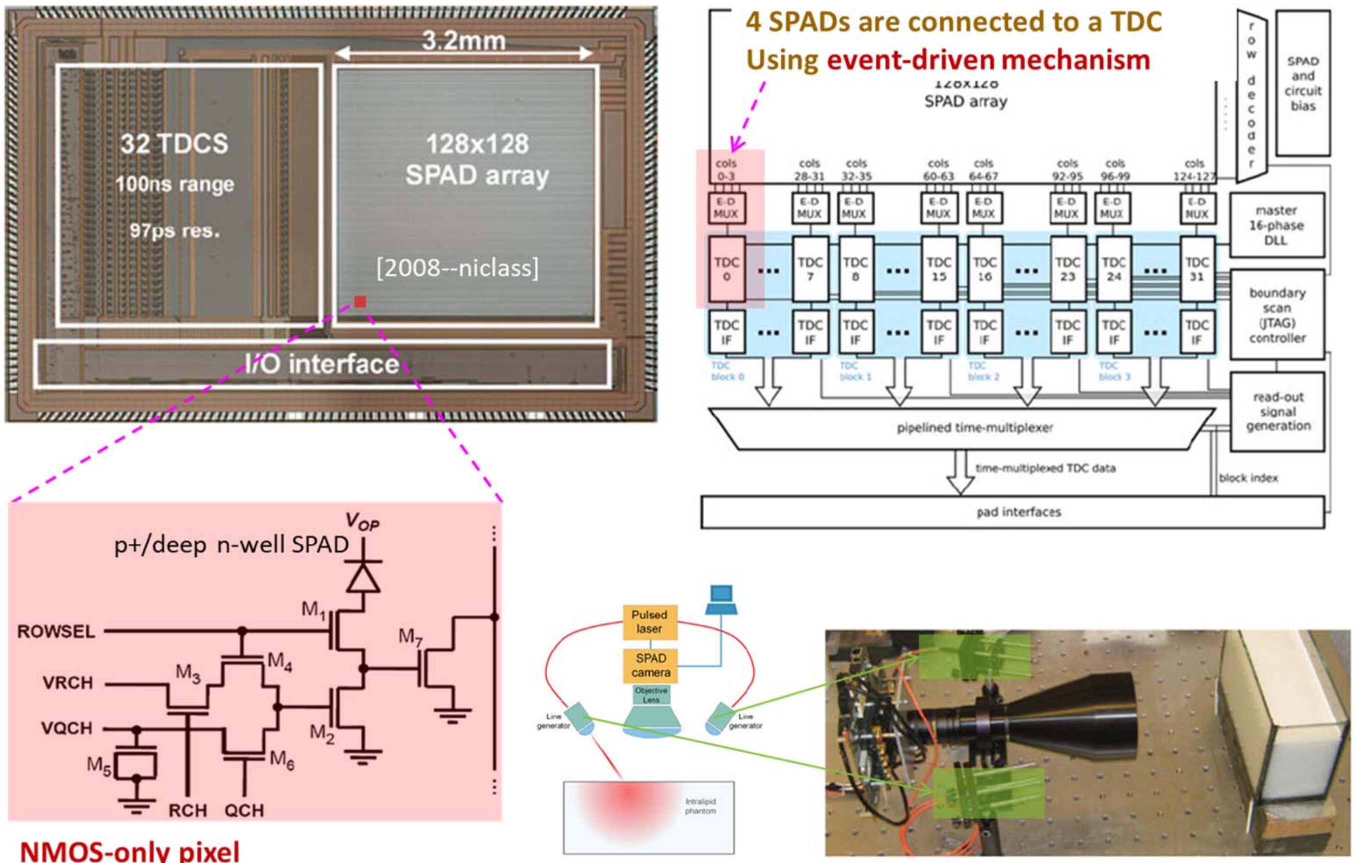


[R. Carmona, BarcelonaTechnoWeek, 2016]

IV. Digital CMOS SPADs imagers

3D NIR imaging with time-gated SPADs

[Pavia, IEEE JSTQE 2012]



4 SPADs are connected to a TDC
Using **event-driven mechanism**

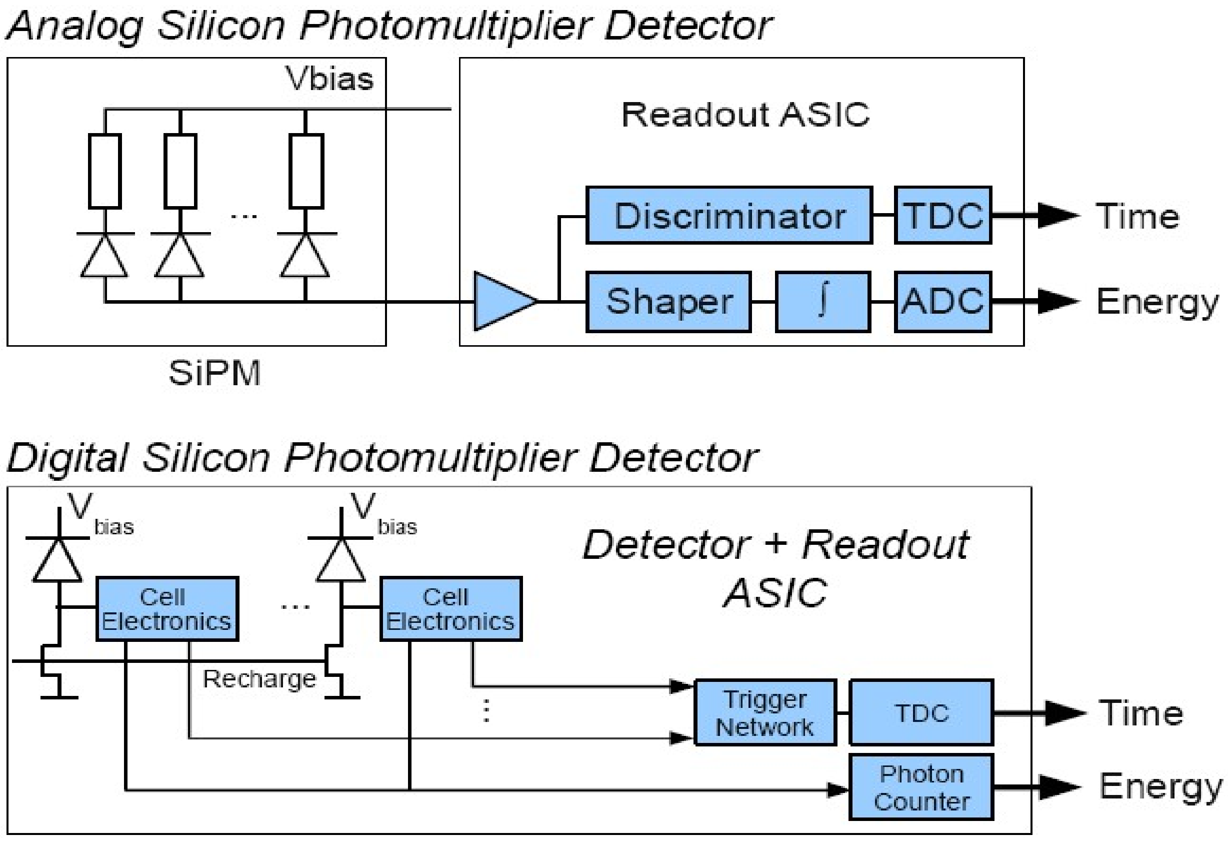
NMOS-only pixel

NIRI setup in reflection mode

[R. Carmona, BarcelonaTechnoWeek, 2016]

IV. Digital SiPMs

- Digital SiPMs are based on digital SPADs but **are not** imagers
- Digital SiPM counts photons in digital domain



YH

©Philips Digital Photon Counting, February 2011

6

IV. Digital SiPMs

- Not so new… so why digital is not ubiquitous?

- It is indeed somewhere
  - Philips Vereos PET
    - CTR < 300 ps FWHM
    - Better results with aSiPMs

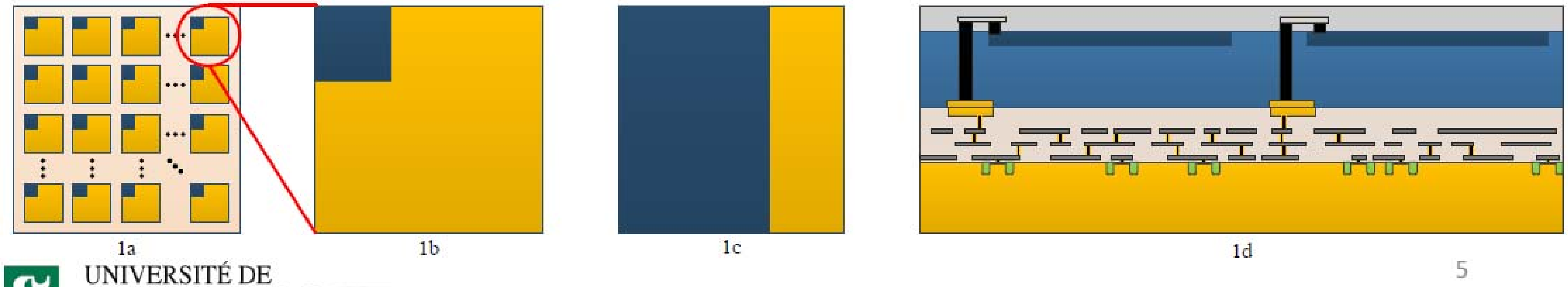
- Still.. Why so limited impact?

1. Electronics in the pixel limits fill factor and thus PDE
2. Based on pure CMOS technology
   - Dedicated SiPMs processes still better in high end applications
3. Read-out and trigger scheme are quite rigid and limited
   - DCR limits trigger efficiency
   - Difficult to use in other applications than PET

IV. 3D digital SiPMs

- 3D integration may help to overcome these limitations

- Monolithic issues
  - Electronics circuit limits the active area
    - Trade off between active area (1b) or performance (1c)
  - Compromise between photo-detector and electronics technology
- 3D solves most issues
- Main challenge
  - Connect each diode on photo-detector chip to quenching electronics chip



UNIVERSITÉ DE SHERBROOKE

3D integrated digital SiPM F. Retiere (TRIUMF) & U. de Sherbrooke (Sherbrooke)

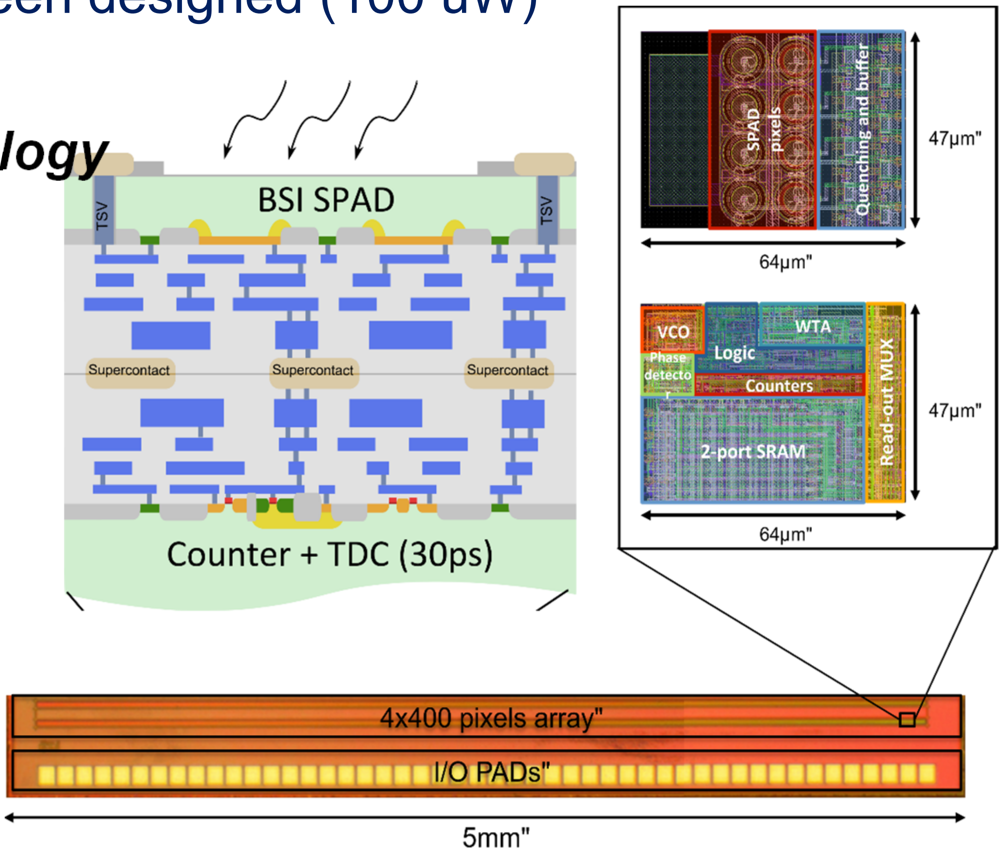
IV. 3D digital SiPMs

- 3D integration allows 1 TDC per SPAD: no interconnection problem
- Very low power TDCs have been designed (100 uW)

SPAD arrays in CMOS technology
Research at TU Delft//EPFL
(group of E. Charbon):

- **SPADnet**
- **3D-integration (flip chip)**

Courtesy of E. Charbon



J. Mata Pavia, M. Wolf, E. Charbon, IEEE NSS, 2014

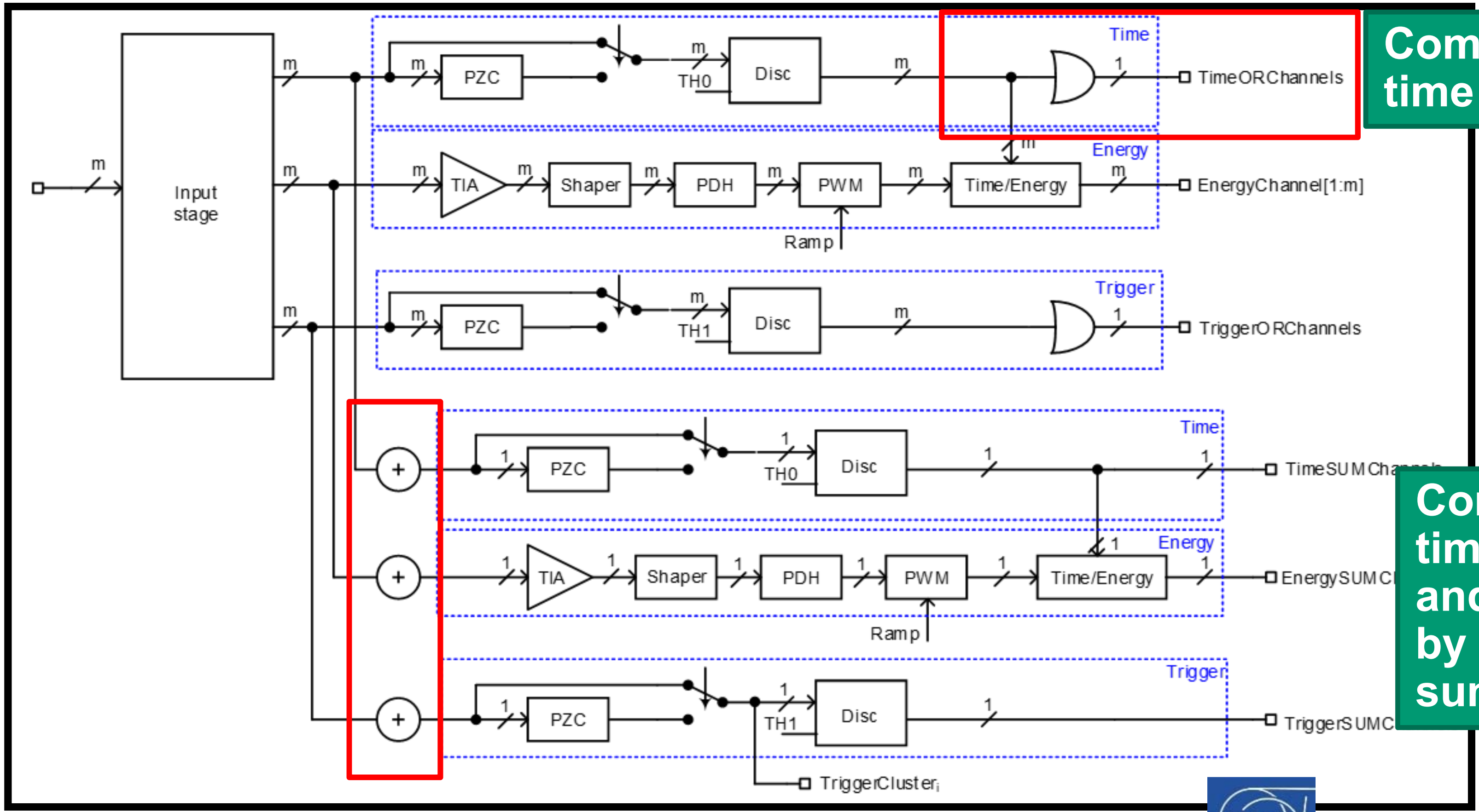
Thanks a lot for your attention !!!

Questions ?

dgascon@fqa.ub.edu

V. Hybrid sensors: 3D mixed-mode SiPMs

- Already working on the concept (ICCUB + CERN):
  - FASTIC: highly reconfigurable FE chip in 65 nm
  - FASTPIX: pixelated version in our roadmap…

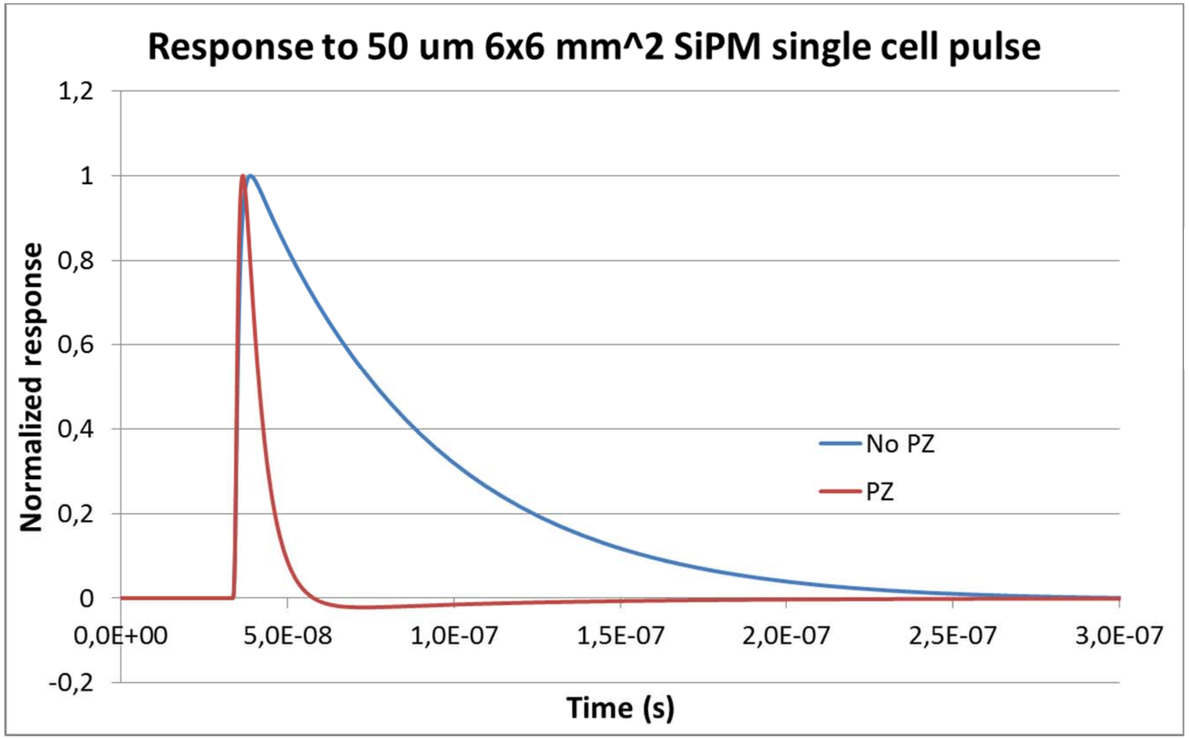


Combined time by OR

Combined time, energy and trigger by analog summation

III. FE circuits: Pole-Zero cancellation

- Pole-Zero (PZ) cancellation of the SiPM recovery long time constant (τ_{slow})
- The PZ shaping has an effect in the signal to noise ratio (SNR)
  - A SNR>5 is required for photopeak identification
  - Can be seen in 2 different ways:
    1) Attenuation of slow frequency components of the signal
    2) Increase of the input referred noise (ENC=Equivalent Noise Charge)

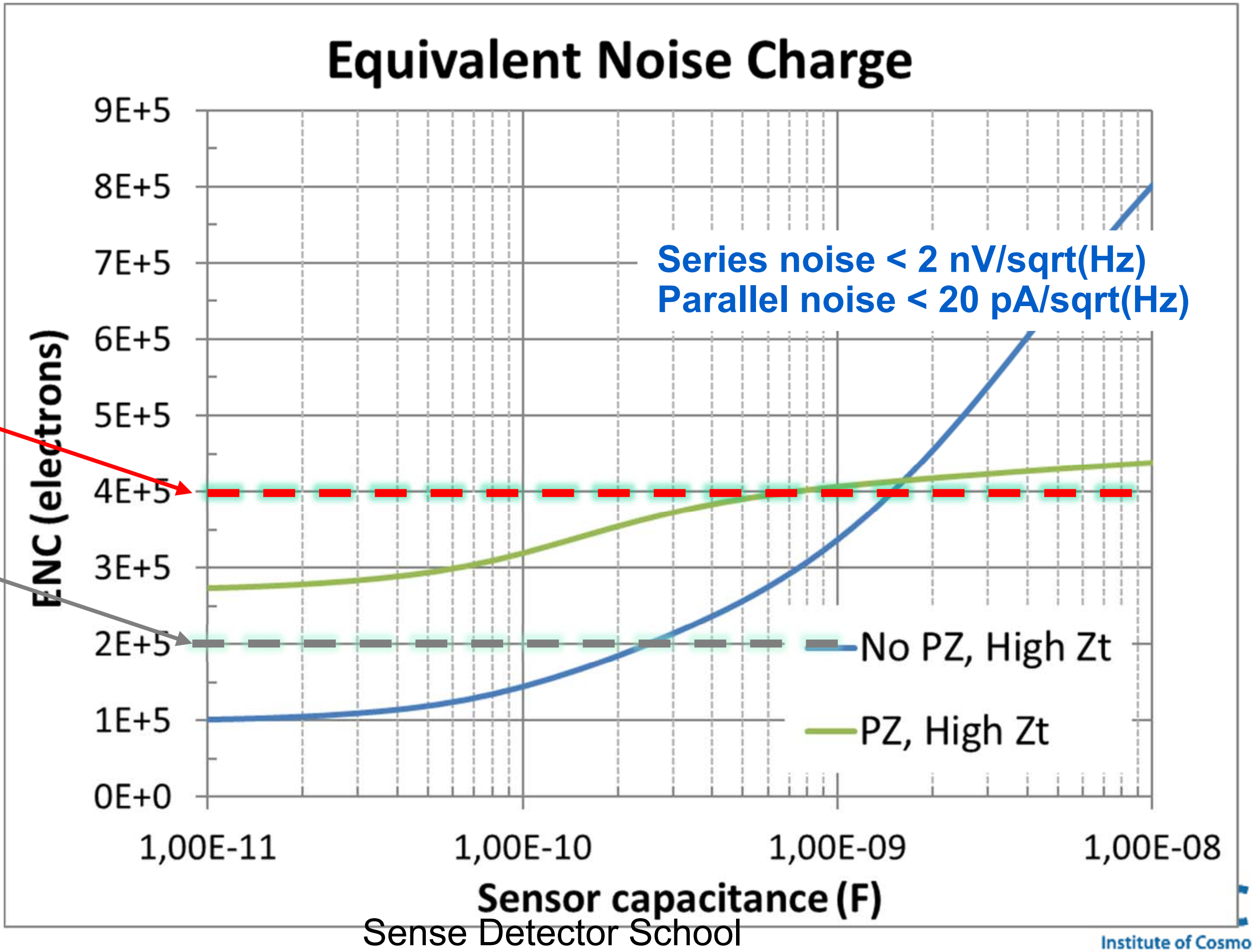


Simulation with a model obtained from 3x3 mm device

III. FE circuits: effect of capacitance and shaping in noise

- Front end electronics for SiPM is needed to:
  - Low noise front end is required for large SiPMs

SiPM capacitances range from 10s pF to more than several nF



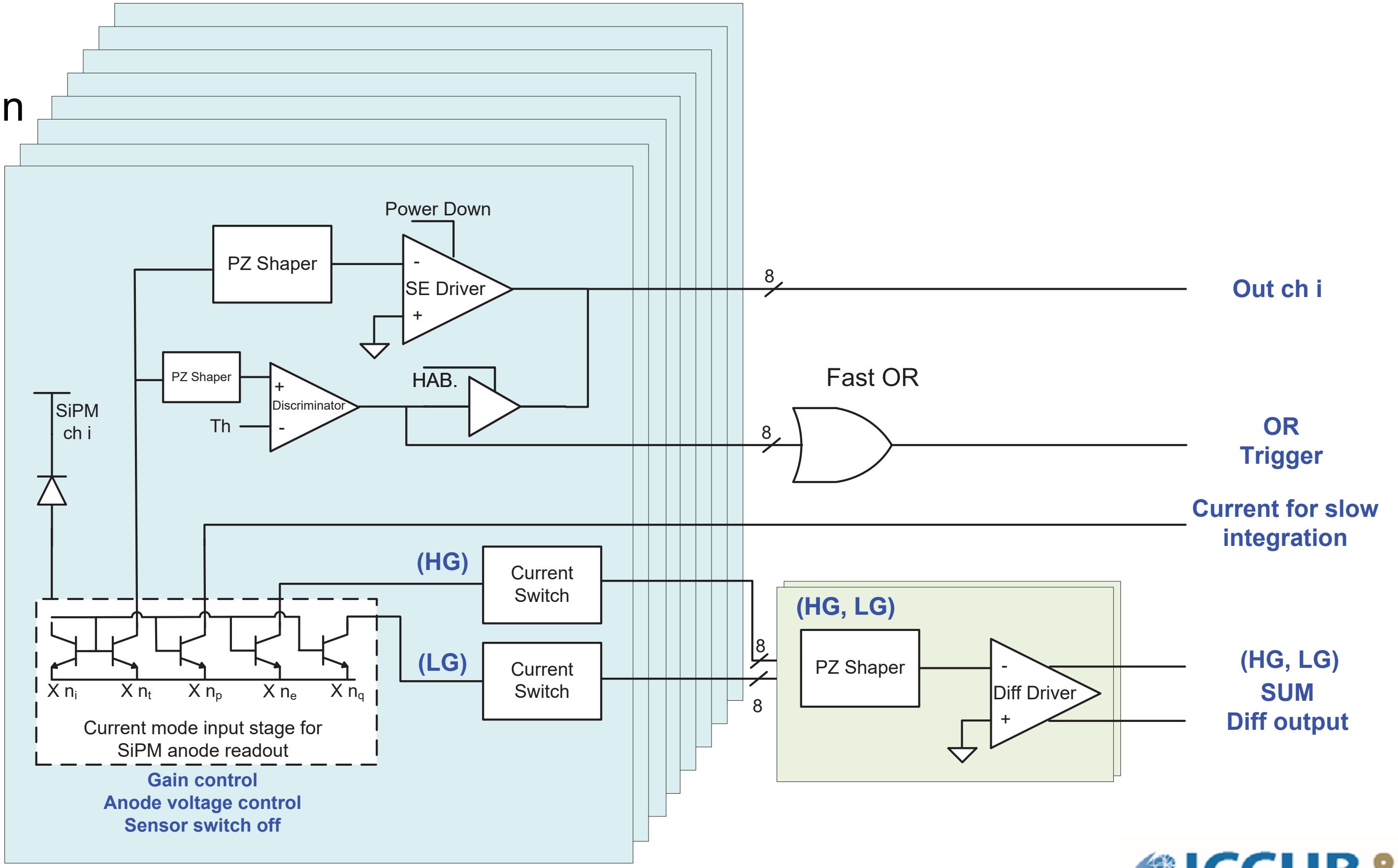
Series noise < 2 nV/sqrt(Hz)
Parallel noise < 20 pA/sqrt(Hz)

ENC_{max} for SNR>5 @ $2*10^6$ nominal gain

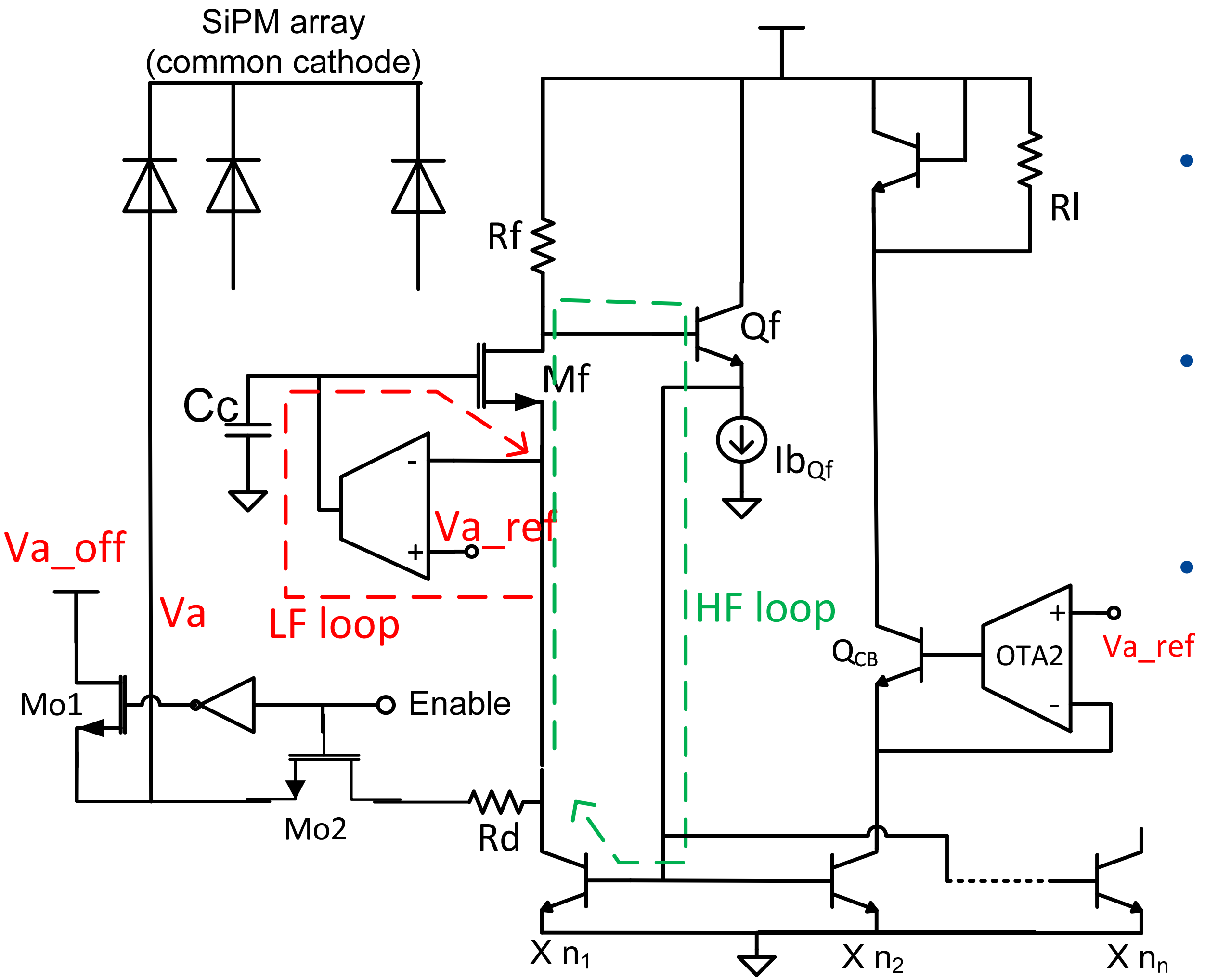
ENC_{max} for SNR>5 @ $1*10^6$ nominal gain

III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- MUSIC: current mode, analog (binary) and designed for astroparticle (CTA) but multipurpose
  - Amplification / impedance adaptation
  - Pole zero cancellation
  - Summation
  - Discrimination



III. FE circuits: MUSIC: Multipurpose SiPM RO chip



- Possible to disable each input reducing overvoltage to Va_off.
- Double feedback loop
  - Low input impedance
  - Anode voltage control
- High bandwith

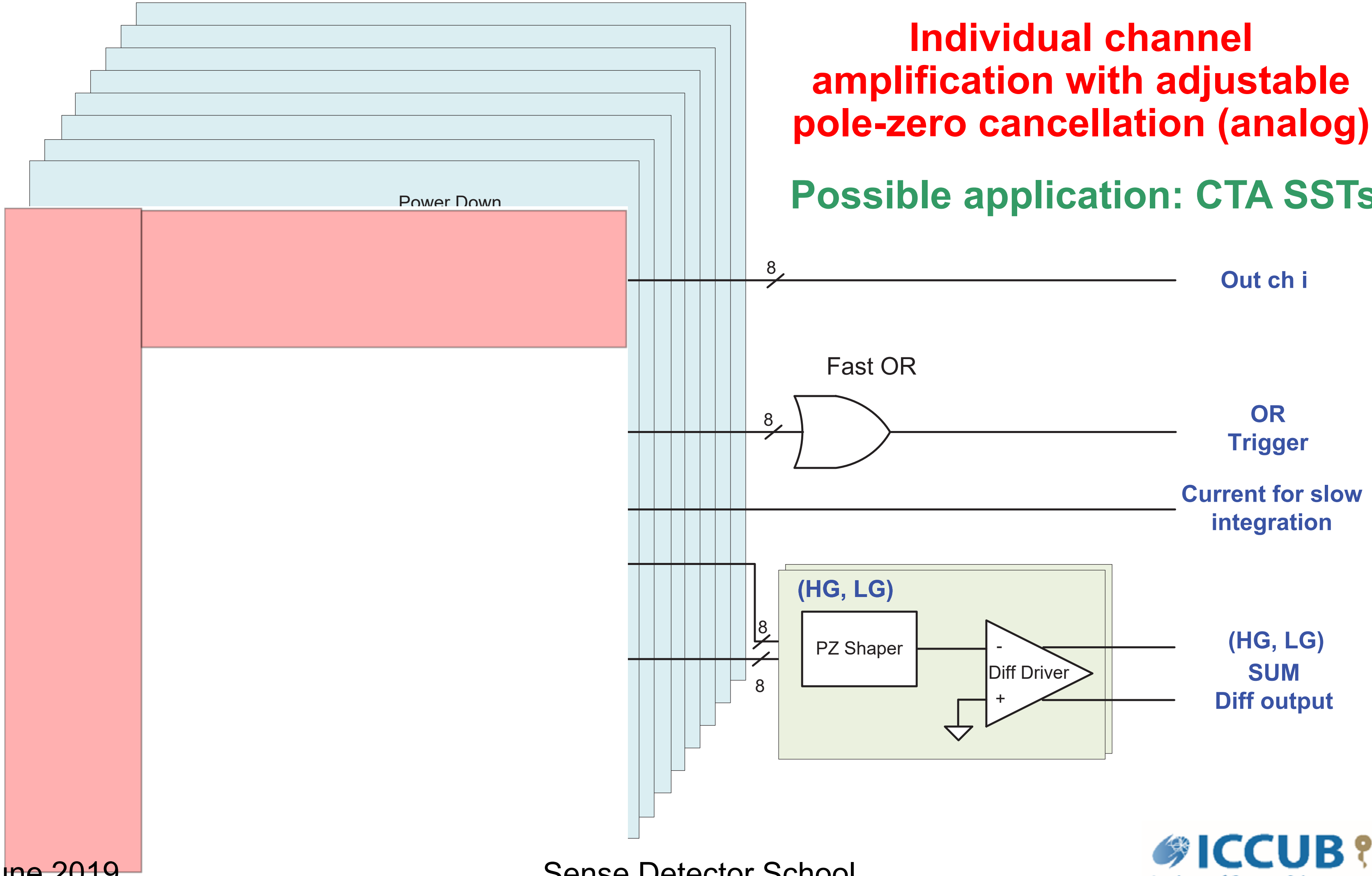
Series noise < 2 nV/sqrt(Hz)
Parallel noise < 20 pA/sqrt(Hz)

III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- MUSIC 8 ch ASIC integrates all those functionalities

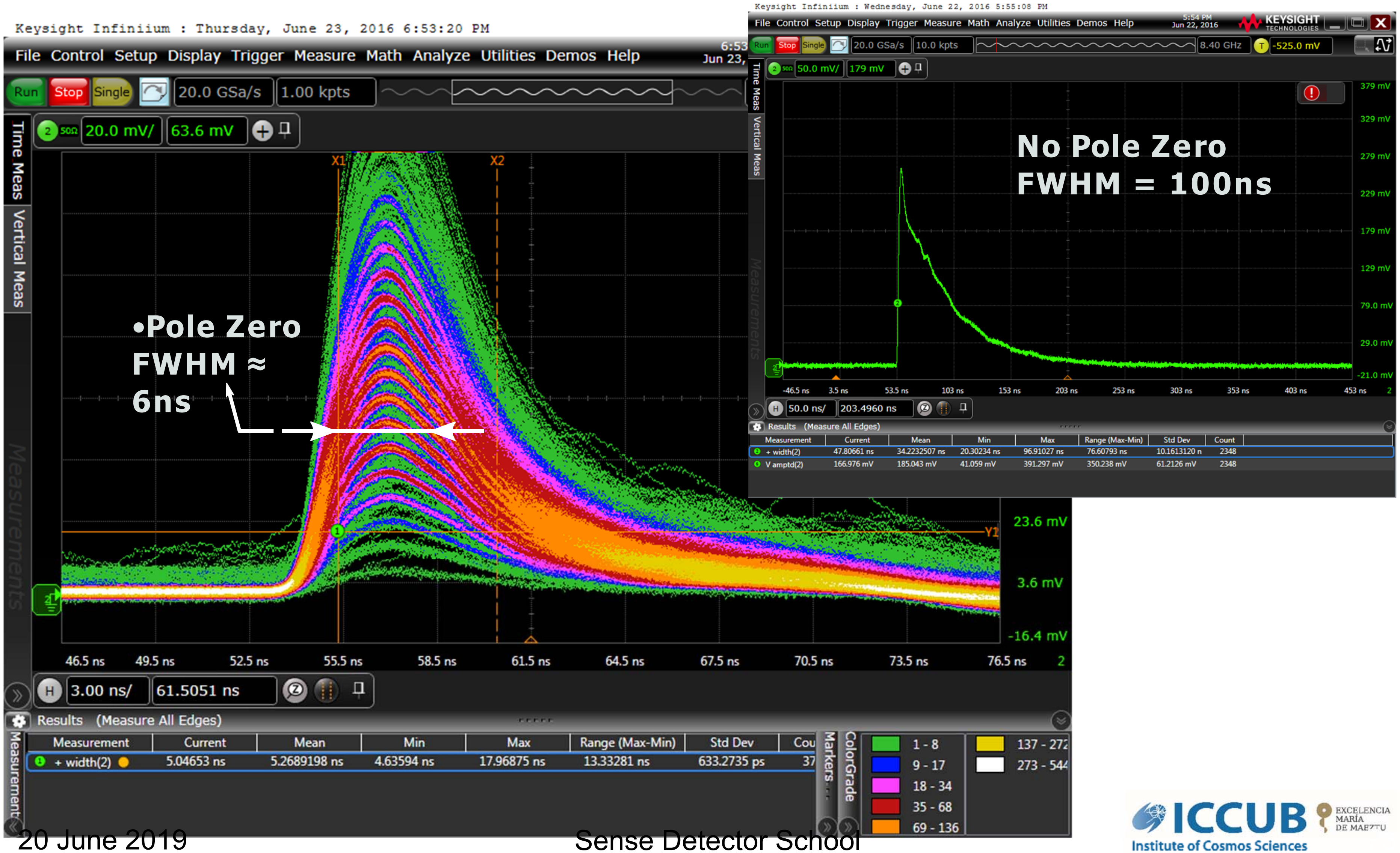
Individual channel amplification with adjustable pole-zero cancellation (analog)

Possible application: CTA SSTs



III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Output for a LCT4 MPPC (3x3 mm^2)



•Pole Zero
FWHM ≈
6ns

No Pole Zero
FWHM = 100ns

Results (Measure All Edges)

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Cou
+ width(2)	5.04653 ns	5.2689198 ns	4.63594 ns	17.96875 ns	13.33281 ns	633.2735 ps	37

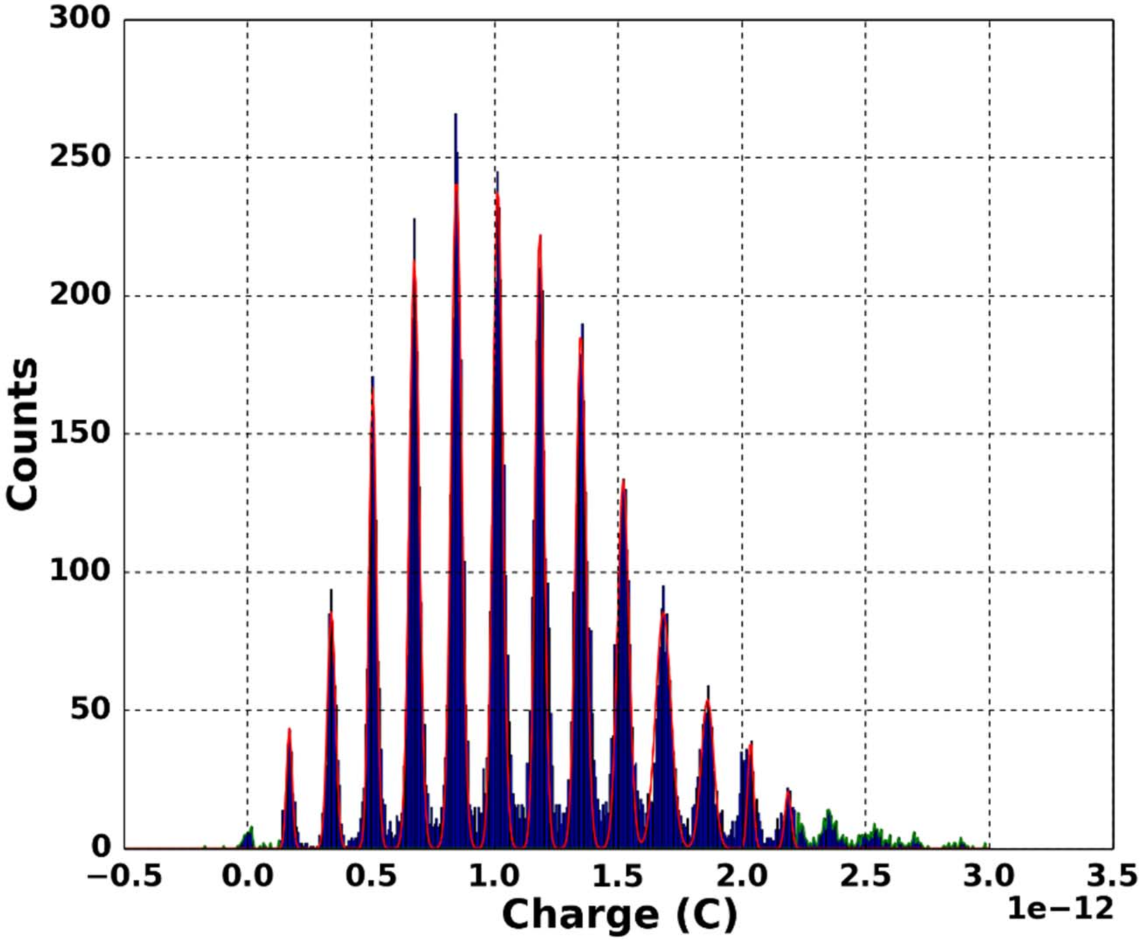
ColorGrade	
🟩	1 - 8
🟦	9 - 17
🟪	18 - 34
🟥	35 - 68
🟧	69 - 136
🟨	137 - 272
⬜	273 - 544

Results (Measure All Edges)

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
+ width(2)	47.80661 ns	34.2232507 ns	20.30234 ns	96.91027 ns	76.60793 ns	10.1613120 n	2348
V amptd(2)	166.976 mV	185.043 mV	41.059 mV	391.297 mV	350.238 mV	61.2126 mV	2348

III. FE circuits: MUSIC: Multipurpose SiPM RO chip

- Charge spectrum for a LCT4 MPPC (3x3 mm^2)
- Pole-zero cancellation
- Excellent resolution with FWHM of 5 ns

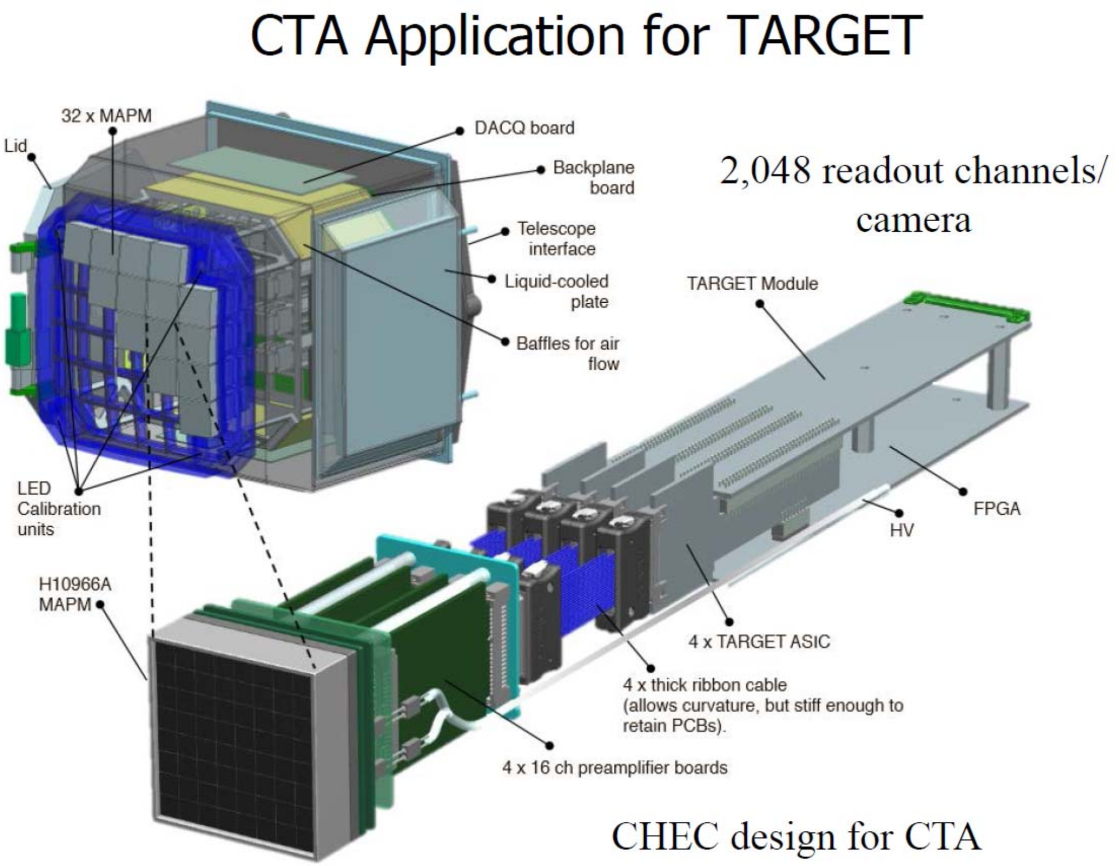


III. FE circuits: conclusions

- Despite the variety of applications and the zoology of ASICs some common requirements and functionalities for the analog FE:
  - Impedance adaptation
  - Low noise current or voltage sensing
  - Shaping, pole-zero cancellation
- Analog signal summation can be used to create efficient large area sensors
  - Although independent readout of small devices will have better performance
  - Analog summation relaxes requirements on digitization and readout
  - As usual in electronics: trade-off !!
- ASICs can do all of that with low power consumption: 1-2 mW
  - SNR >> 10 for 6x6 mm^2 devices
  - Pulse width <5 ns for 6x6 mm^2 devices (PZ cancellation)
  - SPTR < 100 ps FWHM (small devices)
  - But in preamplifiers often the power explodes when low impedance drivers are required: example preamplifier that drives tx line to ADC / Waveform Sampler
    - System-On-Chips when possible !

V. ASICs summary: TARGET: waveform sampling

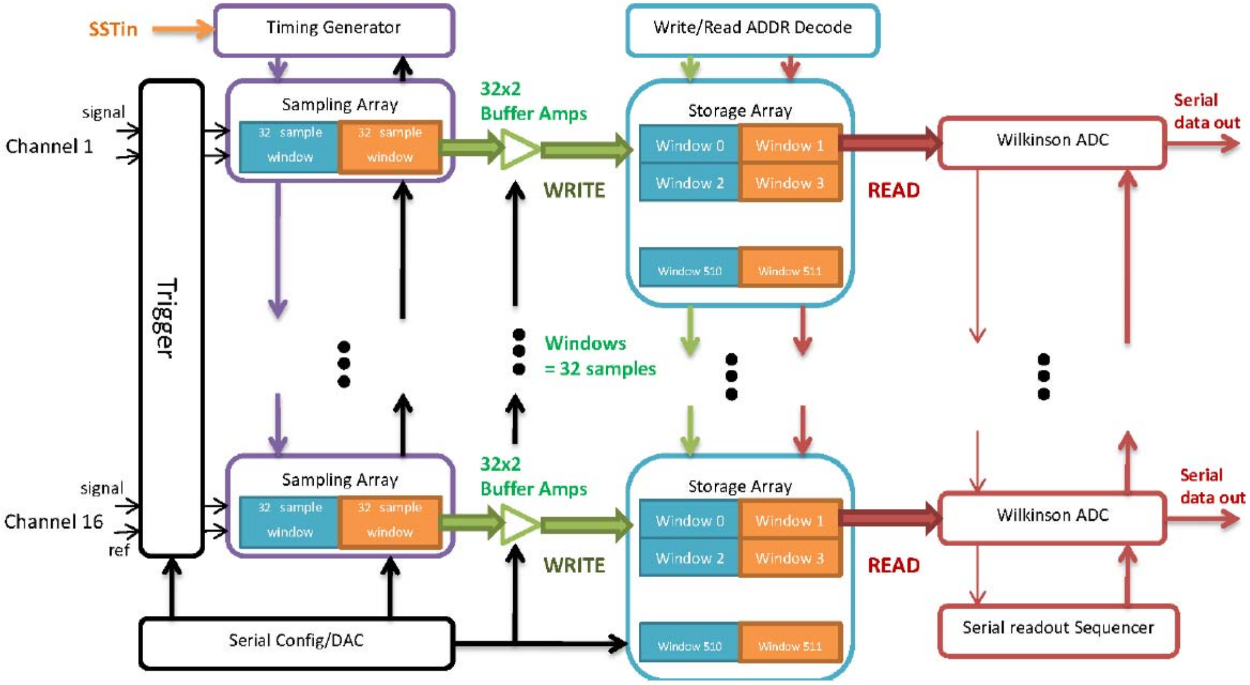
- CHEC camera is an interesting example of compact readout



Gary S. Varner, 2nd Adv SiPM Workshop, Geneva, 2014

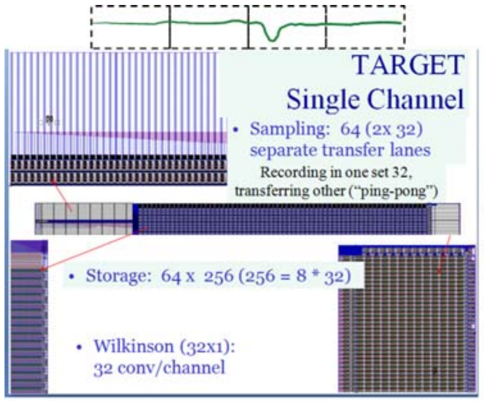
V. ASICs summary: TARGET: waveform sampling

- Several iterations to have a functional chip: TARGET7



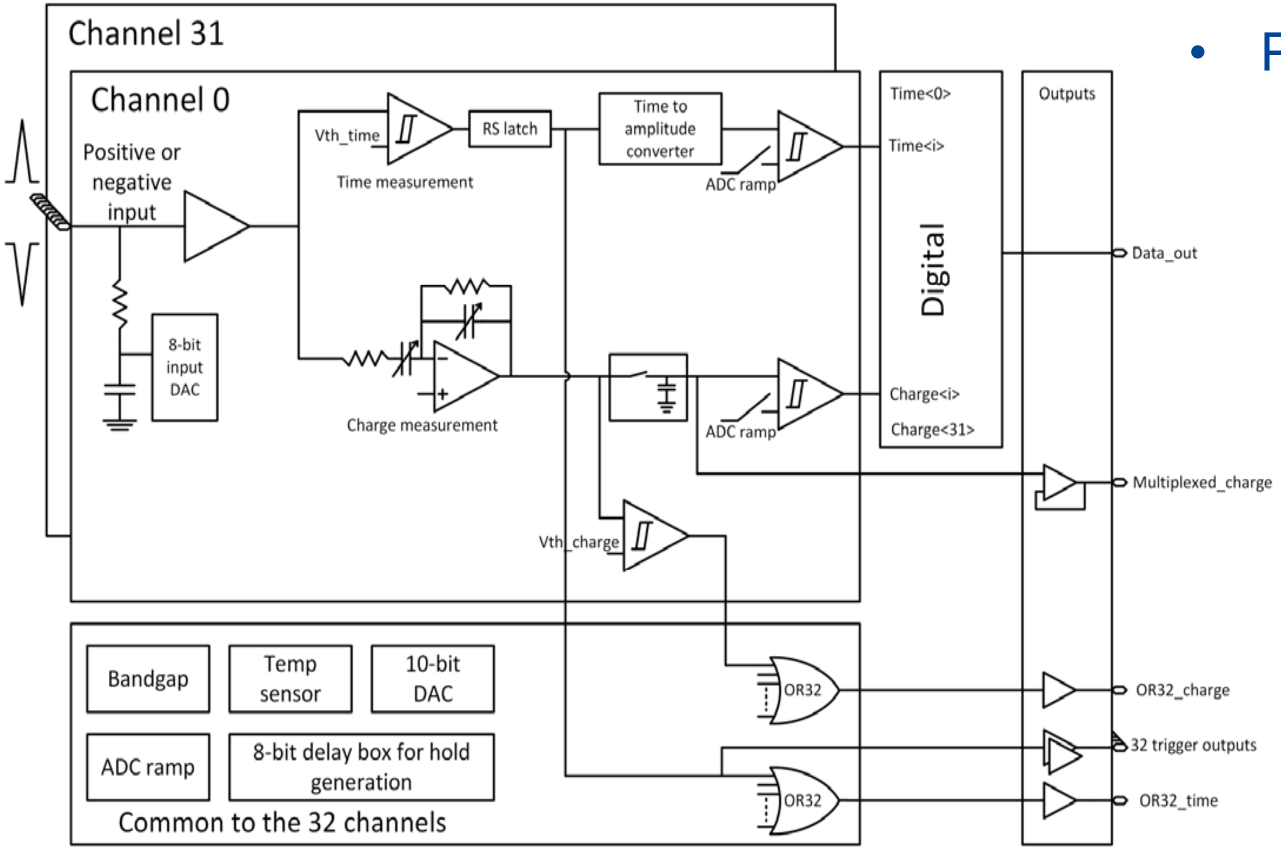
TARGET7 Specification Summary

16384	samples/chan (16-32us trig latency)
16	channels/TARGET ASIC
Σ4 --> 4	Trigger channels (indep. Thr/Width)
~9-10	bits resolution (12-bits logging)
32	samples convert window (~32-64ns)
0.5-1	GSa/s
1	word (RAM) chan, sample readout
<10	us to convert 512 samples (at once)
>100	kHz sustained readout (multibuffer)



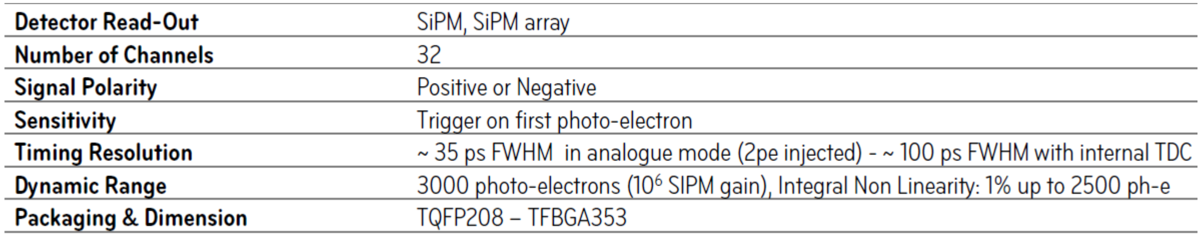
Gary S. Varner, 2nd Adv SiPM Workshop, Geneva, 2014

V. ASICs summary: **PETIROC**



- PETIROC2:
  - Voltage mode,
  - Configurable: analogue, binary or digital
    - S&H + Wilkinson ADC
  - For medical imaging (PET)
  - Versatile: analog or digital
  - But shaping time > 10 ns
  - Max ev. rate is 40 KHz in digital mode
  - Power:

https://www.weeroc.com/fr/products/petiroc-2a



Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP208 – TFBGA353

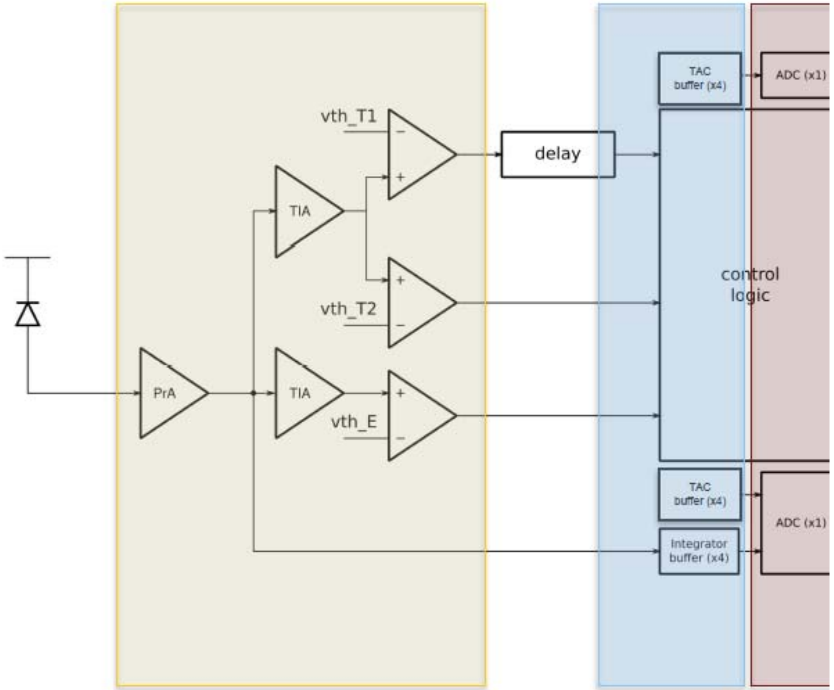
V. ASICs summary: TOFPET

- Pre-amplifier: low input impedance current conveyor
- Two post-amplifiers (TIA) for time and energy measurements
- Three leading edge discriminators;
  - Very low threshold (1-5 p.e.) for optimum PET time resolution
  - multi-level event rejection

- Time to Amplitude Converter (TAC)
- Charge Integrator (CI)
  - configurable integration windows
  - linear amplitude measurement
  - TAC and Charge Integrator are quad-buffered
    - No dead-time due to Poisson fluctuations

- Two 10-bit ADCs per channel
  - Time and amplitude measurements
  - Optionally: Time-over-Threshold

- TOFPET2: current mode, digital (linear ToT) and for medical imaging (PET)
  - Power: 8 mW/ch
  - Max rate 200 KHz/ch

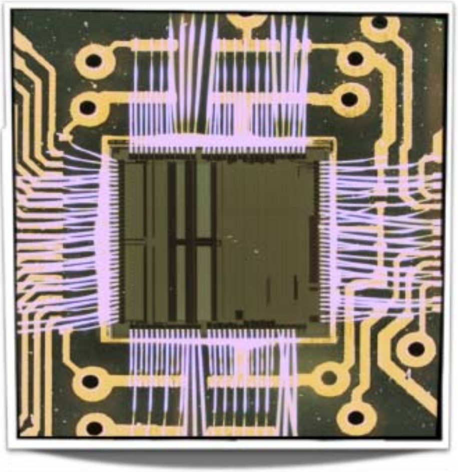


J. Varela, "New results with TOFPET2", FAST, Ljubljana, Jan 2018

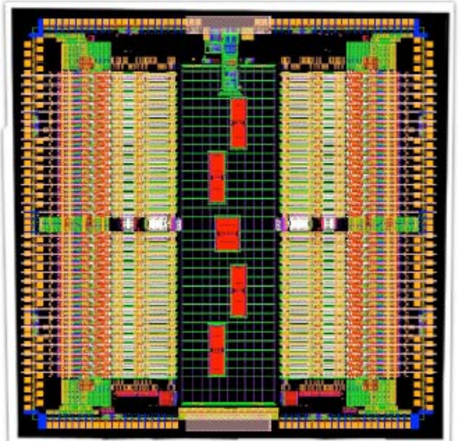
V. ASICs summary: STiC

- STiC: current mode, digital (linear ToT) and for medical imaging (PET)

STiC 2.1
[on test PCB]



STiC 3.0
[Chip layout]



Features:

STiC 2.1: 16 channels
STiC 3.0: 64 channels

Differential and single-ended readout …

Integrated TDC [ZITI, Fischer et al.] and digital data processing …

Timing and ToT-based linearized energy measurement …
[SPTR:180 ps; MPPC S10362-11-100]

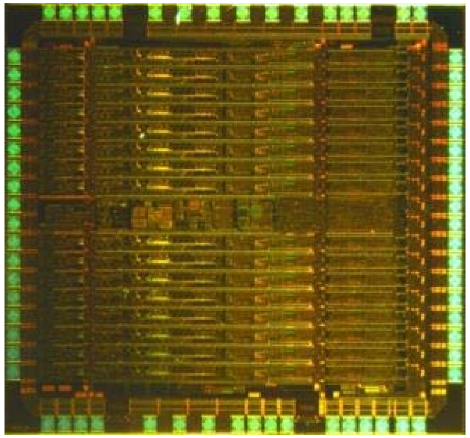
SiPM bias tuning …
[Tuning range: ~ 500 mV]

Serial interface for data transmission and configuration …

STiC — a mixed mode silicon photomultiplier readout ASIC for time-of-flight applications
T. Harion et alt., 2014 JINST 9 C02003

V. ASICs summary: FlexToT: linearized ToT RO chip

- Joint project with CIEMAT to develop a time-over-threshold ASIC for SiPM based PET
  - ICCUB: expertise on electronics and microelectronics design for detector FE
  - CIEMAT: expertise on PET and medical imaging instrumentation



FlexToT

16 channel

SiGe BiCMOS 0.35um

Aaustriamicrosystem

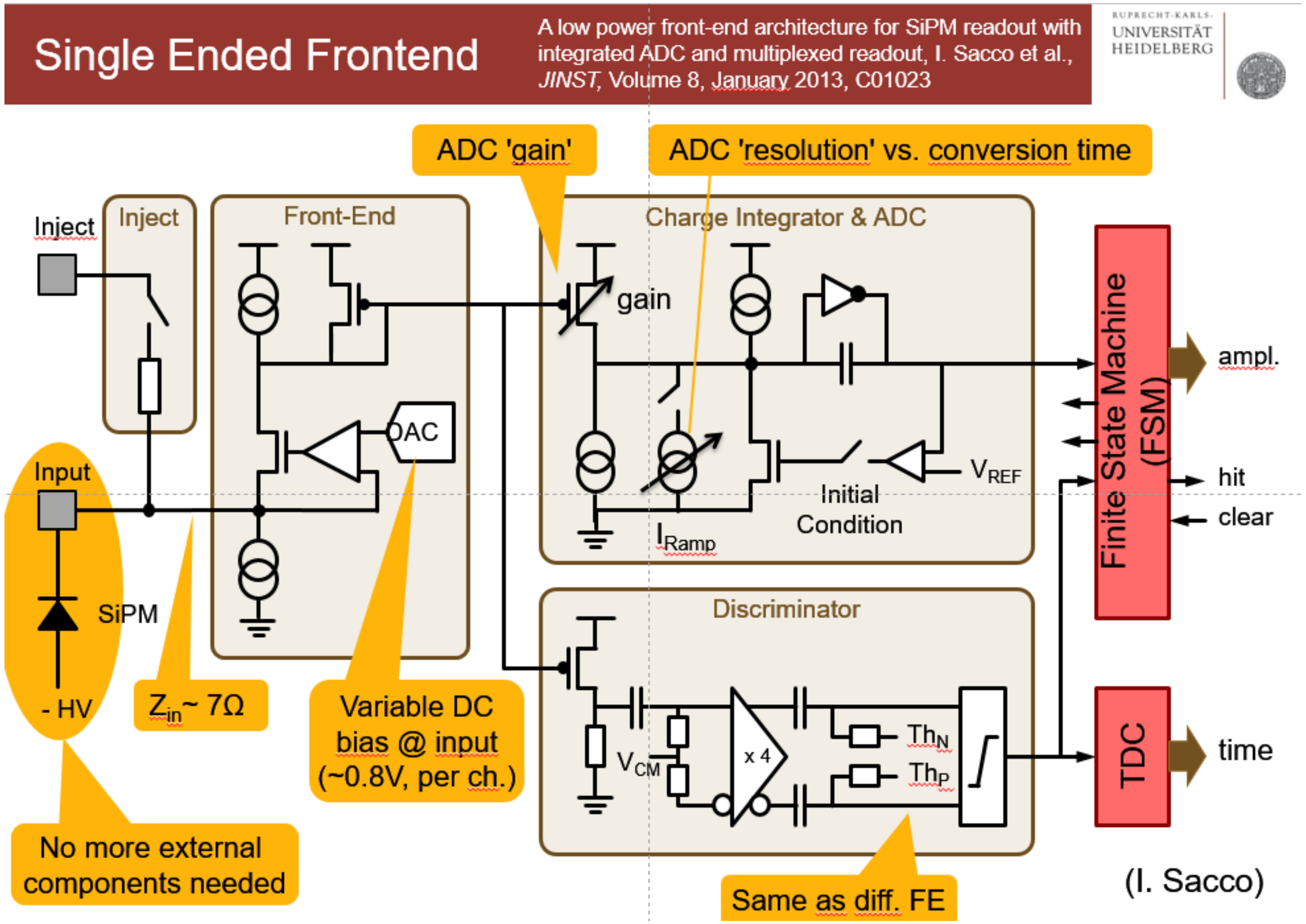
10 mm^2

3.3 V (10 mW/ch)

QFN 64

V. ASICs summary: PETA

- PETA: current mode, charge (ADC) and time (TDC), for PET
  - Choice between Differential FE (both polarities, MRT immune) and Single Ended FE (low Zin, DC bias adjustment, no external coupling parts)
  - Readout rates >200 kHz per channel (in all channels)
  - Power consumption ~30mW / channel



Single Ended Frontend

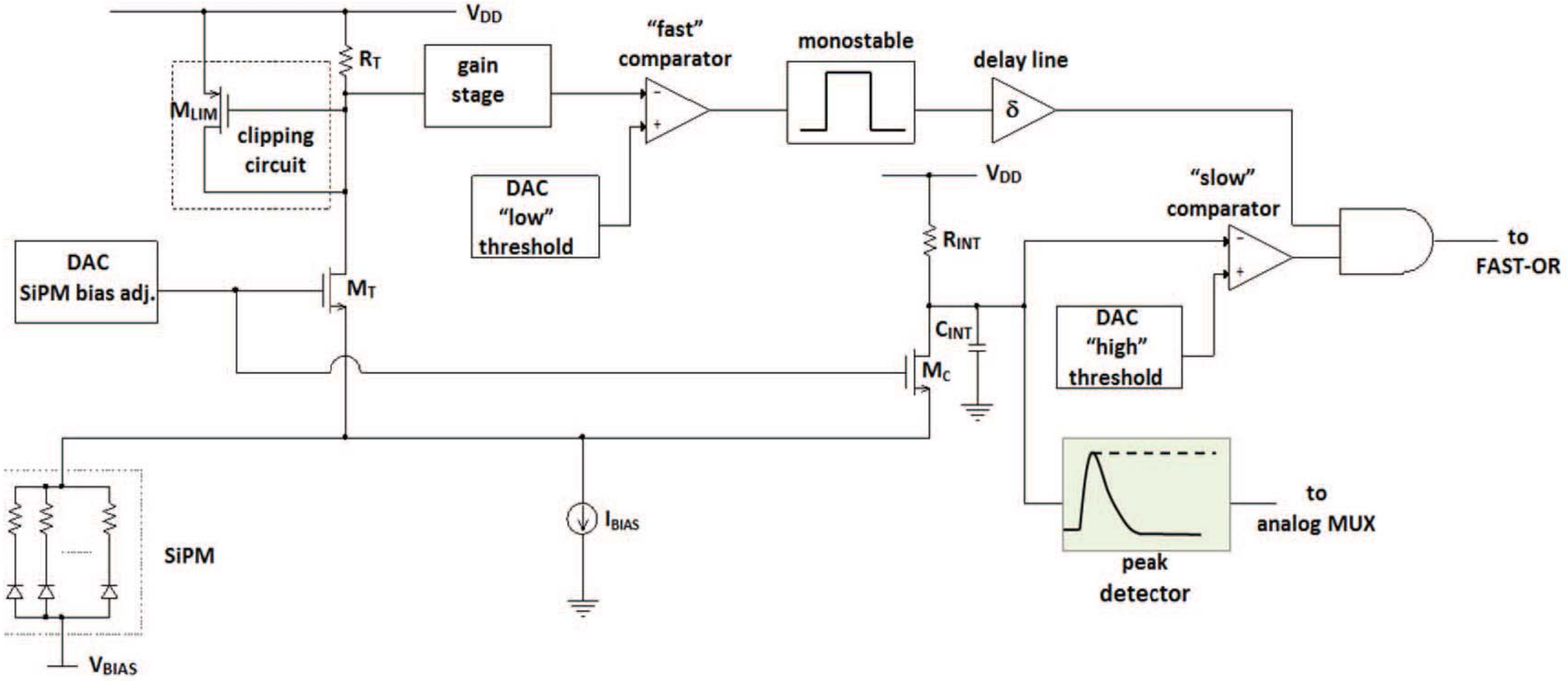
A low power front-end architecture for SiPM readout with integrated ADC and multiplexed readout, I. Sacco et al., *JINST*, Volume 8, January 2013, C01023

(I. Sacco)

P. Fischer, Heidelberg University, The PETA Chip Family FAST Workshop, FBK 2016

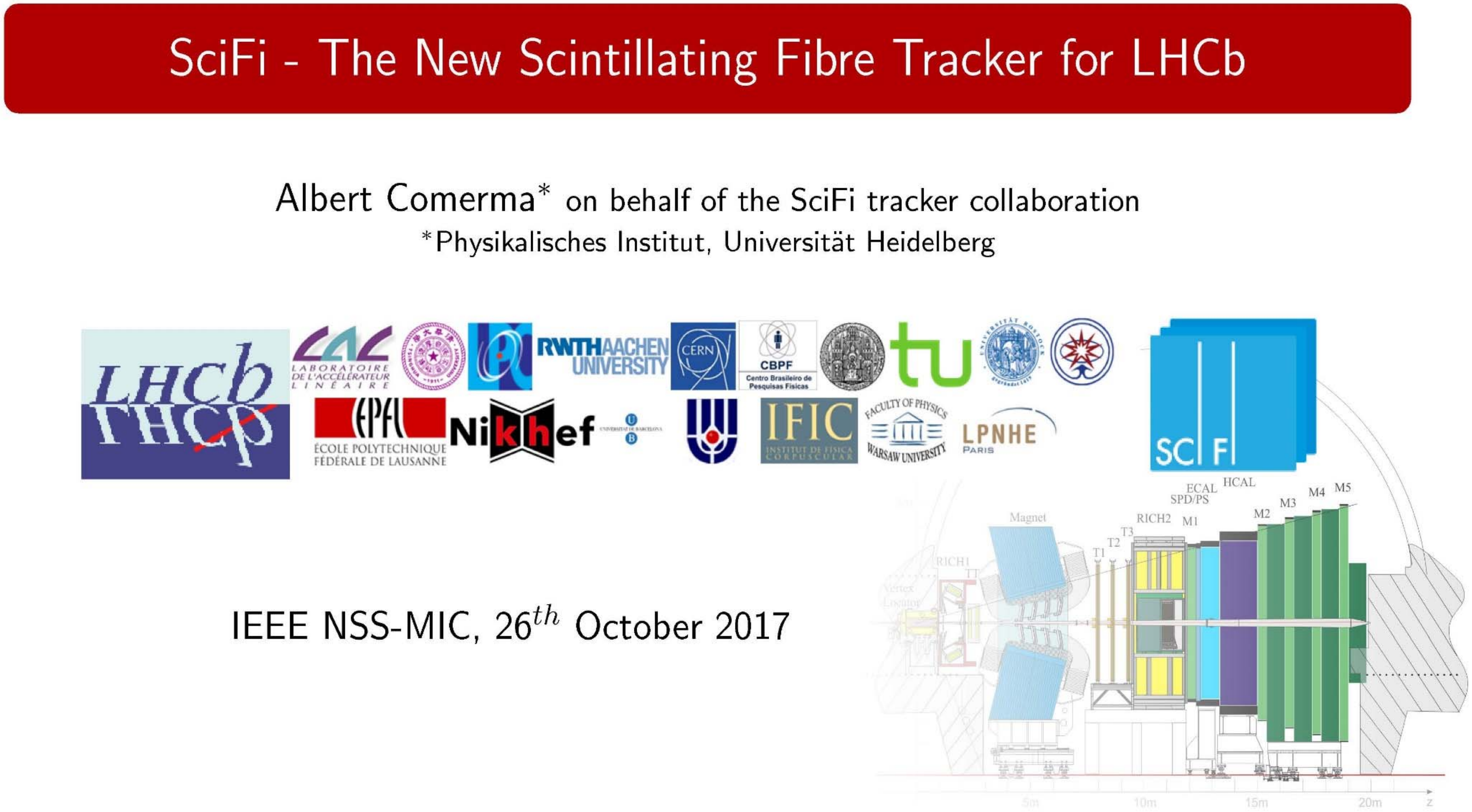
V. ASICs summary: BASIC64

- BASIC64: current mode, digital (peak detector + ADC) and for PET
  - Power: 10 mW/ch
  - Max rate: 75 KHz/ch
  - No TDC for timing



C. Marzocca et alt., "BASIC64: A new mixed-signal front-end ASIC for SiPM detectors," NSS 2016

V. ASICs summary: PACIFIC



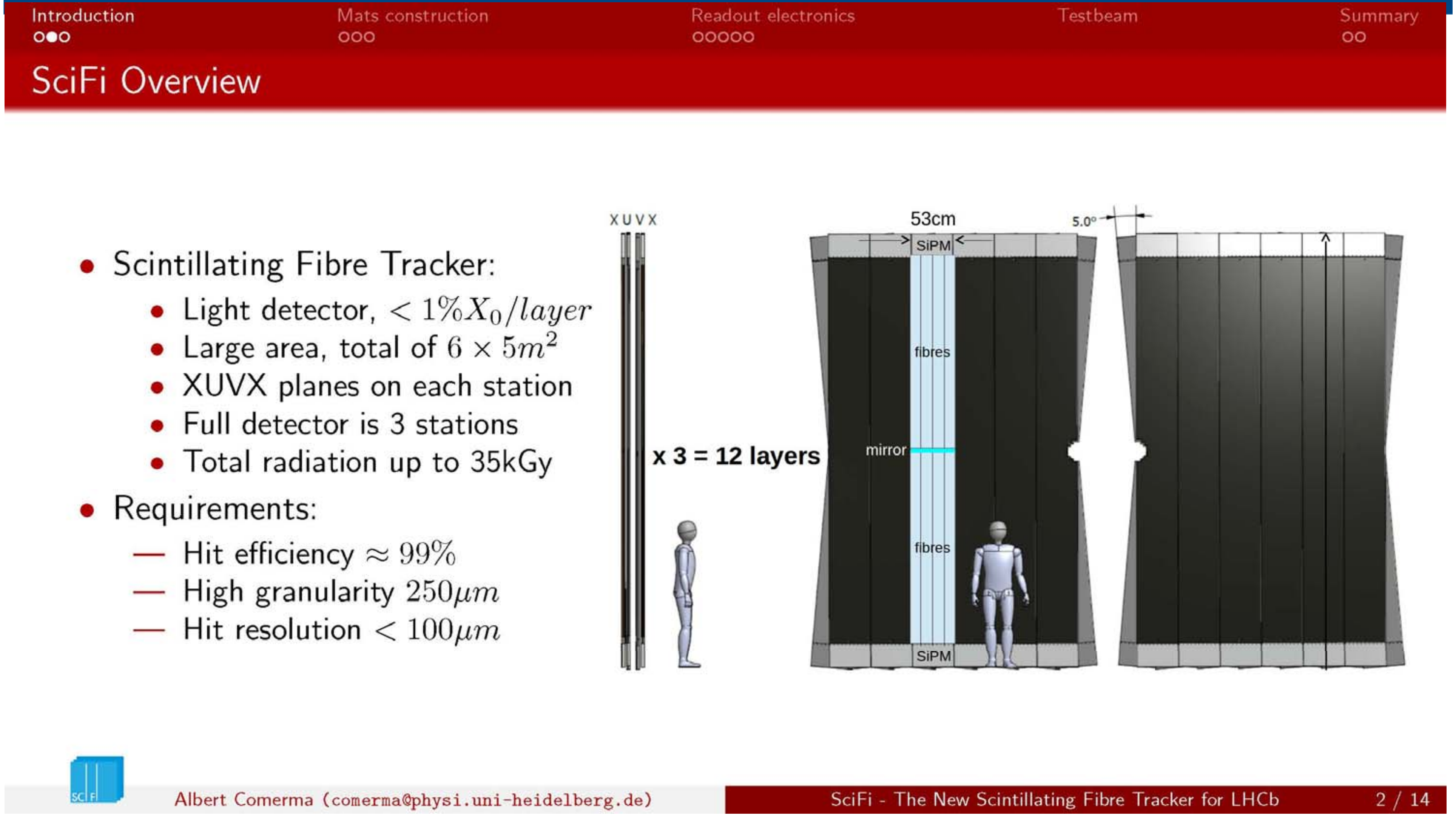
SciFi - The New Scintillating Fibre Tracker for LHCb

Albert Comerma* on behalf of the SciFi tracker collaboration

*Physikalisches Institut, Universität Heidelberg

IEEE NSS-MIC, 26th October 2017

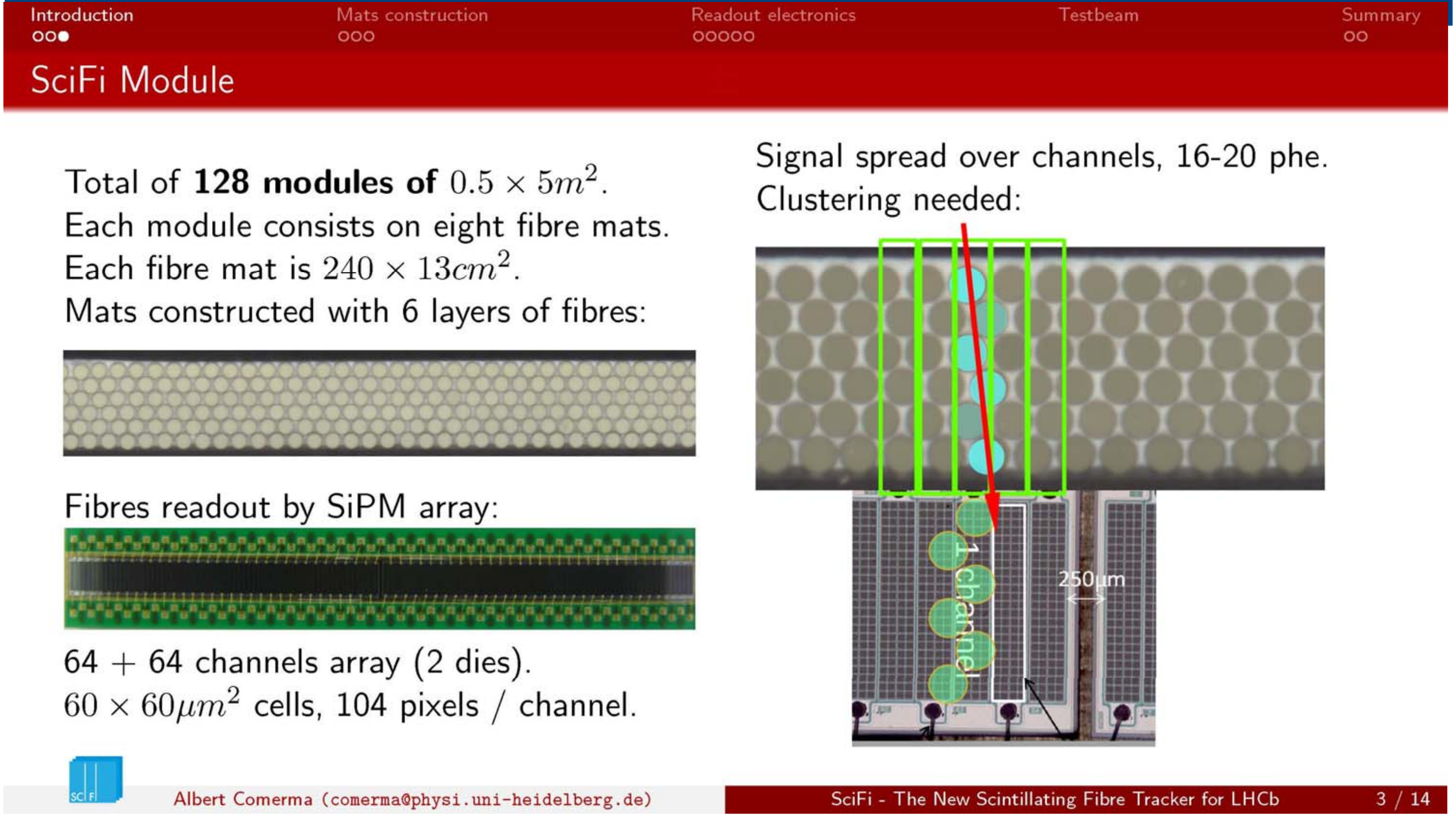
V. ASICs summary: PACIFIC



SciFi Overview

- Scintillating Fibre Tracker:
  - Light detector, $< 1\% X_0/layer$
  - Large area, total of $6 \times 5m^2$
  - XUVX planes on each station
  - Full detector is 3 stations
  - Total radiation up to 35kGy
- Requirements:
  - — Hit efficiency $\approx 99\%$
  - — High granularity $250\mu m$
  - — Hit resolution $< 100\mu m$

V. ASICs summary: PACIFIC



Introduction ○○● Mats construction ○○○ Readout electronics ○○○○○ Testbeam Summary ○○

SciFi Module

Total of **128 modules of** $0.5 \times 5m^2$.
Each module consists on eight fibre mats.
Each fibre mat is $240 \times 13cm^2$.
Mats constructed with 6 layers of fibres:

Fibres readout by SiPM array:

64 + 64 channels array (2 dies).
$60 \times 60\mu m^2$ cells, 104 pixels / channel.

Signal spread over channels, 16-20 phe.
Clustering needed:

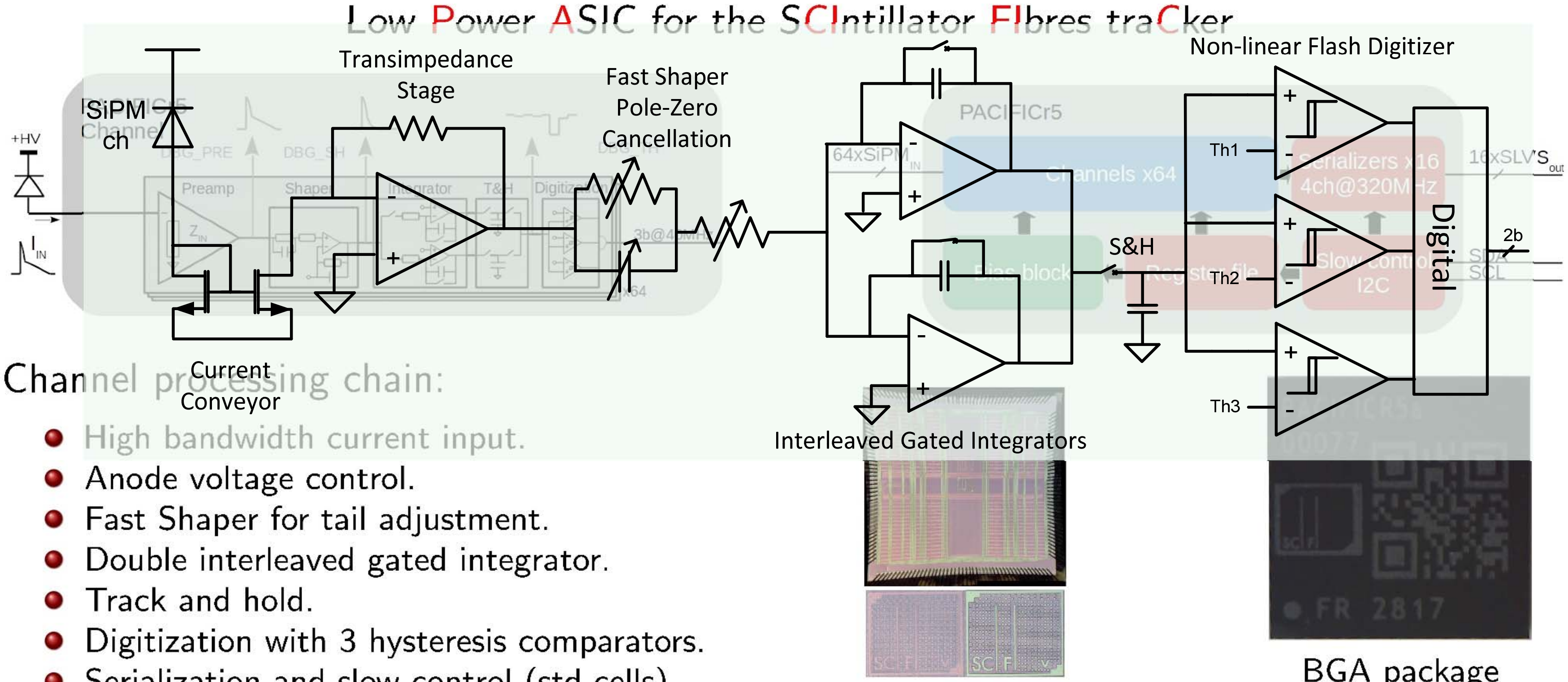
Albert Comerma (comerma@physi.uni-heidelberg.de) SciFi - The New Scintillating Fibre Tracker for LHCb 3 / 14

V. ASICs summary: PACIFIC

PACIFIC

Collaboration: Heidelberg, ICCUB , LPC-Clermont, IFIC-Valencia

Low Power ASIC for the SCIntillator FIbres traCker



Channel processing chain:

- High bandwidth current input.
- Anode voltage control.
- Fast Shaper for tail adjustment.
- Double interleaved gated integrator.
- Track and hold.
- Digitization with 3 hysteresis comparators.
- Serialization and slow control (std cells).

4x3.85mm^2

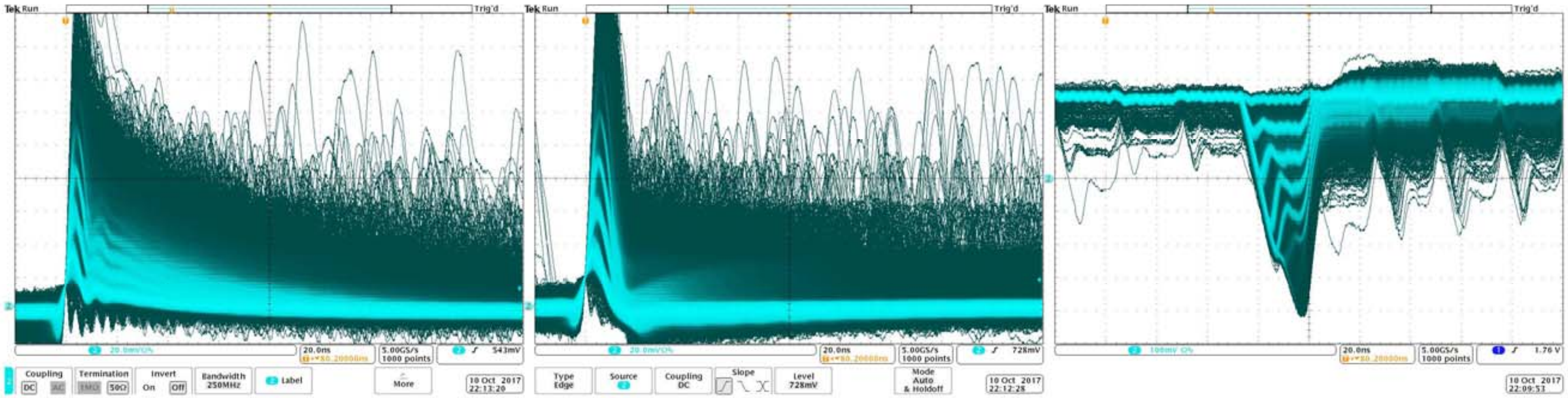
BGA package

$12 \times 12mm^2$ 196pins

V. ASICs summary: PACIFIC

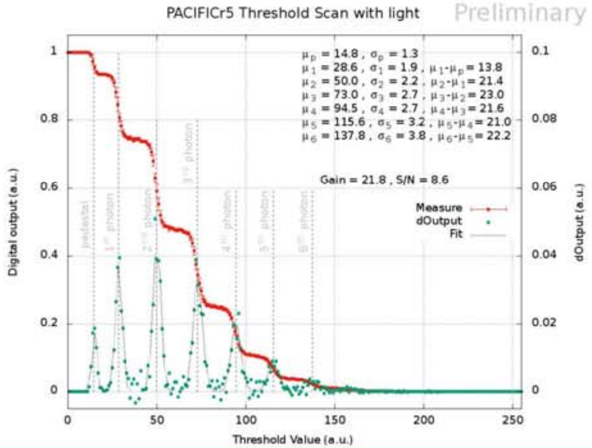
PACIFIC

Collaboration: Heidelberg, ICCUB , LPC-Clermont, IFIC-Valencia



SiPM connected to PACIFIC:

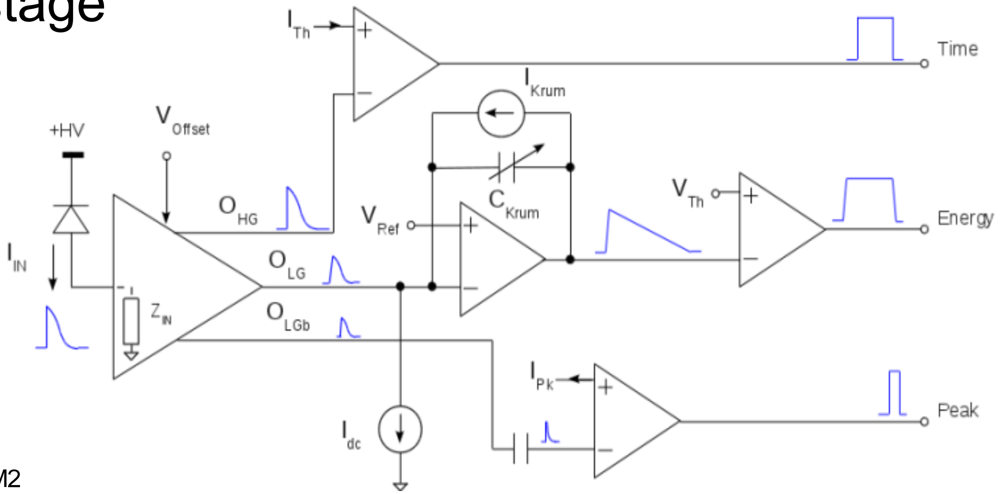
- Analog DEBUG outputs for Preamp, Shaper and TH.
- Synchronous light triggered on front of array.
- Threshold scan of one comparator to measure photons.

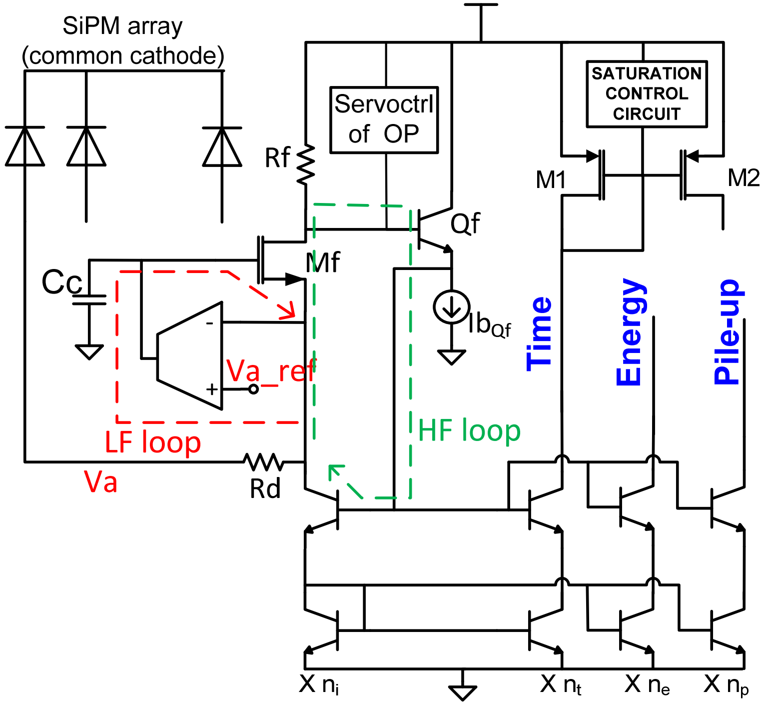


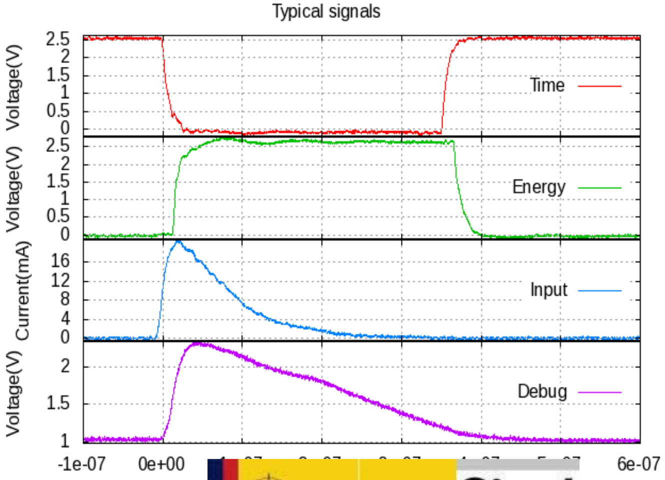
V. ASICs summary: FlexToT: linearized ToT RO chip

Collaboration: ICCUB and CIEMAT

- A Flexible ASIC for SiPM RO (PET, SPECT, Compton)
  - Novel current mode input stage
  - Time resolution for ToF
  - Time over Threshold RO
    - **No ADC**

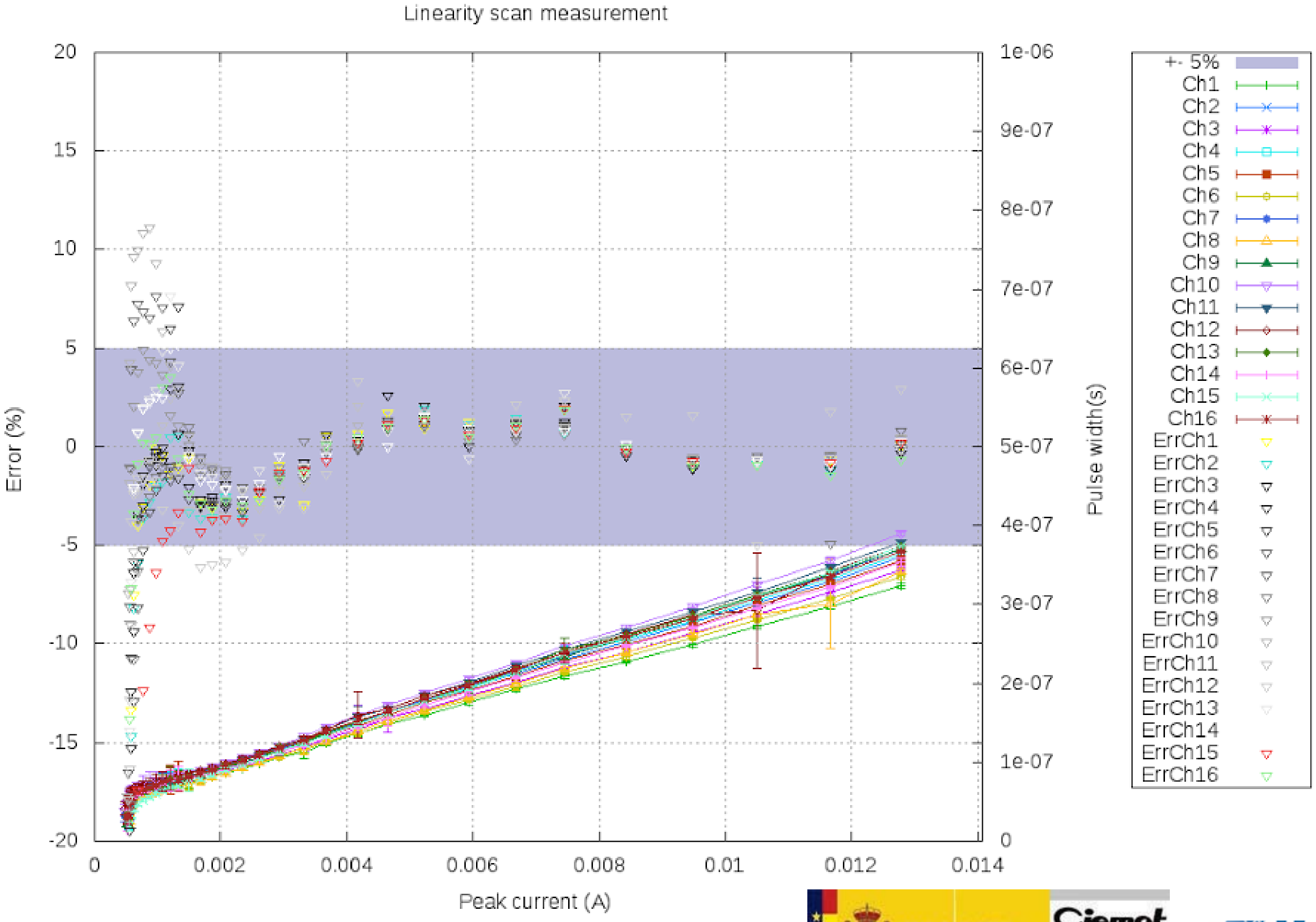






V. ASICs summary: FlexToT: linearized ToT RO chip

- **Good linearity and uniformity**
  - With only comparator threshold offset equalization
- **Different operating ranges can be covered**

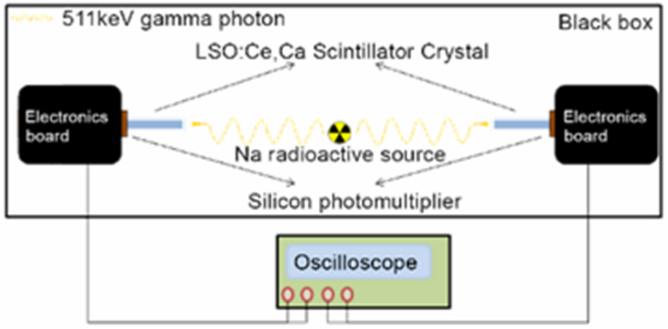


V. ASICs summary: FlexToT: linearized ToT RO chip

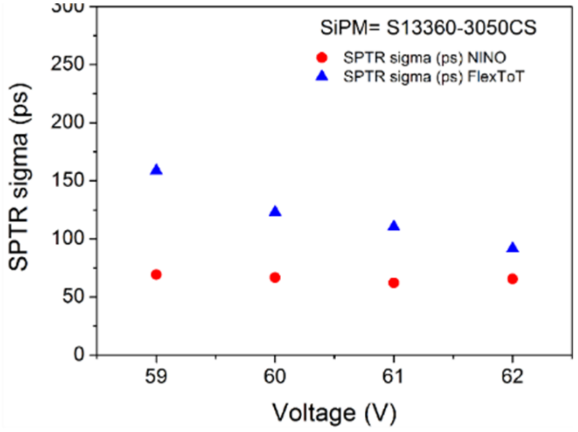
- Measured @ CERN:
  - Single Photon Time resolution (SPTR)
  - Coincidence Time Resolution (CTR)
  - Supported by FAST COST ACTION
    - Many thanks to E. Auffray and S. Gundacker
  - Similar results as for NINO but 3 times lower power consumption

Coincidence Time Resolution (CTR): 128 ps FWHM

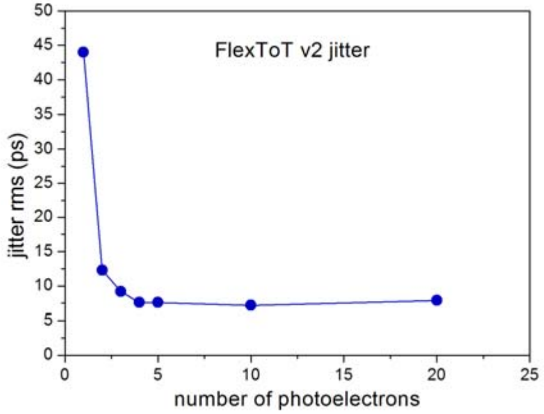
- 2x2x5 mm3 LSO:Ce,Ca crystals.
- Measurements performed in a black-box at 15 ºC.
- Coincidences corresponding to 511 KeV photopeak (±3σ).



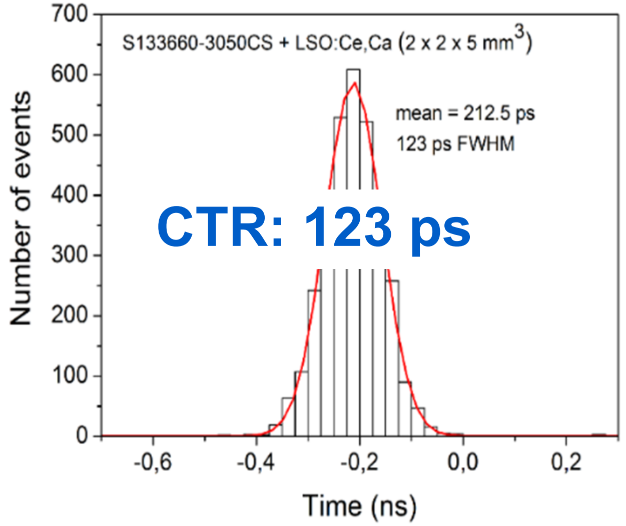
Coincidence Time Resolution (CTR) test bench setup



SPTR=90ps



Jitter floor: 7 ps rms



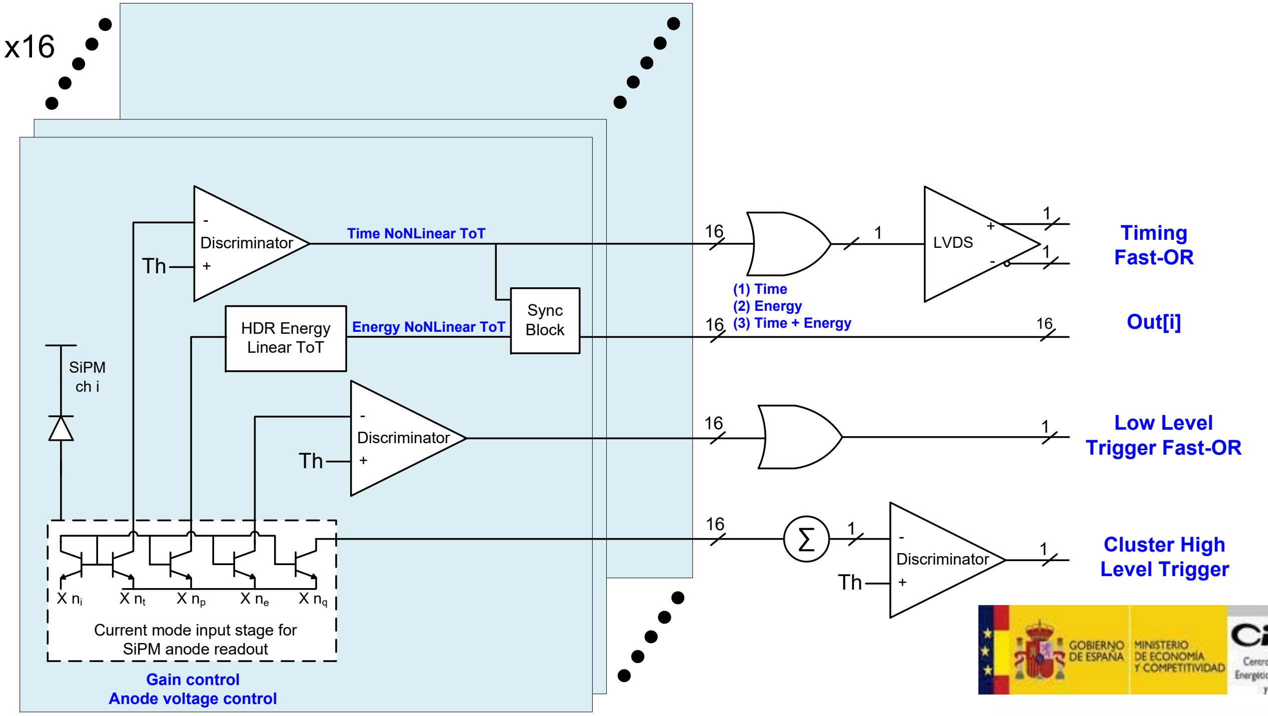
CTR: 123 ps

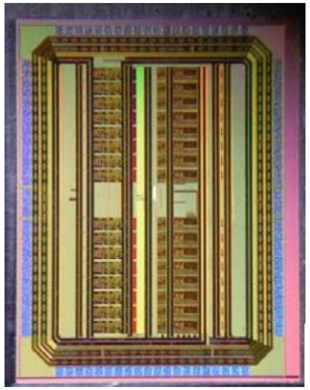
V. ASICs summary: HRFlexToT: linearized ToT RO chip

- A new version of the FlexToT has been recently developed.
  - A linear Time over Threshold with higher resolution (>8bits)
  - Lower power consumption (about 3.5 mW/ch)
  - Different trigger levels and cluster trigger for monolithic crystals.
  - Different scintillator time constants.

HRFlexToT

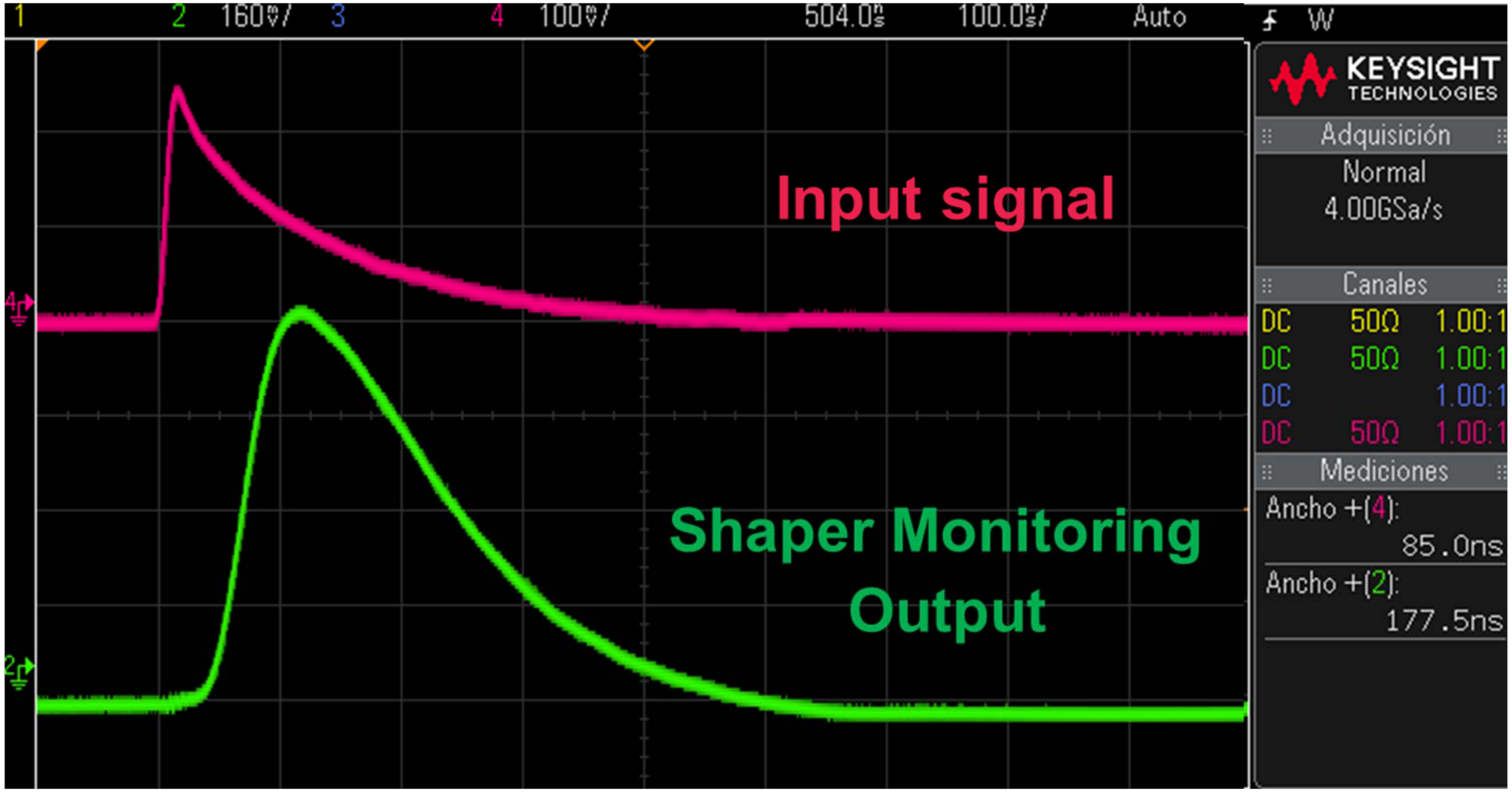
180 nm CMOS





V. ASICs summary: HRFlexToT: linearized ToT RO chip

- Based on shaper and peak detector circuits



1 2 160mV/ 3 4 100mV/ 504.0ns 100.0ns/ Auto

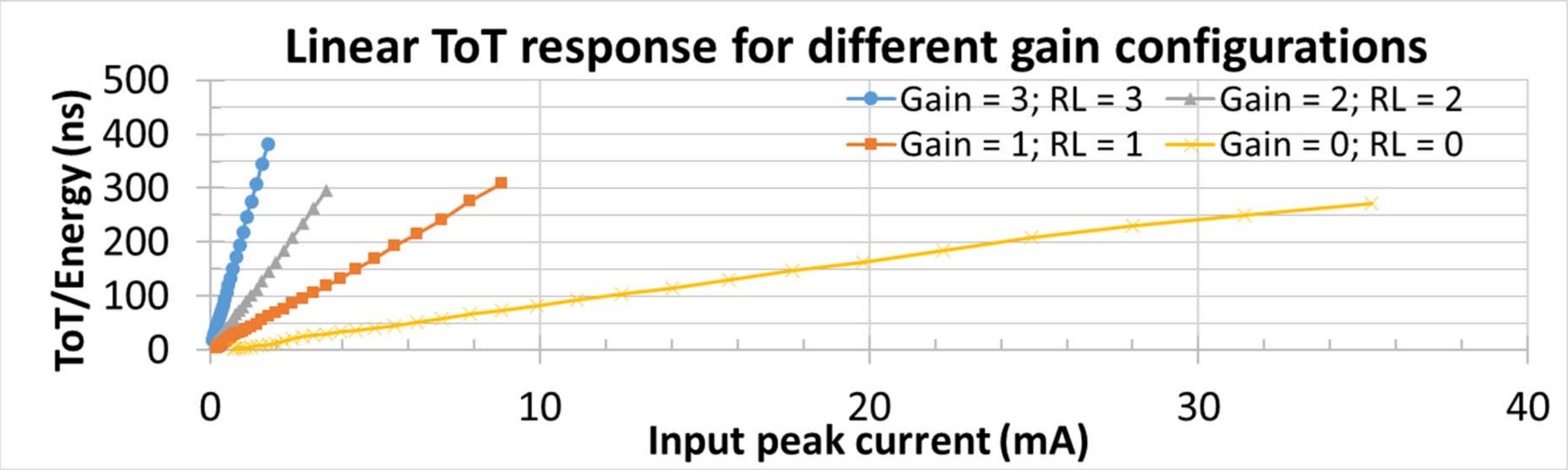
Adquisición
Normal
4.00GSa/s

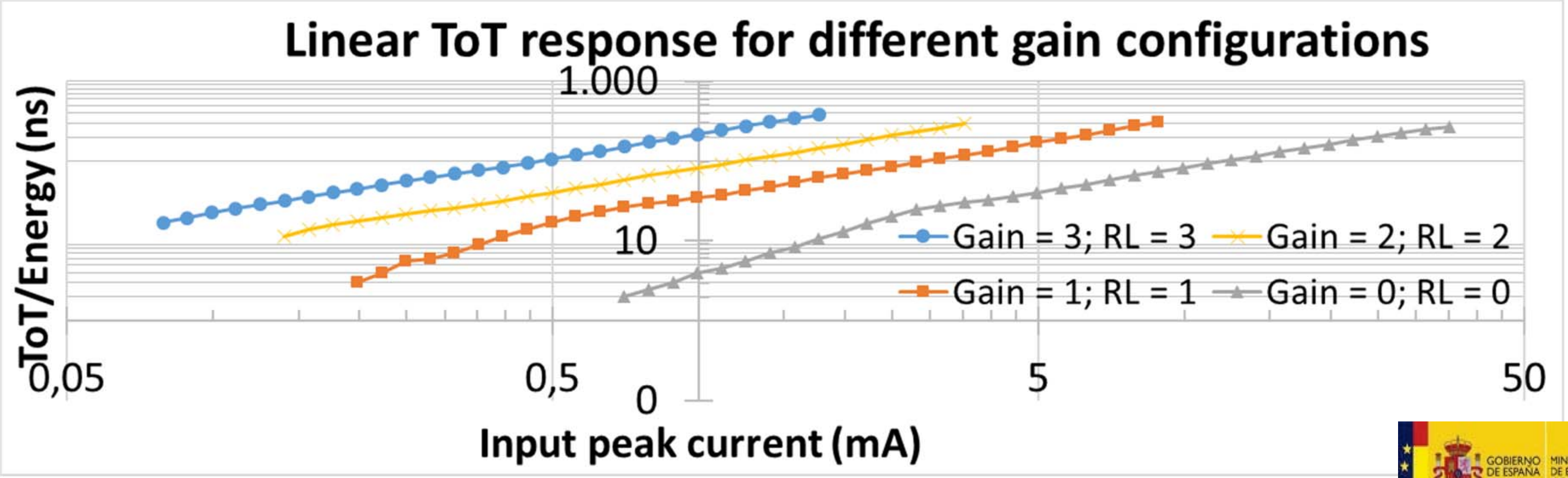
Canales
DC 50Ω 1.00:1
DC 50Ω 1.00:1
DC 1.00:1
DC 50Ω 1.00:1

Mediciones
Ancho +(4): 85.0ns
Ancho +(2): 177.5ns

V. ASICs summary: HRFlexToT: linearized ToT RO chip

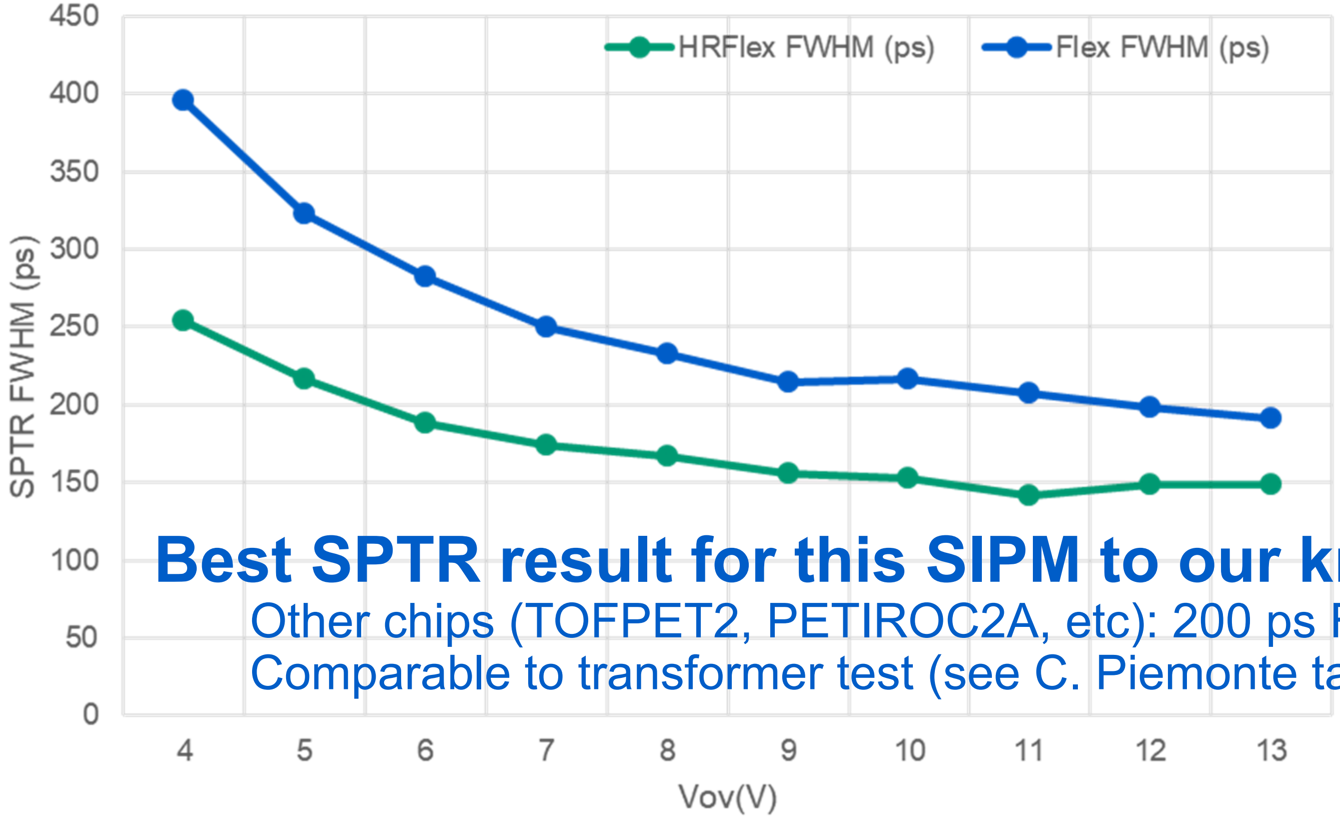
- Linearity and dynamic range





V. ASICs summary: HRFlexToT: linearized ToT RO chip

- Preliminary results
  - **3x3 mm^2** HPKK device (50 um) cell, **S13660**.
  - ***SPTR*** of about 60 ps rms (<***150 ps FWHM***) with 3.5 mW/ch

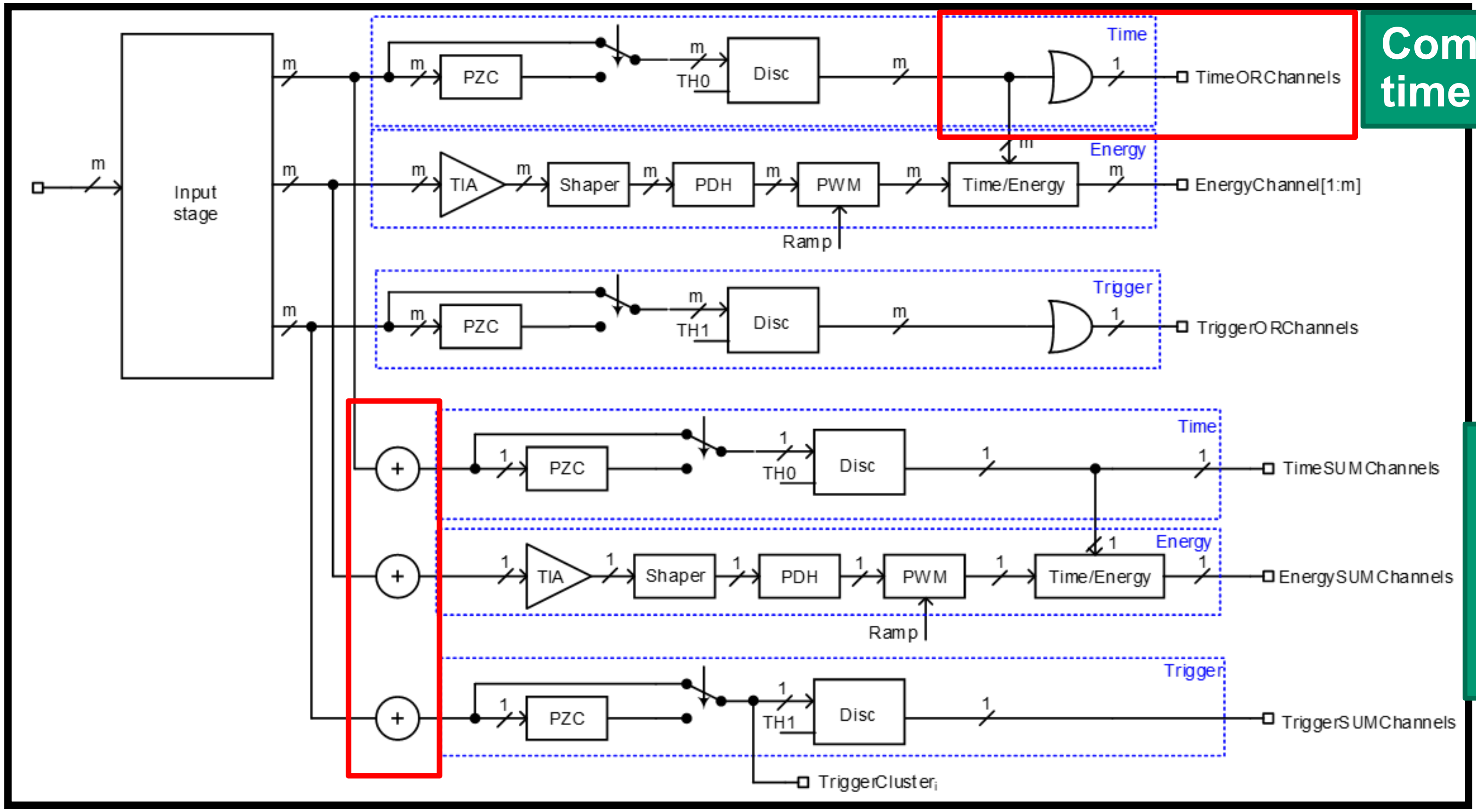


Best SPTR result for this SIPM to our knowledge:

Other chips (TOFPET2, PETIROC2A, etc): 200 ps FWHM for S13360
Comparable to transformer test (see C. Piemonte talk).

IV. ASICs summary: outlook

- New ASIC ***FastIC*** in 65 nm being developed by ICCUB and CERN
  - Very low power input stage, low input impedance, summation, < 10 ps TDC…
- First step towards a Hybrid Single Photon Pixel Detector



Combined time by OR

Combined time, energy and trigger by analog summation

II: Input stage optimization

- In current sensing, R_{in} should be minimized for best timing (improved di/dt), **but any value smaller than $R_{in,min}$ = 5 Ω make the parasitic input network to resonate.**
  - Low R_{in} trade-offs with power consumption; it can be reduced by means of feedback schemes, at the cost of compromising stability.
  - In practice, R_{in} in the range 15 Ω – 20 Ω are desirable in order to be compatible with detectors showing Cdet = 10 pF (PMTs/MCPs) – 1 nF (Large SiPMs).
- In voltage sensing, R_{in} should be maximized for best timing (improved dv/dt). **Signal dynamics are favourable since underdamped response is not possible under such a case.**
  - The parallel resonance can boost the slew-rate even more, but one should rely on parasitics…
  - Large R_{in} results in degraded count-rate capabilities. PZ cancellation becomes compulsory.
- Optimum bandwidth in the signal path, prior to discrimination $BW_{opt} \sim 3\frac{1}{2\pi\sqrt{L\,C_{det}}}$
  - The minimum LC_{det} product (5 nH short connection / 10 pF in PMT) already results in 1 GHz optimum bandwidth.

→ No point in designing current sensing circuits faster than 1 GHz, since only noise would be integrated, worsening σ_t!

I. Introduction: current IACTs cameras

- Even some CTA telescopes will still be based on PMTs

incoming photon

photoelectric effect PE
(generation of the primary electron)

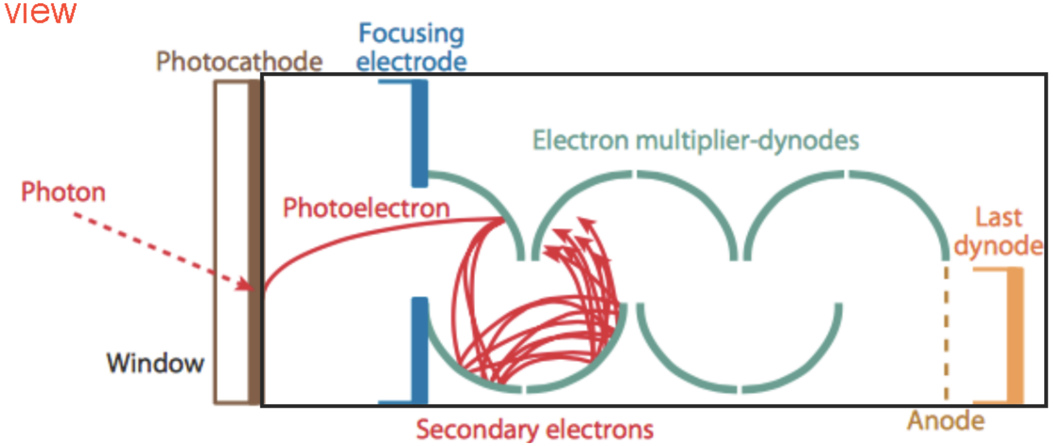
electron multiplication chain

- production of secondary electrons
 => **measurable electric signal**

photomultiplier tube (**PMT**) - THE photodetector!

NO Si-based!

schematic view

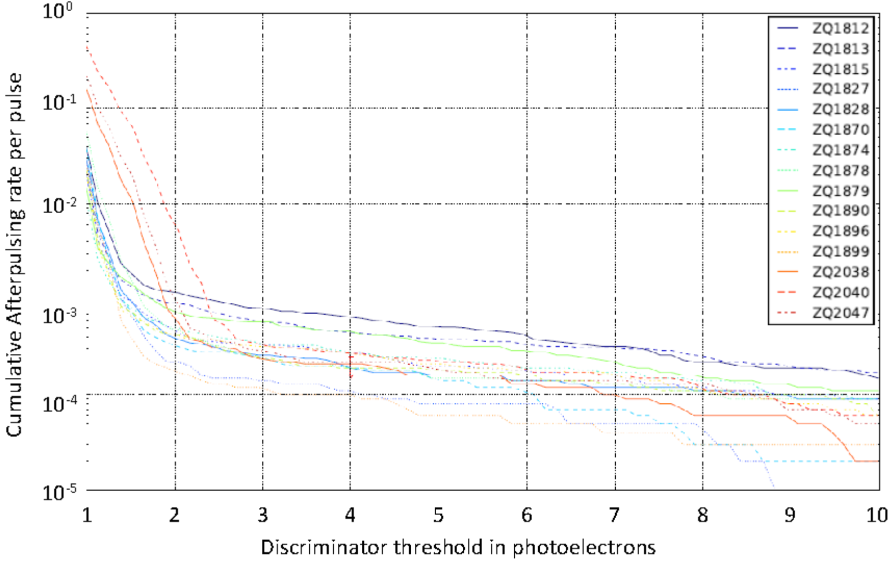


C. Casella, "Application of photosensors", ICCUB- Technoweek, 2016.

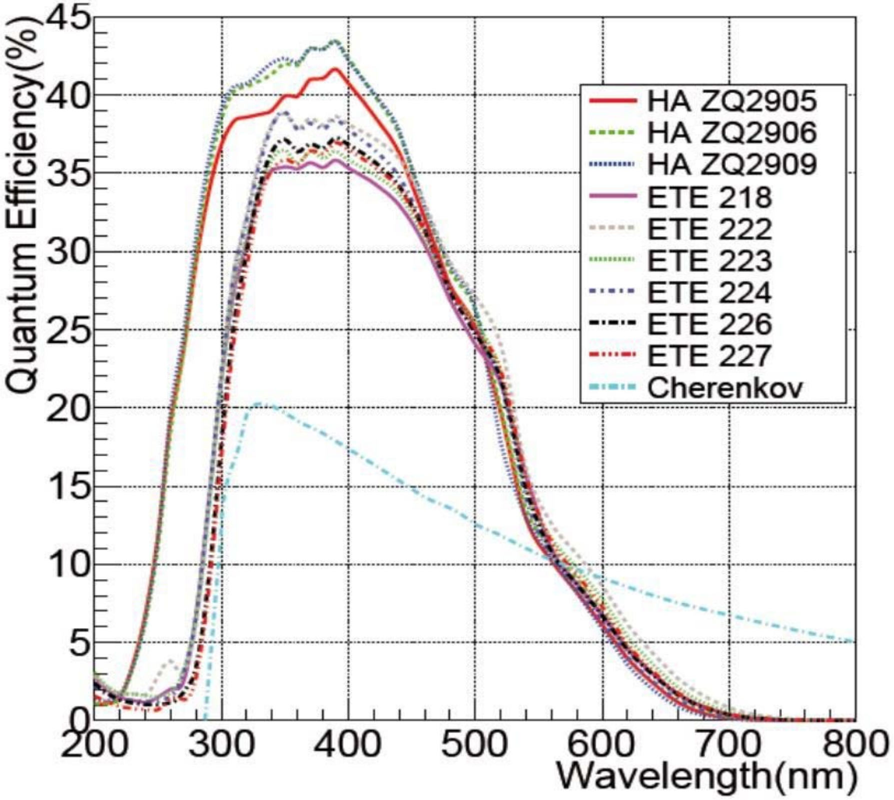
I. Introduction: current IACTs cameras

- Even some CTA telescopes will still be based on PMTs
- Amazing progress in last 10 years
  - PMTs developped for CTA

Afterpulsing at 4 ph.e.
Threshold << 0.02 %



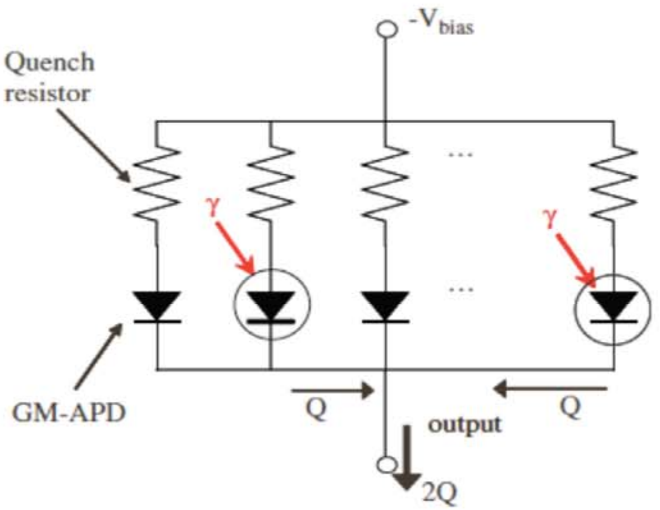
Peak PDE > 35 %

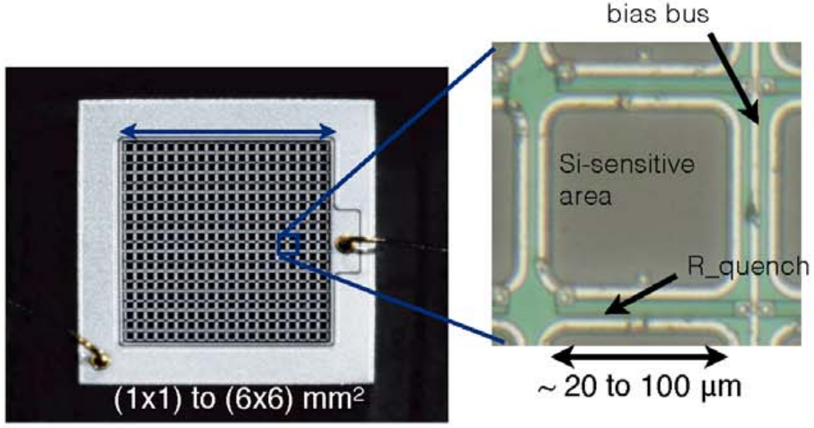


22.04.2015 APPEC TF,
Razmik Mirzoyan:
Recent Progress on PMT and SiPM, where we are going to

I. Introduction: SiPM based IACTs cameras

- SiPM principle





nr cells ~ 100 to 15000 / mm^2

SiPM : array of micro-cells ***APD-like operated in G-mode*** connected to a **common bias** through **independent quenching resistors**, all integrated within a sensor chip.
The output is the **analogue sum of all cells**

individual cell (i.e. one diode, *APD-like*)

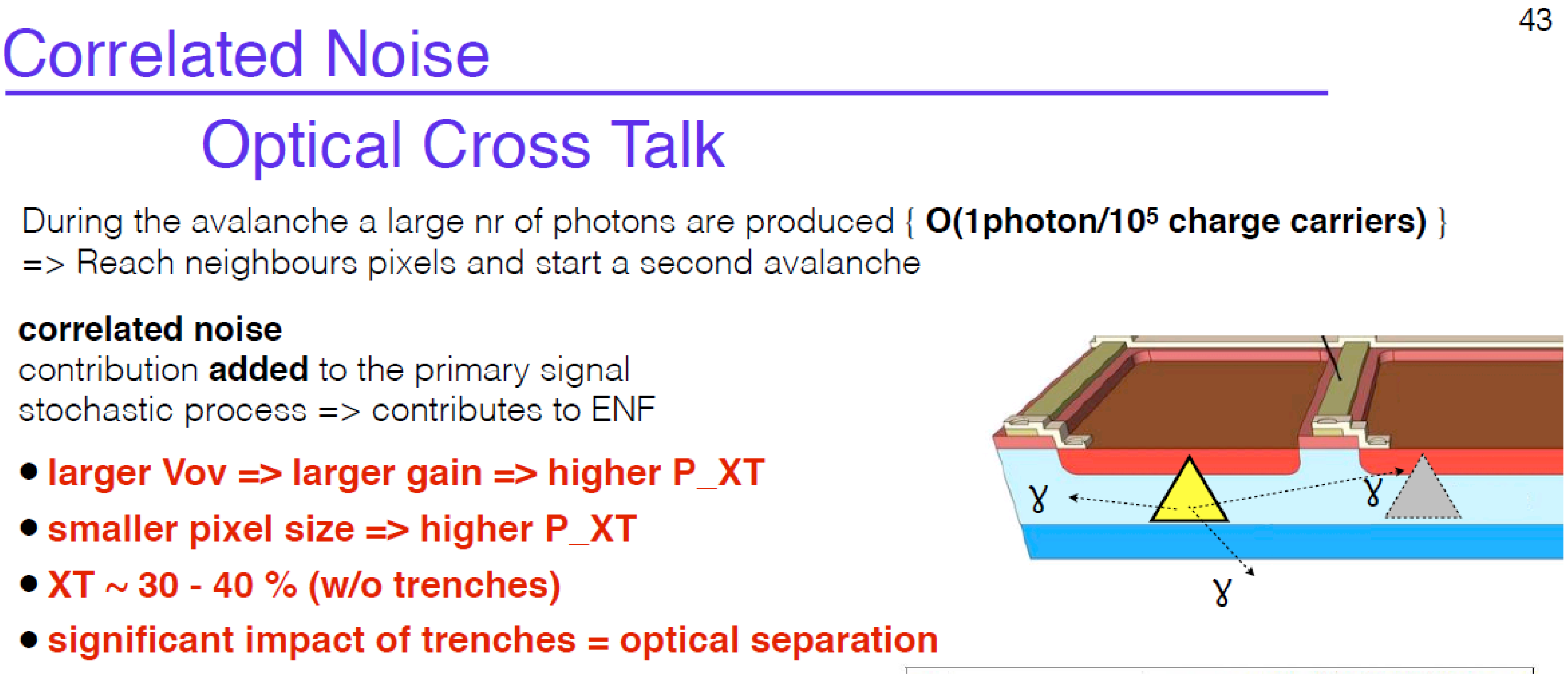
- Vbias > Vbreakdown
- Gain ~ 10^6 - 10^7
- Geiger regime (fully saturated)
- **No analogue info at the single cell level !**

- when hit by 1(2,3...n) photon(s)
  => full discharge
  => Qcell = Ccell $\underbrace{\text{(Vbias - Vbreakdown)}}_{\text{overvoltage}}$

C. Casella, "Application of photosensors", ICCUB- Technoweek, 2016.

I. Introduction: SiPM based IACTs cameras

- What is crosstalk in a SiPM?



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Correlated Noise

Optical Cross Talk

During the avalanche a large nr of photons are produced { **O(1photon/10^5 charge carriers)** }
=> Reach neighbours pixels and start a second avalanche

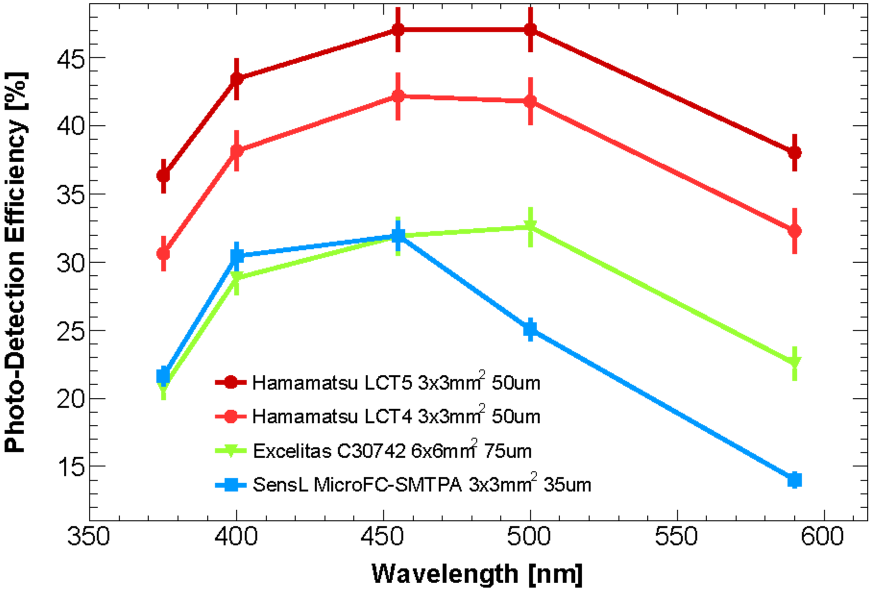
correlated noise
contribution **added** to the primary signal
stochastic process => contributes to ENF

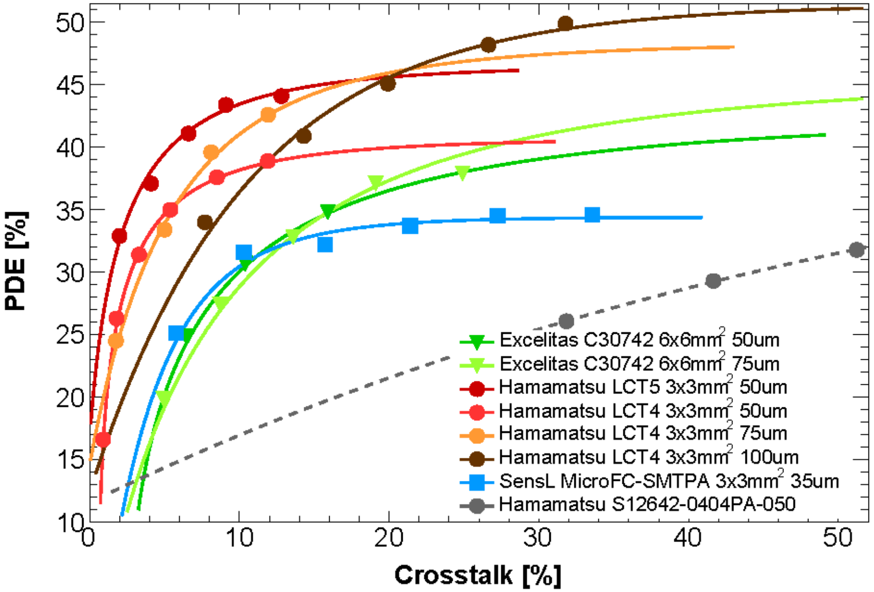
- **larger Vov => larger gain => higher P_XT**
- **smaller pixel size => higher P_XT**
- **XT ~ 30 - 40 % (w/o trenches)**
- **significant impact of trenches = optical separation**

C. Casella, “Application of photosensors”, ICCUB- Technoweek, 2016.

I. Introduction: SiPM requirements for IACTs

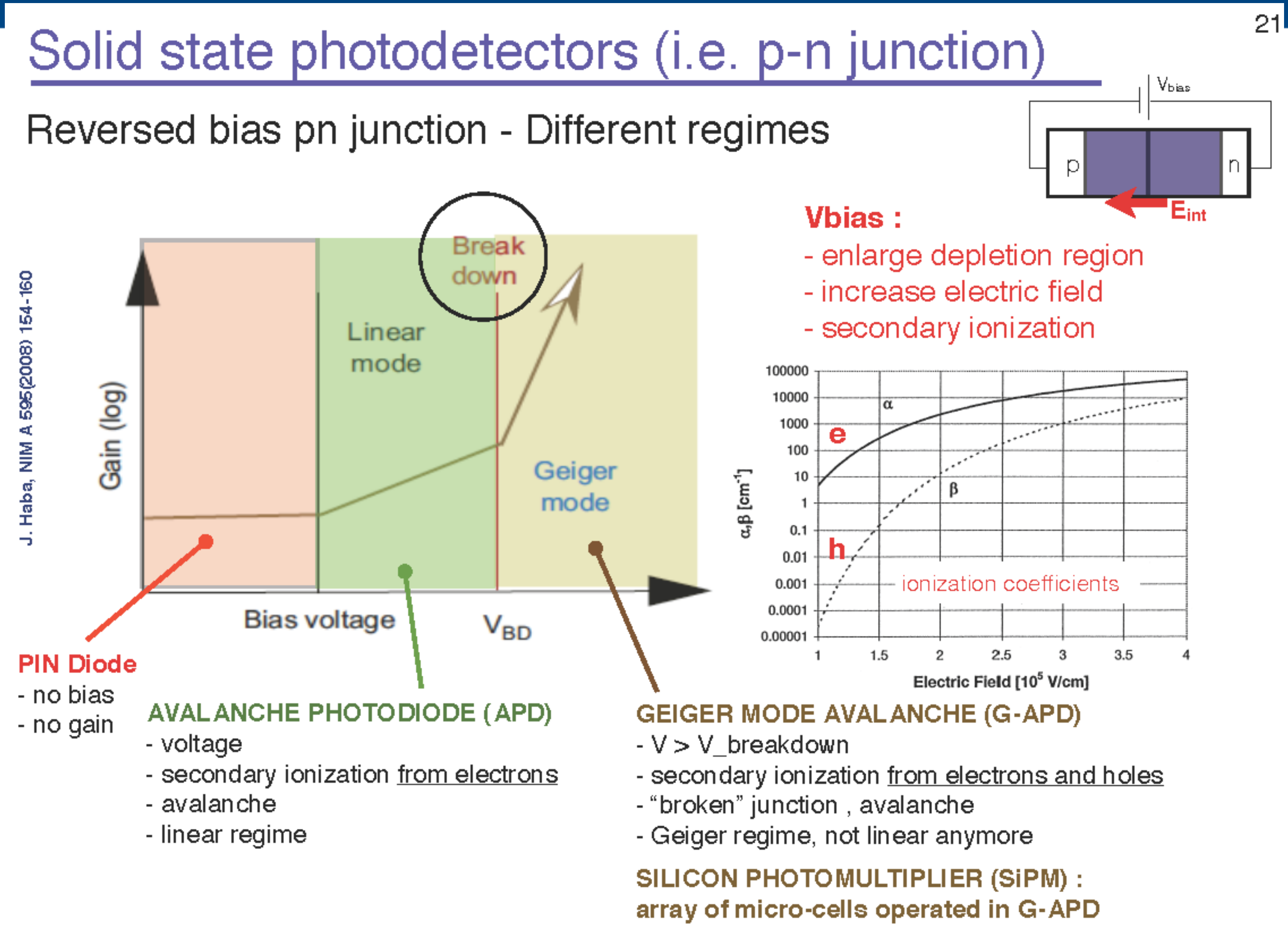
- High PDE > 40 %
  - A higher PDE results in a higher reconstruction rate of Cherenkov photons and decreases the energy threshold
- Low crosstalk
  - Crosstalk degrades the single photon charge resolution
- Trade-off between PDE and crosstalk





J. Biteau et alt. "Performance of Silicon Photomultipliers for the Dual-Mirror Medium-Sized Telescopes of the Cherenkov Telescope Array", ICRC2015

I. Introduction: SiPM based IACTs cameras



Solid state photodetectors (i.e. p-n junction)

Reversed bias pn junction - Different regimes

Vbias :
- enlarge depletion region
- increase electric field
- secondary ionization

PIN Diode
- no bias
- no gain

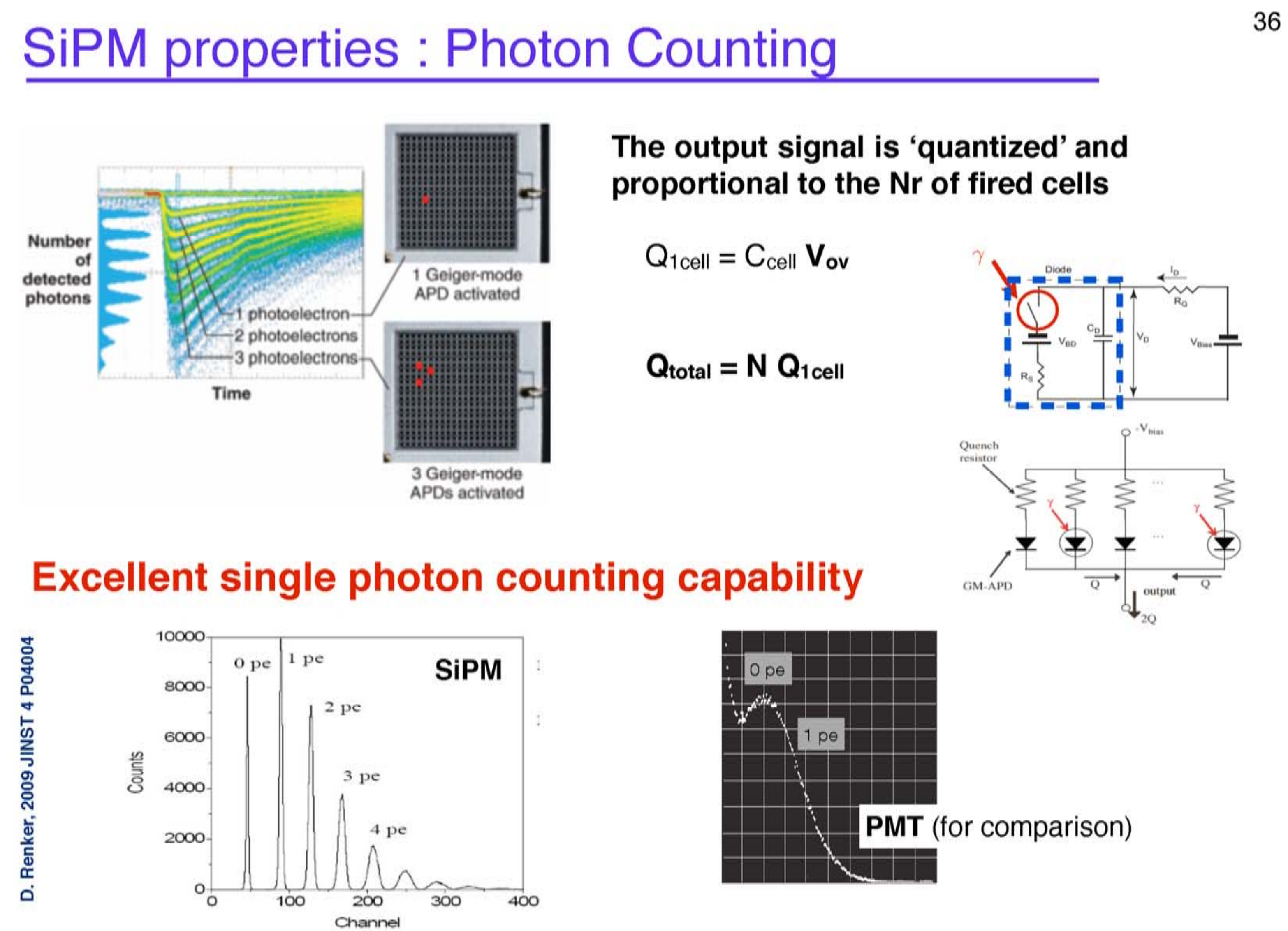
AVALANCHE PHOTODIODE (APD)
- voltage
- secondary ionization from electrons
- avalanche
- linear regime

GEIGER MODE AVALANCHE (G-APD)
- V > V_breakdown
- secondary ionization from electrons and holes
- “broken” junction , avalanche
- Geiger regime, not linear anymore

SILICON PHOTOMULTIPLIER (SiPM) :
array of micro-cells operated in G-APD

C. Casella, “Application of photosensors”, ICCUB- Technoweek, 2016.

I. Introduction: SiPM based IACTs cameras



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SiPM properties : Photon Counting

The output signal is 'quantized' and proportional to the Nr of fired cells

$$Q_{1cell} = C_{cell}\,\mathbf{V_{ov}}$$

$$\mathbf{Q_{total} = N\,Q_{1cell}}$$

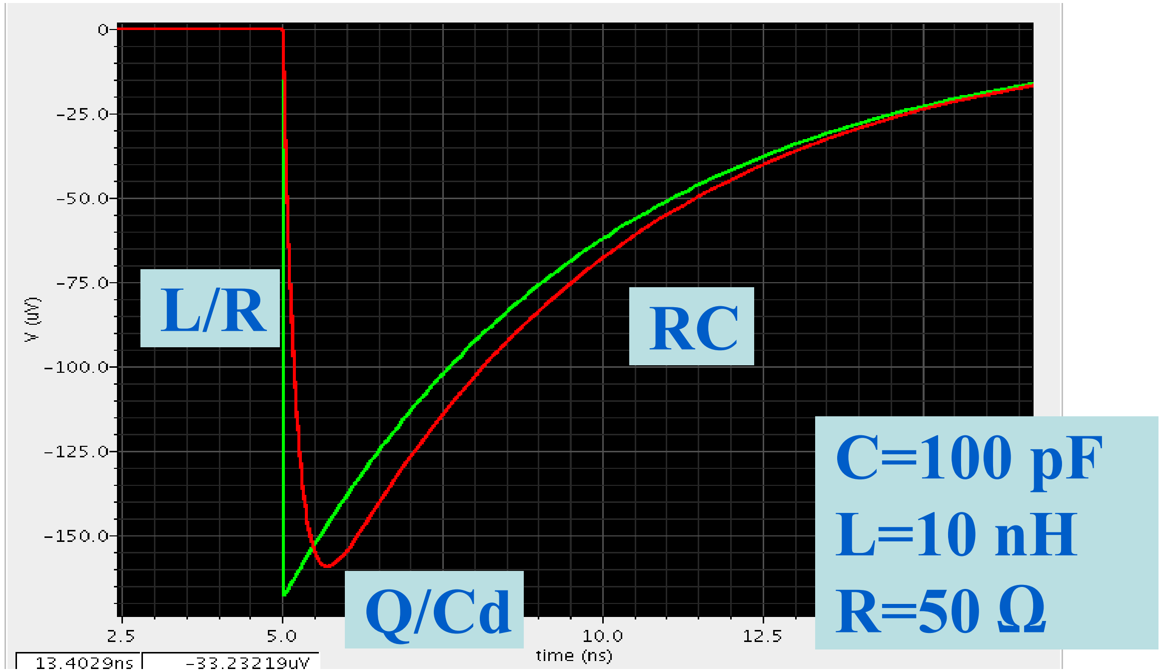
Excellent single photon counting capability

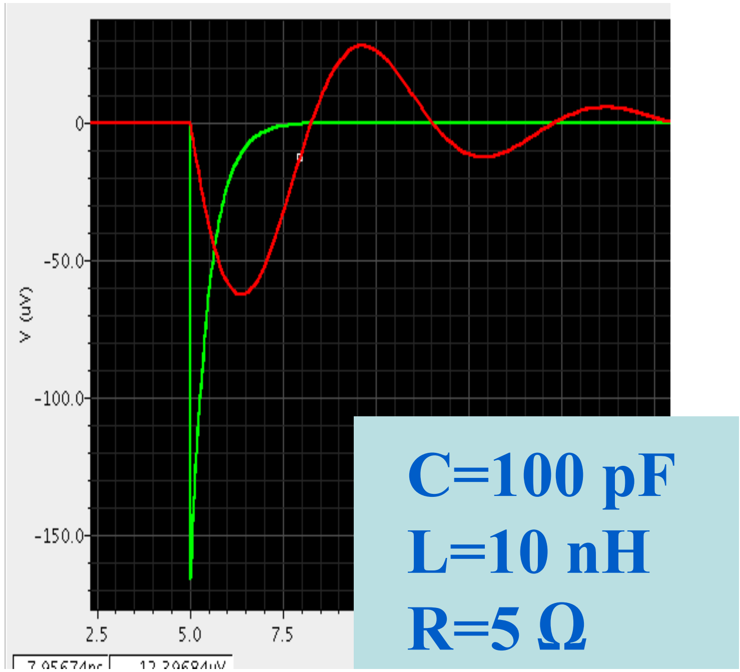
PMT (for comparison)

C. Casella, "Application of photosensors", ICCUB- Technoweek, 2016.

Basic pulse shapes

- **Short pulse : Q=16 fC, Cd=100 pF, L=0-10 nH, RL=5-50 Ω**
- **Smaller signals with SiPM (large Cd) ~ mV/p.e.**
- **Sensitivity to parasitic inductance**
- **Choice of RL : decay time, stability**
- **Convolve with current shape… (here delta impulse)**

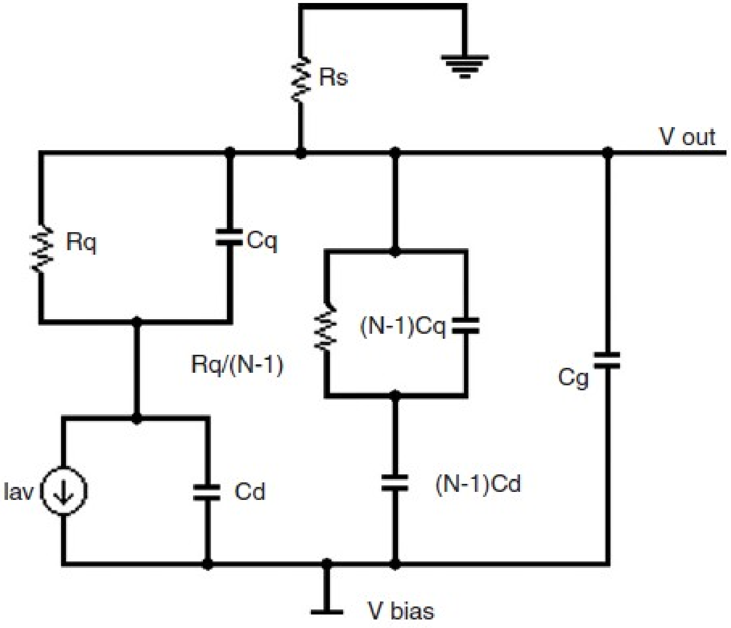




C. De La Taille, Photodet conference, 2012

SiPM modelization

- **Modelization by Corsi et al [NIM A572 2007]**



[F. Corsi et al. NIM A572]

	SiPM IRST, $N = 625$, $V_{\text{bias}} = 35\ \text{V}$
R_q (kΩ)	393.75
V_{br} (V)	31.2
Q (fC)	148.5
C_d (fF)	34.13
C_s (fF)	4.95
C_g (pF)	27.34

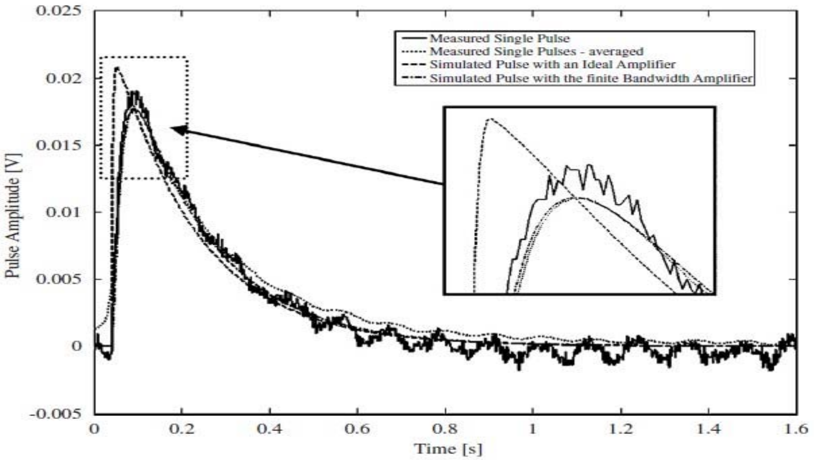


Fig. 2. Fitting of real data with the simulation results on the device model.

Electrical model of a SiPM

Collazuol 2008

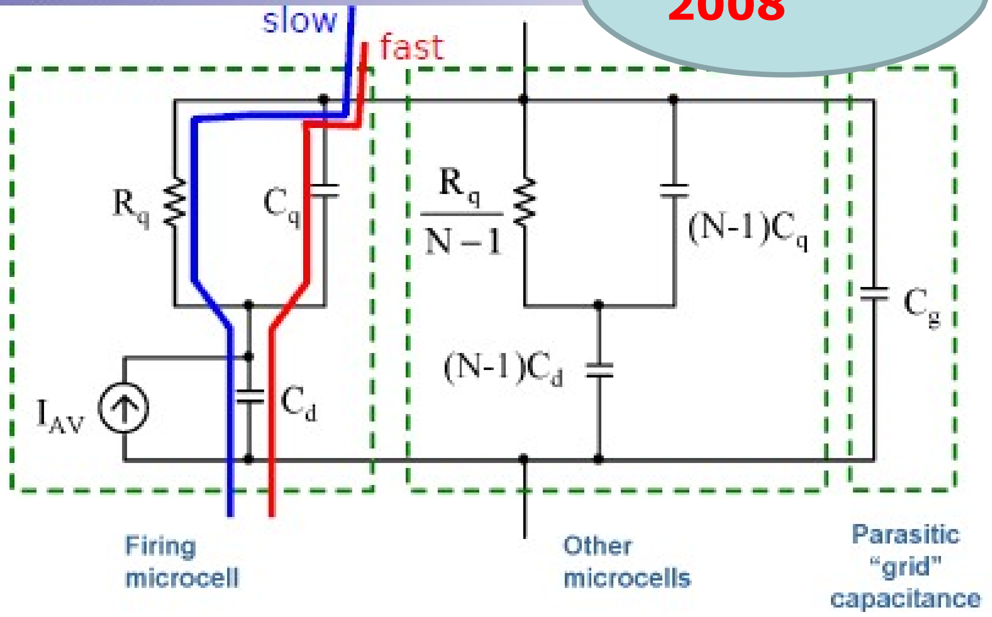
R_q: quenching resistor
(hundreds of kΩ)

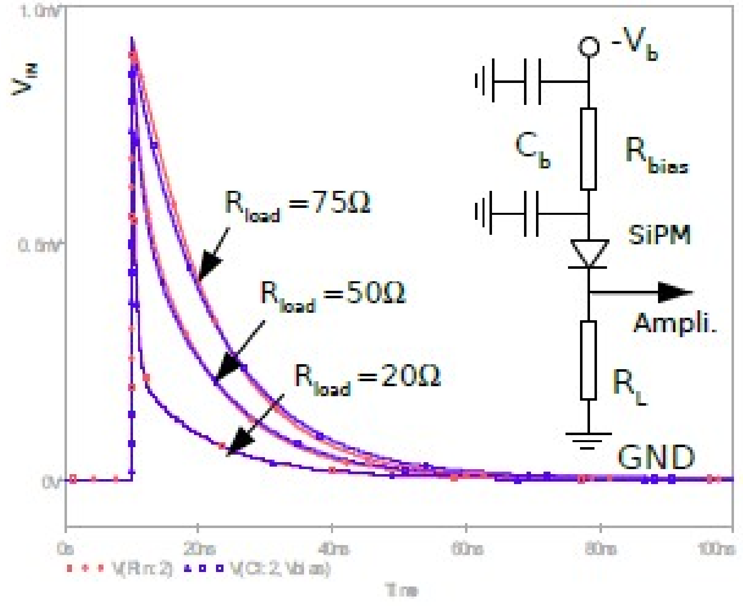
C_d: junction capacitance
(few tens of fF)

C_q: parasitic capacitance in parallel to R_q (few tens of fF, $C_q < C_d$)

I_{AV}: SiPM ~ ideal current source
current source modeling the total charge delivered by a cell during the avalanche $Q=\Delta V(C_d+C_q)$

C_g: parasitic capacitance due to the routing of Vbias to the cells (metal grid, few tens of pF)





1) the peak of V_{IN} is independent of R_s

A constant fraction Q_{IN} of the charge Q delivered during the avalanche is instantly collected on $C_{tot}=C_g+C_{eq}$.

2) The circuit has two time constants:

- $\tau_{IN} = R_L\ C_{tot}$ (fast)
- $\tau_r = R_q\,(C_d+C_q)$ (slow)

Decreasing R_s, the time constant τ_{IN} decreases,
the current on R_s increases and
the collection of Q is faster

F. Corsi, C. Mazzocca et al.

SiPM equivalent circuit

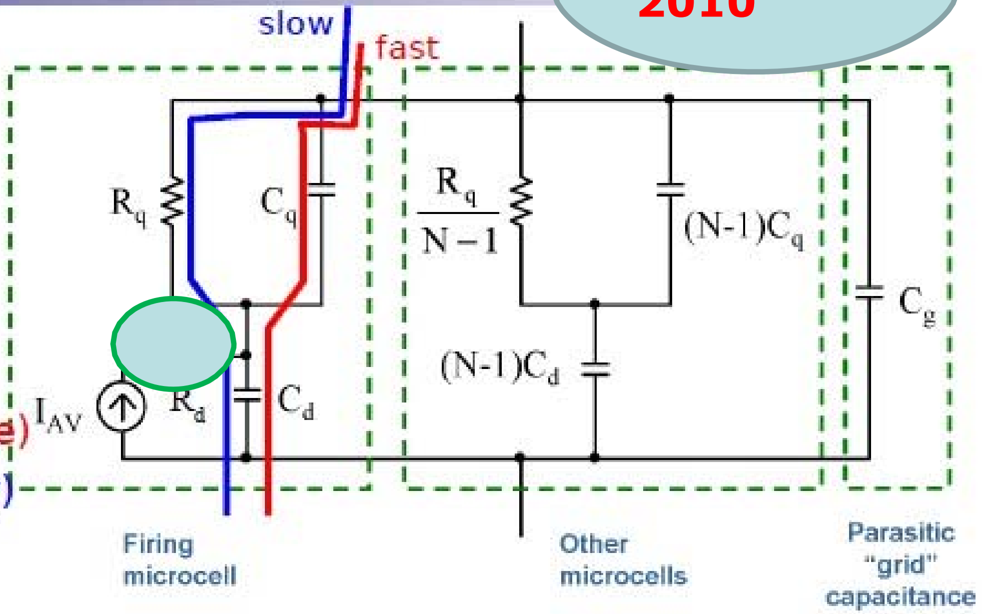
Collazuol 2010

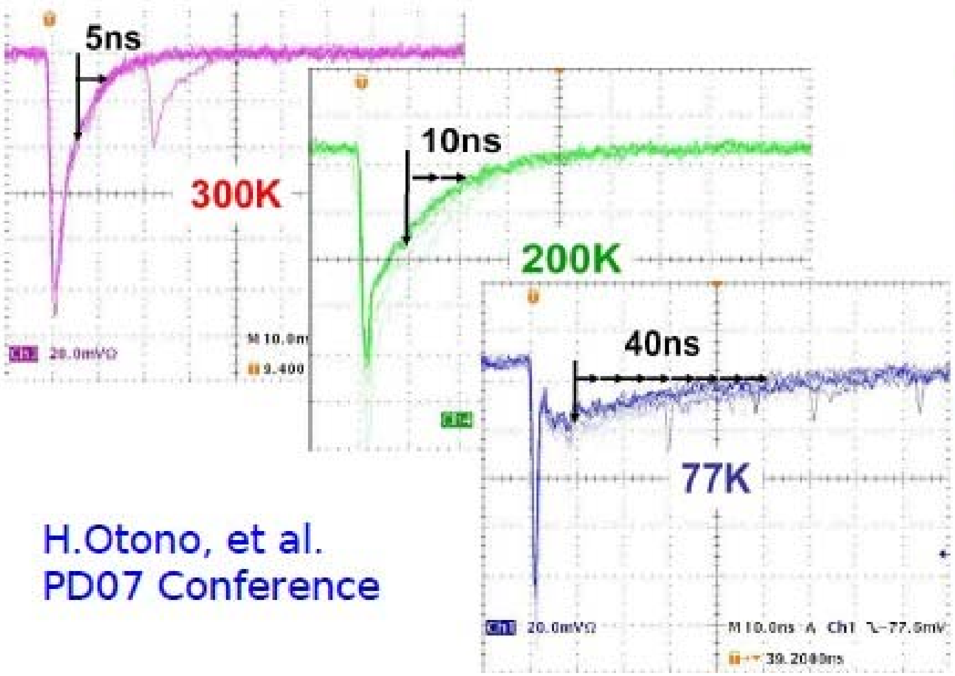
Single cell model → $(R_d||C_d)+(R_q||C_q)$
SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

Signal = slow pulse $(\tau_{d\ (rise)}, \tau_{q\text{-}slow\ (fall)})$ +
+ fast pulse $(\tau_{d\ (rise)}, \tau_{q\text{-}fast\ (fall)})$

- $\tau_{d\ (rise)} \sim R_d(C_q+C_d)$
- $\tau_{q\text{-}fast\ (fall)} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{q\text{-}slow\ (fall)} = R_q\ (C_q+C_d)$ (slow; cell recovery)

F. Corsi, et al. NIMA 572(2007)





H.Otono, et al.
PD07 Conference

Pulse shape:

The two current components show different behavior with Temperature

→ fast component is independent of T because stray C_q couple with external R_{load} (no dependence on T) while R_q is strongly dependent on T

(we used low light level, BW filters against noise and AC coupling → difficult to disentangle the two components)