Upgrading the Inner Tracking System and the Time Projection Chamber of ALICE

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on behalf of the ALICE collaboration
Motivation

Physics Goals for Run 3 + Run 4:

- **Heavy-flavour** mesons and baryons (down to very low $p_T$) → mechanism of quark-medium interaction
- **Charmonium states** → dissociation/regeneration as tool to study de-confinement and medium temperature
- **Di-leptons** from QGP radiation and low-mass vector mesons → $\chi$ symmetry restoration, initial temperature and EOS
- High-precision measurement of **light and hyper-nuclei** → production mechanism and degree of collectivity

→ High-precision measurements of **rare probes at low $p_T$**
→ Cannot be selected by hardware triggers as they are characterised by very low S/B

Strategy

- Need to record **large minimum-bias data sample**
  → Read out all Pb-Pb interactions up to the maximum LHC Pb-Pb collision rate of 50 kHz
  → Collect $L_{Pb-Pb} = 13 \text{ nb}^{-1}$ (increase the minimum-bias data sample by factor 50-100 with respect to Run 2)
- Improve **tracking efficiency** and **resolution** at low-$p_T$
  - Increase tracking granularity
  - Reduce material thickness
  - Minimise the distance to IP
- Preserve **Particle IDentification (PID)**
  - Consolidate and speed-up main ALICE PID detectors
ALICE Upgrades

New Inner Tracking System (ITS)
New Muon Forward Tracker (MFT)
New TPC Readout Chambers (ROCs)

New Fast Interaction Trigger (FIT) Detector
Readout upgrade
Integrated Online-Offline system (O²)
FoCal proposal (Run 4)

Upgrade posters:
Dimuon polarization measurement for detecting ultra-intense magnetic field in Pb-Pb collisions at the ALICE experiment, T. Osako
Muon Forward Tracker: adding vertexing capability to the ALICE MUON Spectrometer, Y. Yamaguchi
Quantitative evaluation of muon track matching efficiency with Muon Forward Tracker and Muon Spectrometer at ALICE, K. Kamano
Towards improved measurements with the upgrade of the ALICE Inner Tracking System in LS3, D. Andreou
Performance evaluation of a Forward Calorimeter for ALICE upgrade, Y. Minato
The ALICE TPC: Upgrade and Physics Perspective, B. Nielsen
Time Projection Chamber
Time Projection Chamber (TPC)

- Diameter: 5 m, length: 5 m
- Gas: Ne-CO₂-N₂, Ar-CO₂
- Max. drift time: ~100 μs
- 18 sectors on each side
- Inner and outer readout chambers: IROC, OROC

Previous detector (Run 1, Run 2):
- 72 MWPCs
- ~550 000 readout pads
- Wire gating grid (GG) to minimize Ion Back-Flow (IBF)
- Rate limitation: few kHz

Operate the new TPC at 50 kHz → no gating grid
Continous Readout with GEMs

TPC Upgrade requirements:
- Nominal gain = 2000 in Ne-CO$_2$-N$_2$ (90-10-5)
- Ion Back-Flow (IBF) < 1% ($\varepsilon = 20$)
- Energy resolution: $\sigma_E/E < 12\%$ for X-rays from $^{55}$Fe
- Stable operation under LHC Run 3 conditions → Unprecedented challenges in terms of loads and performance

Adopted solution: 4-GEM stack
- Combination of standard (S) and large pitch (LP) GEM foils
- Highly optimised HV configuration
- Result of intensive R&D
TPC Readout Electronics

Newly developed FE SAMPA ASIC (130 nm TSMC CMOS)

- 32 channels (positive or negative input)
- PASA pre-amplifier + 10-bit ADC
- Programmable conversion gain and peaking times
- DSP, memory, high-speed e-links
- Readout mode: continuous or triggered
- Excellent noise figure of $670\,\text{e}^{-} (@18\,\text{pF on detector})$
- Production and testing completed

Front-End Cards (FECs)

- 5 SAMPA chips per FEC (3276 FECs in total)
- System continuously digitises signals at 5 MHz
- All ADC values read out at 3.3 TB/s
- FECs send digitised data over fiber optic links to ALICE Common Readout Units (CRU)
- Production and testing (97.4% yield) completed, installation ongoing
TPC upgrade sequence

Remove Services and FEE (outside cleanroom)  
Uninstall MWPC ROC  
Install GEM ROC  
Install new FECs + test  
Ready for transportation to SX2

11 Apr  
7 Mar  
14 Apr (A)  
5 Aug (C)  
13 May (A)  
16 Aug (C)  
14 Jun (A)  
25 Aug (C)  
5 Jul (A)  
16 Sep (C)  
14 Oct (A)  
31 Oct (C)  
25 Nov (A)  
7 Jan (C)  
2 Mar 2020

A Large Ion Collider Experiment

TPC in cleanroom. Cleaning & irradiation tests  
FC HV infrastructure modification  
Survey, shimming, sealing  
Pre-commissioning with cosmics, laser, pulser, X-ray

Done  
Done  
Done  
Ongoing

Done  
Done  
Done  
Done

Done  
Done  
Done  
Ongoing

Upgrading the ITS and TPC of ALICE | QM2019 | November 5th, 2019 | Felix Reidt
Noise Performance of the Sector Test System

IROC:

- Mean: 0.97

OROC:

- Mean: 1.05

Design noise value of 1 ADC demonstrated!
Inner Tracking System (ITS2)
Inner Tracking System (ITS) Upgrade

10 m² active silicon area, 12.5×10⁹ pixels
- Based on the ALPIDE Monolithic Active Pixel Sensor
  - In-pixel amplification, shaping, discrimination and Multiple-Event Buffers (MEB)
  - In-matrix data sparsification
  - High detection efficiency: > 99% and low fake-hit rate: << 10⁻⁶/pixel/event
  - Radiation tolerant: > 270 krad Total Ionising Dose (TID),
    > 1.7×10¹² 1 MeV/n MeV/n Neq Non-Ionising Energy Loss (NIEL)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Previous ITS</th>
<th>New ITS2</th>
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<tbody>
<tr>
<td>Distance to IP (mm)</td>
<td>39</td>
<td>22</td>
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<tr>
<td>X₀ (innermost layer) (%)</td>
<td>~ 1.14</td>
<td>~ 0.35</td>
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<tr>
<td>Pixel pitch (μm²)</td>
<td>50 x 425</td>
<td>27 x 29</td>
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<tr>
<td>Readout rate (kHz)</td>
<td>1</td>
<td>100</td>
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<tr>
<td>Spatial resolution (rφ x z) (μm²)</td>
<td>11 x 100</td>
<td>5 x 5</td>
</tr>
</tbody>
</table>

Layout
- 7 layers (inner/middle/outer): 3/2/2
- 192 staves (IL/ML/OL): 48/54/90

Improve resolution, less material, faster readout
A Large Ion Collider Experiment

Construction Installation and Commissioning Timeline

Detector Construction and Assembly
- ~72000 chips $\rightarrow$ ~2600 Hybrid Integrated Circuits (HICs) $\rightarrow$ ~280 Staves (electrical chip yield*: ~65%, HIC yield*: ~85%, stave yield*: ~95%)
- > 10 production sites in Asia, EU and the US
- ~30 involved institutes
- All detector elements and electronics ready for integration at CERN
- Production of additional spare parts will be completed by end of Nov ‘19
- Integration of Outer Barrel layers 75% done, will finish mid-Nov ‘19

On-surface commissioning with final services ongoing

Installation in the ALICE cavern

6-month global commissioning in ALICE

*excluding pre-series and setup material

Cosmic muon tracks in the Inner Half-Barrel

On-surface commissioning clean room
Example results from the Commissioning

Run 001098 (15 x 10^6 events @ 50 kHz, VBB = -3 V, THR = 100 e tuned)

54 chips,
~ 28M pixels

- Very quiet detector
- Fake-hit rate stable over time

Threshold tuning effective
- Very good uniformity
- Less than 1000 dead pixels

216 chips,
~ 113M pixels
Detected Performance in Run 3 and Run 4

**ITS2**
- Improved tracking efficiency
- Improved tracking resolution
- Pointing resolution 3x better in transverse plane (6x along beam axis)

**New TPC Readout Chambers (GEM)**
- Preserve momentum resolution for TPC + ITS tracks
- Preserve particle identification via $dE/dx$ (M. Aggarwal et al. NIM A903 (2018), 215-223)
Inner Tracking System (ITS3) after LS3
Can we get closer to the IP? Can we reduce the material?
Material budget

- Observations:
  - Silicon makes up only about 15% of total material
  - Irregularities due to support/cooling and overlap
- Removal of water cooling
  - possible if power consumption stays below 20 mW/cm²
- Removal circuit board (power+data)
  - possible if integrated on chip
- Removal of mechanical support
  - benefit from increased stiffness by rolling Si wafers
Implementation

- **Air cooling**
  - possible below 20 mW/cm²
  - studied in the context of ITS2
  - achievable if periphery outside the fiducial volume

- **Wafer-scale chip**
  - Stitching to overcome reticle size limit
  - Chip spanning half or full stave length
  - Neither support structure nor electrical substrate necessary

- **Thinning and bending**
  - Currently 50 µm (25 µm active volume)
  - Below 50 µm, Si wafers become flexible, “paper-like”
  - Smaller pixels would allow shallower active volume
Layout and Mechanics

- Smaller beam pipe diameter and wall thickness (0.14% $X_0$)
- Sensor thickness 20 - 40 µm (0.02 - 0.04% $X_0$)
- Total material up to $r \sim 4$ cm reduced by a factor of 3
- Material homogeneously distributed → essentially zero systematic error from material distribution
- Sensors held in place by low-density carbon foam
- Cooling at the extremities (chip peripheries)
- Plug-in replacement of the current Inner Barrel
Performance gain of ITS3 over ITS2

- Pointing resolution 2x better
- Improved tracking efficiency for low momenta
- Improved physics performance for heavy-flavour baryons and low-mass dielectrons


POSTER: Towards improved measurements with the upgrade of the ALICE Inner Tracking System in LS3, D. Andreou
Summary

- TPC ReadOut Chambers (ROCs) and electronics validated to perform as expected
- The new ITS2 will significantly improve the low-$p_T$ tracking and the pointing resolution
- ITS2 and TPC are set to run at 50 kHz in Run 3
- Both upgrades on track for Run 3 operation in 2021
- ITS3 R&D has started and promises to further improve heavy-flavour baryon and low-mass dielectron measurements

Thank you for your attention!
ITS Layout

• 7 layers (inner/middle/outer): 3/2/2 from R = 22 mm to R = 400 mm
• 192 staves (IL/ML/OL): 48/54/90
• Ultra-lightweight support structure and cooling
ALPIDE - The Monolithic Active Pixel Sensor for the ITS Upgrade

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25 µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel (~30 µm) => low capacitance (~fF)
- Reverse bias voltage (-6 V < V_{BB} < 0 V) to substrate to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors ➔ full CMOS circuitry within active area
- In-pixel amplification and shaping, discrimination and Multiple-Event Buffers (MEB)
- In-matrix data sparsification
- On-chip high-speed link (1.2 Gbps)
- Low total power consumption < 40 mW/cm²
ITS Upgrade – Outer Barrel

- Middle Layer staves: 84 cm long, 114 chips in 8 modules, 59M pixels
- Outer Layer staves: 150 cm long, 196 chips in 14 modules, 103M pixels
- Excellent noise and threshold uniformity maintained across the full stave (after chip-to-chip tuning)

Threshold:
- $\mu = 99.4 \, e^-$
- $\text{RMS}(\mu) = 20.6 \, e^-$

Noise:
- $\sigma = 5.53 \, e^-$
- $\text{RMS}(\sigma) = 0.96 \, e^-$
Wafer-scale chip

• Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  – typical sizes of few cm$^2$
  – modules are tiled by chips connected to a flexible printed circuit board
• New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  – actively used in industry
  – a 300 mm wafer can house a chip to equip a full half-layer
  – requires dedicated chip design
Wafer-scale chip (2)

- Starting from ALPIDE architecture
- Porting to 65 nm technology node
  - smaller pixels
  - larger wafers (300 mm instead of 200 mm)
- Basic building block of 15 mm height
  - to be repeated n times in vertical direction to obtain the sizes needed per layer

Possible architecture

Figure 6: Diagram of stitched sensor in one direction (horizontal and vertical dimensions not to scale). Stitching in the vertical direction is also possible.

2.3.1 CMOS TECHNOLOGY OPTIONS

The baseline technology for the development of the proposed sensor is the 65 nm CMOS process of Tower Semiconductor, which offers a number of advantages with respect to the 180 nm process used for the development of ALPIDE:

- The process, which uses wafers that are 300 mm in diameter, allows the realization of the entire half-cylinder as a single chip. On the other hand, the 180 nm process uses wafers that are 200 mm in diameter. In this case, each half-cylinder would need to be further segmented in the longitudinal direction (at $z = 0$) in two halves (quarter-cylinders), with each quarter-cylinder realized as a single chip. This would not only complicate the mechanical and electrical integration, but also increase the material budget as it would require electrical interconnections (i.e. a flexible printed circuit board) to the second chip.

- Owing to the smaller feature size of the transistors, the pixel pitch can be reduced by a factor larger than two. This allows a significant reduction of the charge collection time and also a better position resolution.

The 180 nm is the fall-back option in the unlikely case the 65 nm would turn out to be too sensitive to radiation damage or inadequate for the realization of pixel sensors. Generic and specific R&D is planned to address this in the initial phase of the project (see Sec. 6.1). The 180 nm fall-back option is estimated to be slightly cheaper. The 65 nm option, however, will not only allow a simplification of detector layout and assembly, but will also enable the realization of a circuit with significantly enhanced performance, especially in terms of time resolution and of rate capabilities. This will certainly be beneficial also in terms of synergies with other projects and applications.
Thinning and bending silicon

- CMOS sensors are already very thin
  - ALPIDE is 50 µm thick
  - it uses an epitaxial layer of 25 µm as sensing layer, i.e. 50% of volume is active
  - thinner (18, 20 µm) epitaxial layers were also tried and yield similar performances

- Realistically heights of ≈ 30-40 µm are already possible
  - The 65 nm process has even thinner metal stack
  - smaller pixels would likely allow for even thinner epi-layers

- Below 50 µm, Si wafers become flexible, “paper-like”
Thinning and bending silicon

- Bending Si wafers and circuits is generally possible and done in industry.
- Radii much smaller than our needs have been achieved.
- Results can depend on circuitry.
  - Demonstration with ALPIDE wafers under way.
- Interconnection options to be studied.

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ITS2 Physics Performance - Heavy Flavour Examples

- Full reconstruction of the B meson down to 1 GeV/c
- $\Lambda_c$ baryon measurement in Pb-Pb collisions down to 2 GeV/c
- Access to the charmed baryon to charmed meson ratio
Physics Performance in Run 3 and Run 4 - $\Lambda_c$ Baryon Measurement

- Profits from improved pointing resolution
- Access to 0 - 10 % centrality class (instead of 0 - 20 % with ITS2)
- Crucial to refine the measurement of the total charm cross section
Physics Performance in Run 3 and Run 4 - Low Mass Dielectrons

- Reduction of photo conversion background by a factor of 3 due to lower material budget up to the first track point
- Reduced combinatorial background due to better identification of conversion electrons
- Better rejection of charm decay electrons due to the improved pointing resolution
Assembly procedure