



# Measurements with the CLICTD chip

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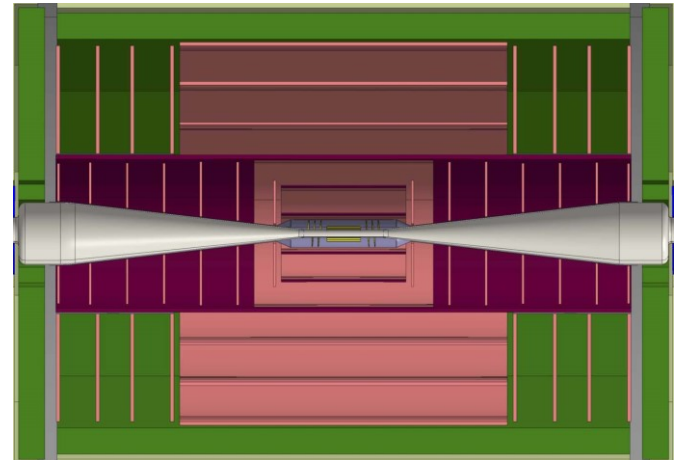
# Overview



- Introduction
- The process
- The CLICTD chip
- I-V characteristics
- Measurement results
- Summary and outlook

# Introduction

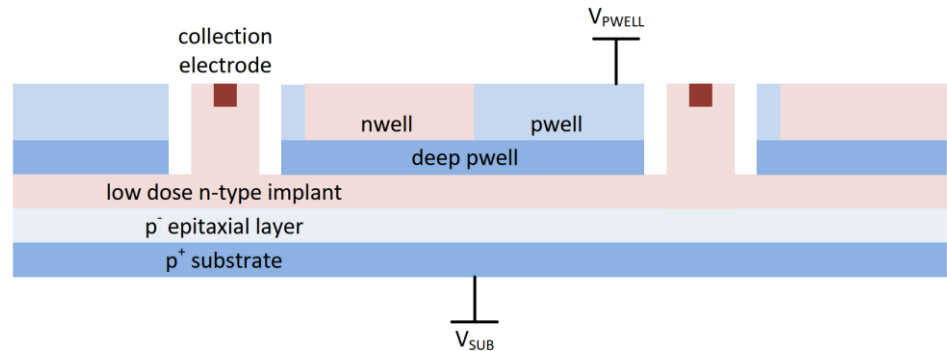
- The CLIC Tracker Detector (CLICTD) chip:
  - A monolithic pixelated detector chip designed in the framework of the CLIC silicon tracker study
  
- Requirements for a monolithic chip for the CLIC silicon tracker:
  - Single point resolution in one dimension  $\leq 7 \mu\text{m}$  (transverse plane)
  - Energy measurement with 5-bit resolution (ToT)
  - Time measurement with 10 ns bins and 8-bit resolution (ToA)
  - No multi-hit capability
  - Material budget 1-1.5%  $X_0$  (incl. supports, cables, cooling) (i.e.  $\sim 200 \mu\text{m}$  for silicon detector and readout)
  - Power consumption  $< 150 \text{ mW/cm}^2$  (Power pulsing, duty cycle 156 ns / 20 ms)



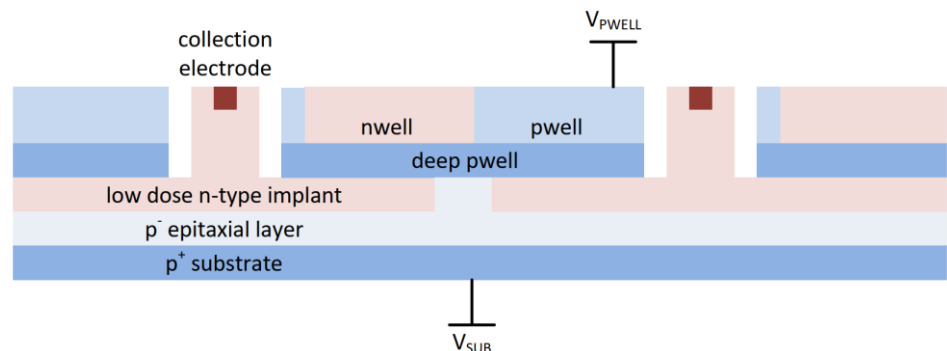
# The process

- The CLICTD chip was designed in a 180 nm CMOS imaging process
  - The signal is collected with a small N-well on the P-type high resistivity epitaxial layer (small detector capacitance → minimise analog power consumption)
  - Deep P-well shielding the on-channel electronics from the collection electrode
  - The epitaxial layer is fully depleted by including an additional deep N-type implant
  - Using a process split, additional wafers are produced with a segmented deep N-type implant

- 1<sup>st</sup> process split: continuous N-layer



- 2<sup>nd</sup> process split: gap in N-layer (only in the long dimension)
  - To increase the lateral field and thereby to reduce the charge collection time

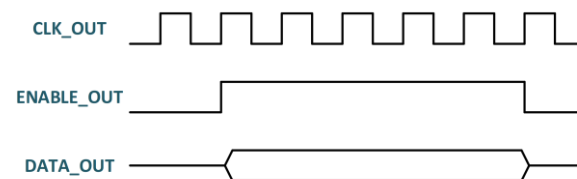
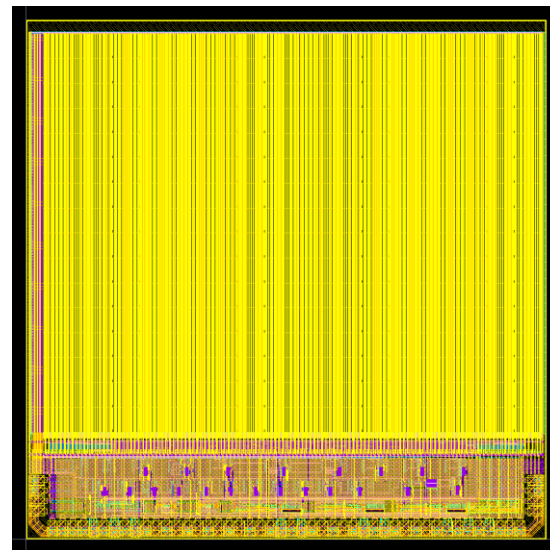







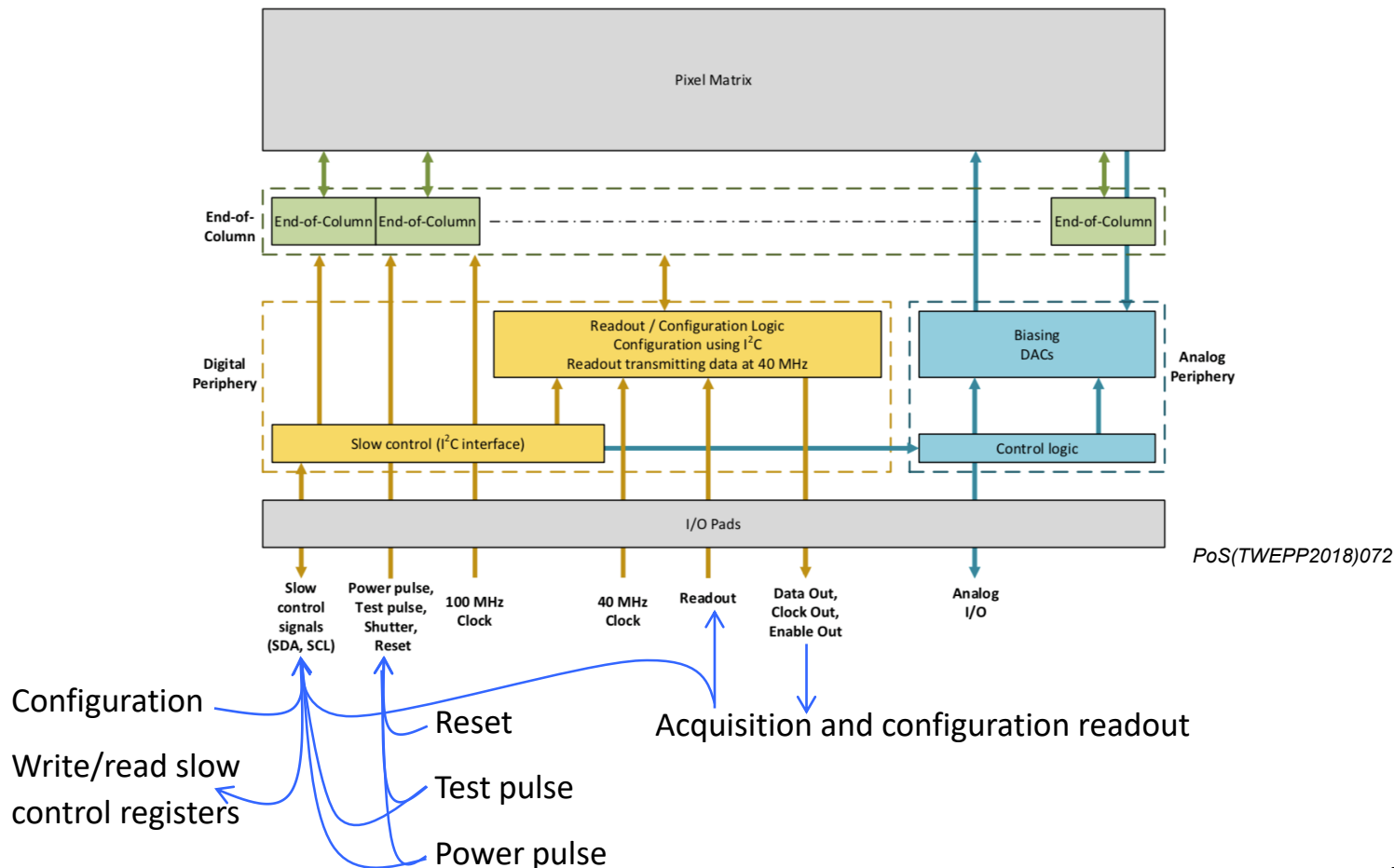
# The CLICTD chip

- The CLICTD chip:
  - Chip area:  $5 \times 5 \text{ mm}^2$
  - Sensitive area (pixel matrix):  $4.8 \times 3.84 \text{ mm}^2$
  - Number of pixels:  $16 \times 128$
  - Verified using UVM  
(Universal Verification Methodology)
- The CLICTD periphery and interface:
  - Analog periphery:
    - 20 DACs for biasing the analog part
    - Internal bandgap reference
  - Digital periphery:
    - I<sup>2</sup>C interface for the slow control
      - Reading / writing internal registers
      - Matrix configuration
    - Serial readout at 40 MHz
      - Readout time  $\sim 70 \mu\text{s}$   
(CLICTD matrix size, using compression, 1% occupancy)



# CLICTD verification (I)

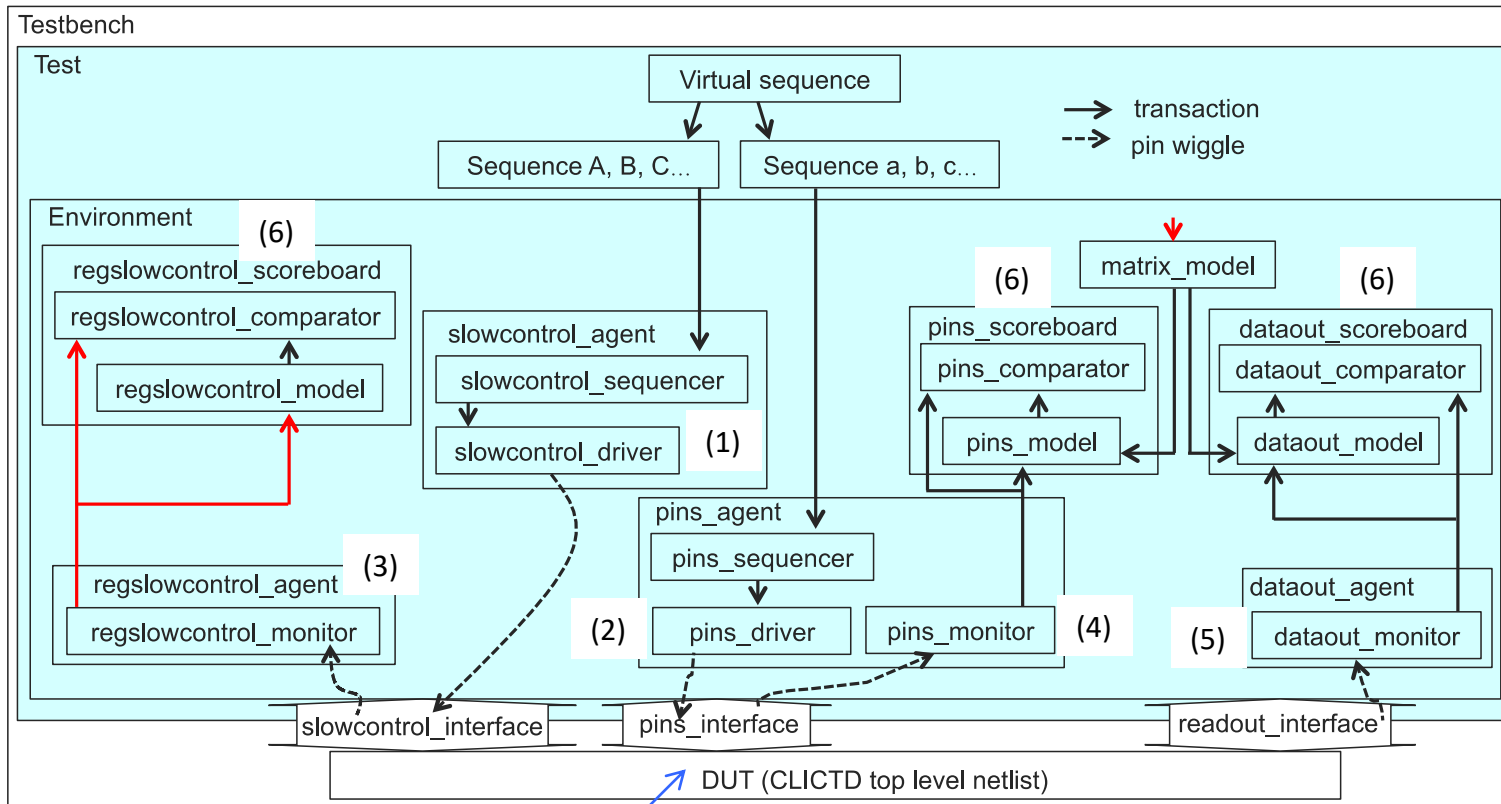
- Implemented using  (Universal Verification Methodology):
  - Randomized stimuli to maximize the number of operation scenarios simulated
- Simulated scenarios include the chip main operations:



# CLICTD verification (II)

The framework has been run on the intermediate and final versions of the RTL and postlayout netlist, unveiling some bugs that were successfully fixed

## UVM framework to verify the CLICTD

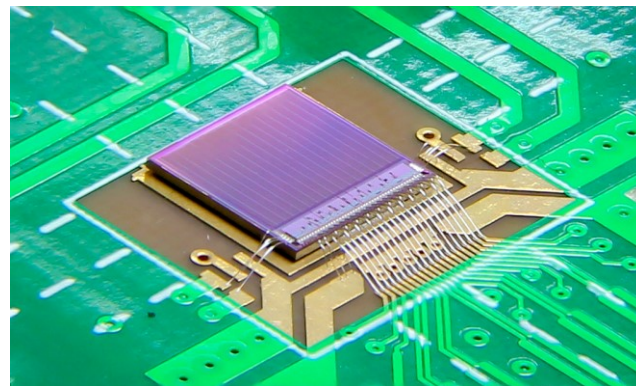


- (1) Send commands via the slow control
- (2) Send commands by activating pins
- (3) Read slow control registers
- (4) Read pin values
- (5) Read serial readout pin values
- (6) Report whether the chip response matches the expected values

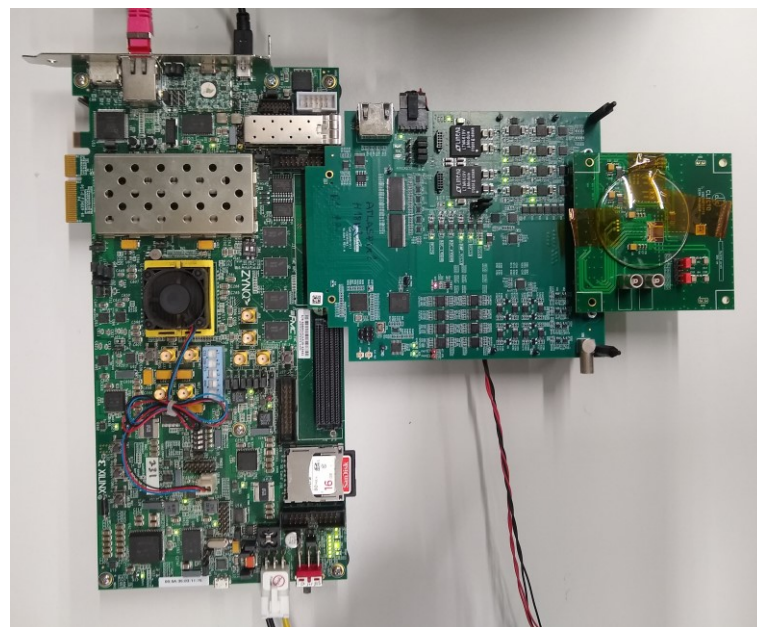
Device Under Test: in the last iteration, CLICTD post-layout top level netlist

# Measurement setup

- CLICTD chips received: July 2019
- First samples wire-bonded on PCB received shortly after
  - 2 samples from “Rev. A” – continuous N-implant
  - 1 sample from “Rev. B” – gap in N-implant
- Communication established using CaRIBOu DAQ
  - Based on a ZC-706 evaluation kit
    - ARM microprocessor + Kintex-7 FPGA
  - DAQ system provides:
    - Power supplies
    - Clocks
    - Communication interfaces
    - Analog I/O
    - Differential and single-ended digital signals

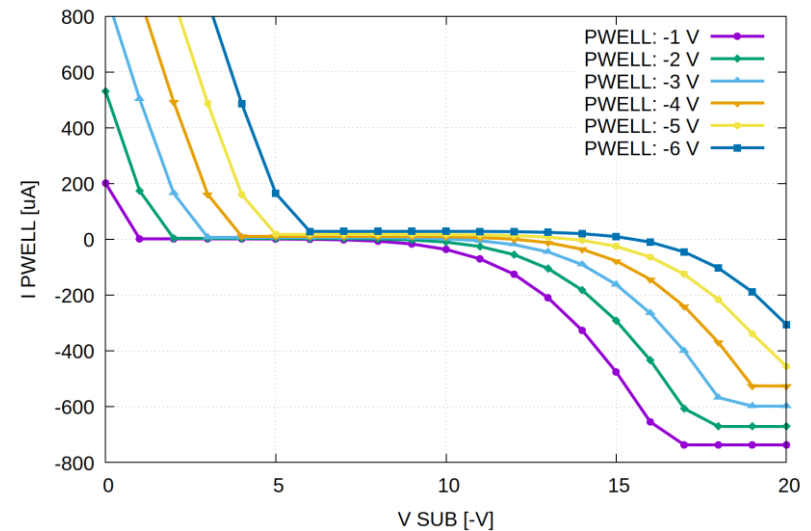
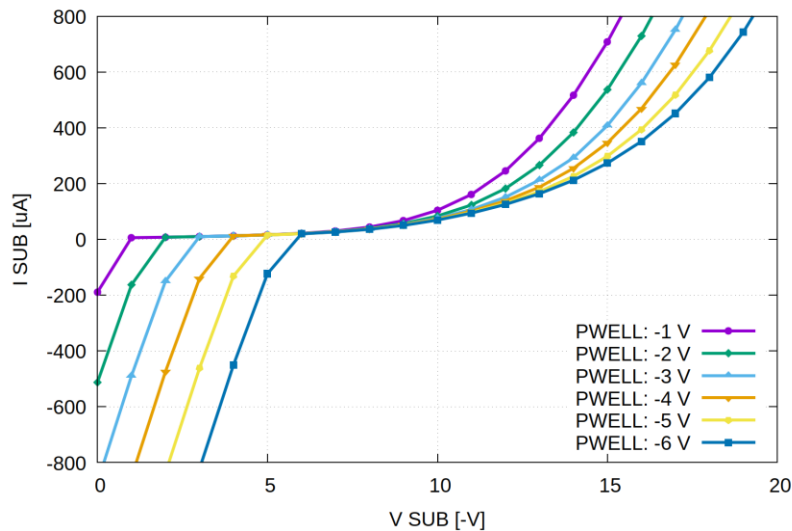
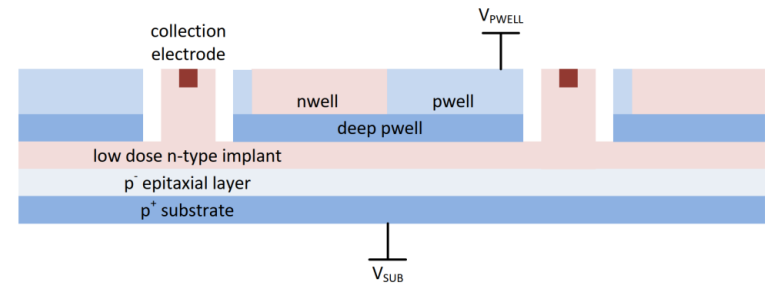


*Photo: M. Vicente*



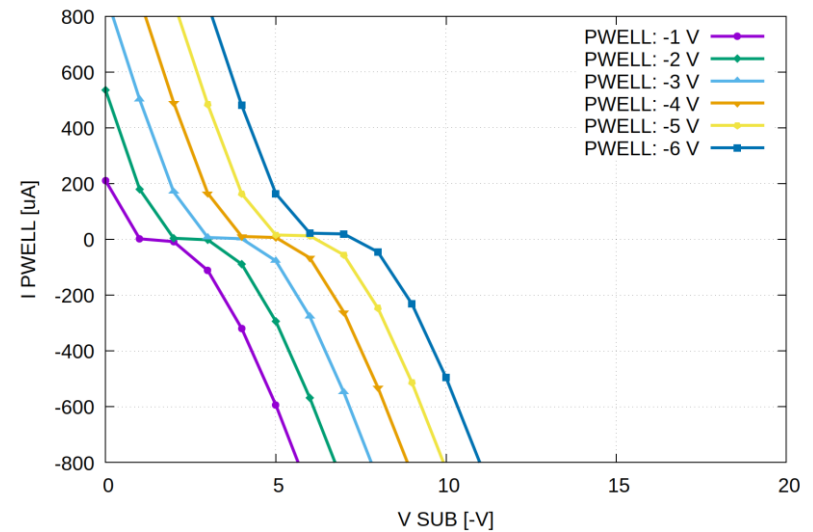
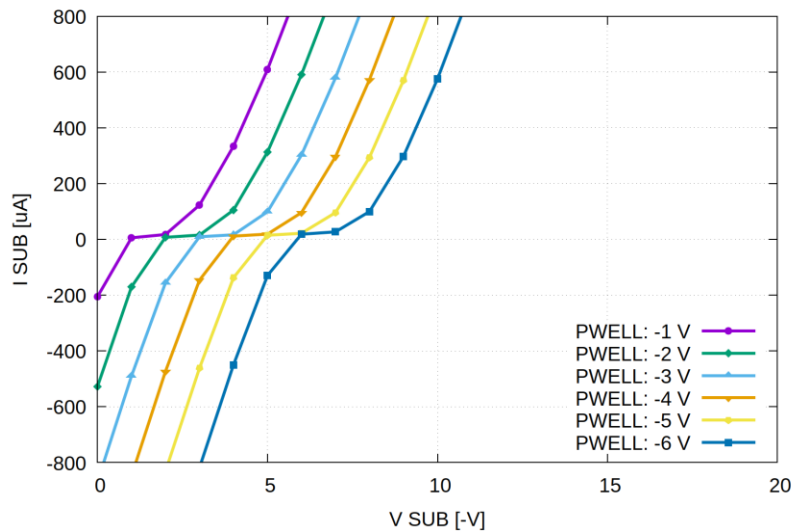
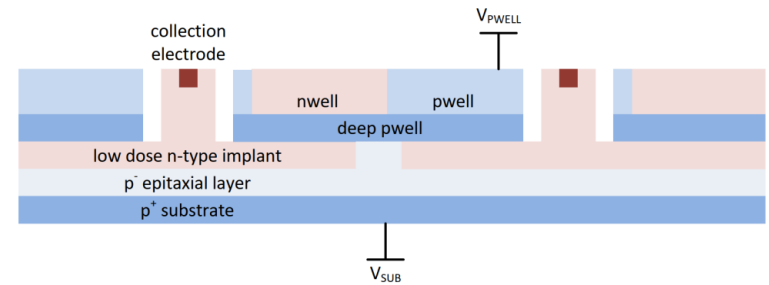
# I-V characteristics

- Sensor I-V measured by scanning the substrate bias, for different values of the deep P-well bias
- Leakage current was measured at both nodes: SUB and PWELL (using two external power supplies)
- 1<sup>st</sup> process split: continuous N-layer



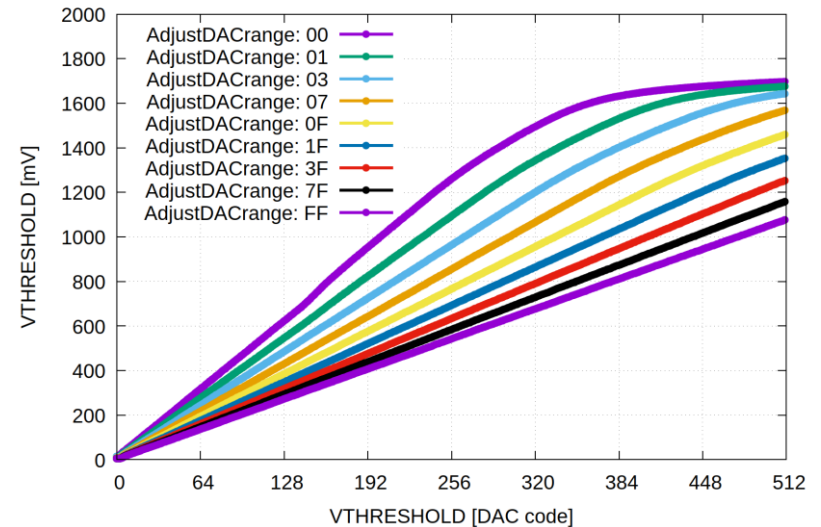
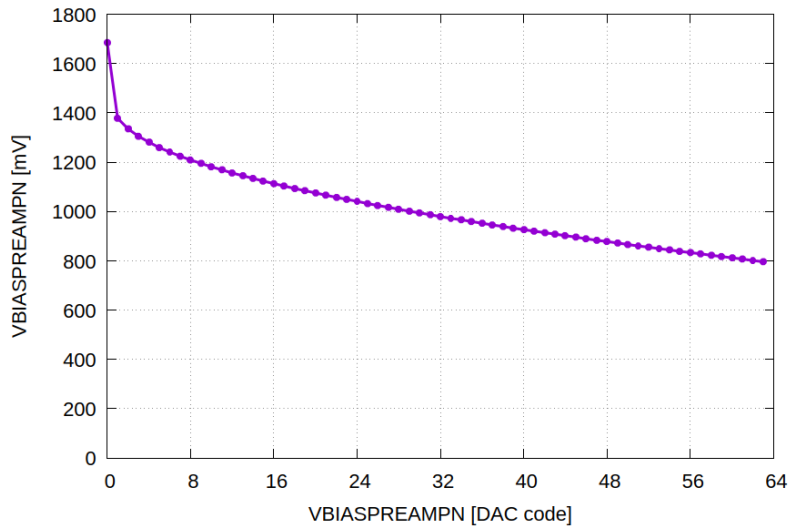
# I-V characteristics

- 2<sup>nd</sup> process split: gap in N-layer
- Reduced isolation due to the gap in the N-layer



# DAC scans

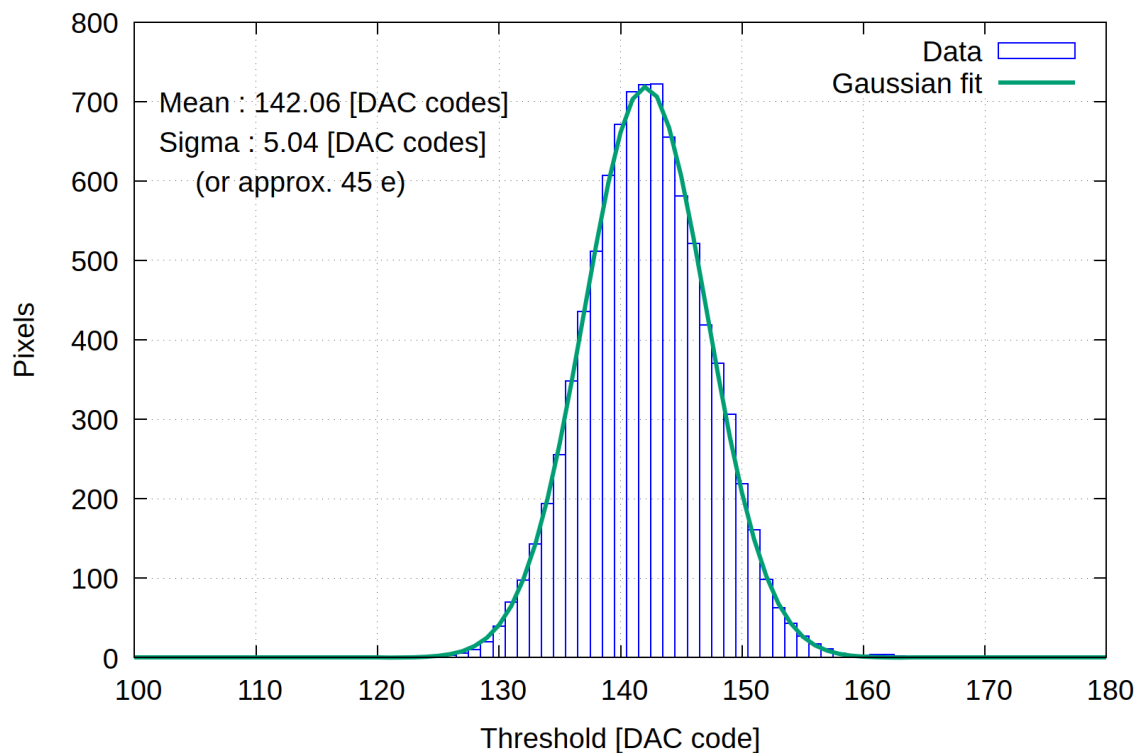
- Current and voltage DACs were scanned, confirming that they operate as expected
  - Example current DAC (left): preamplifier bias current
  - Example voltage DAC (right): threshold voltage
    - Threshold voltage scanned for different values of the register for tuning the DAC range



# Threshold scan

- Unequalised matrix
- Local threshold tuning DACs set to mid-range
- Front-end not tuned

*Preliminary results  
-  
Work in progress*



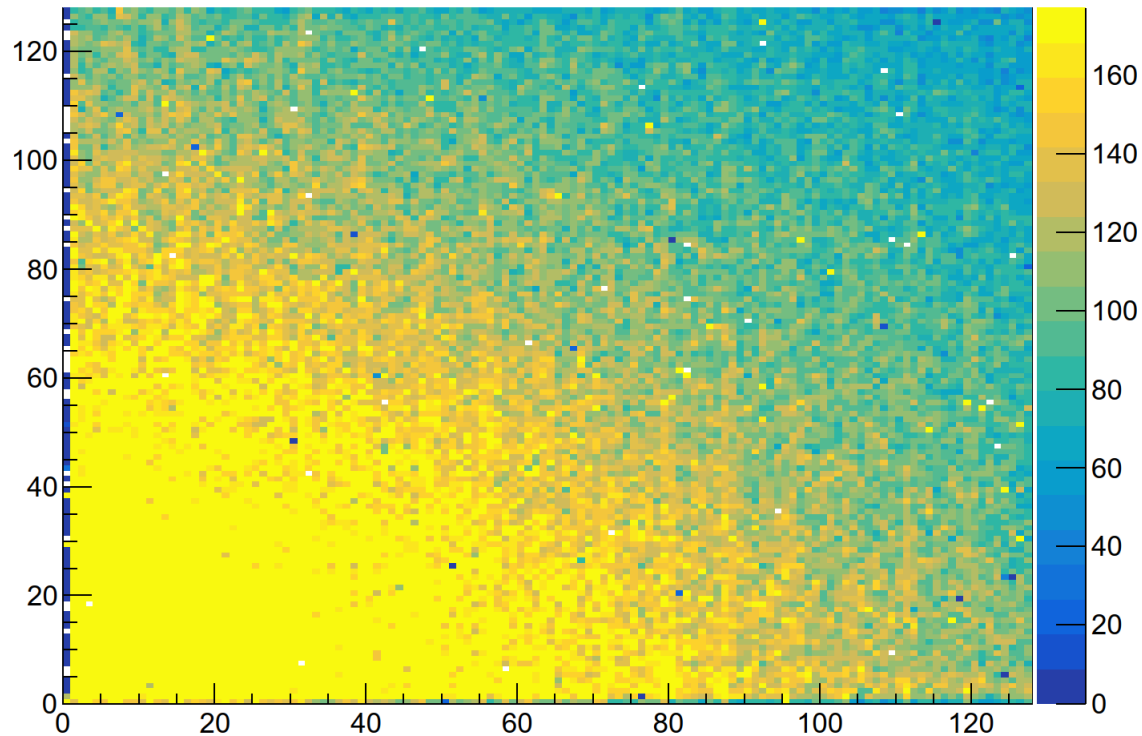
*Sample from  
1<sup>st</sup> process split*

# Measurement with Sr90 source

- Unequalised matrix, counting mode
- Global threshold set to  $\sim 240$  e $^-$ . Local threshold tuning DACs set to mid-range
- Front-end not tuned
- 10000 frames – 40 ms long shutter

CLICTD source measurement hitmap

*Sample from  
1<sup>st</sup> process split*



*Preliminary results  
-  
Work in progress*

Plot: K. Dort

# Power consumption

- Analog power consumption: 40 mW (22 mA @ 1.8 V VDDA) for the full chip
  - After applying power pulsing: power reduced to 9 mW (5 mA)
    - Close to the  $\sim 8$  mW expected for the analog periphery
  - Power consumption of the analog front-end is configurable by periphery DACs
    - Currently at 170 mW/cm<sup>2</sup>
    - Can be further studied and optimised following detailed characterisation of the front-end
- Digital power consumption: 80 mW (45 mA @ 1.8 V VDDD) for the full chip
  - 45 mW estimated for clock distribution (corresponding to 240 mW/cm<sup>2</sup>)
  - 20 mW LVDS drivers (3 drivers in chip)
  - 5 mW LVDS receivers (Simulated value, 2 receivers in chip)
  - 10 mW estimated for digital periphery
- Power pulsing:
  - Analog power consumption during standby:  $\sim 2$  mW/cm<sup>2</sup>
  - Digital domain: the clock stops being distributed in the matrix. Simulated static leakage power:  $\sim 0.6$  mW/cm<sup>2</sup>
  - Estimated total power consumption during standby (analog + digital):  $\sim 3$  mW/cm<sup>2</sup> + 43 mW periphery
  - Estimated average power consumption over the CLIC cycle:  **$\sim 4$  mW/cm<sup>2</sup> + 43 mW periphery**  
 (50 Hz cycle, assuming 30  $\mu$ s power-on time, in order to allow the front-end to be ready for detecting particles)

*Preliminary results  
-  
Work in progress*



# Summary and outlook



- The CLICTD chip:
  - Simultaneous 8-bit ToA and 5-bit ToT measurement
  - Cell dimensions:  $300 \times 30 \mu\text{m}^2$
  - Sensitive area:  $4.8 \times 3.84 \text{ mm}^2$  (16 columns, 128 rows)
  - Chip dimensions:  $5 \times 5 \text{ mm}^2$
  - Two versions produced:
    - Version 1: continuous N-layer
    - Version 2: gap in N-layer
- First results with the chip obtained:
  - Sensor I-V characteristics indicate that the sensor can be operated at its nominal bias
  - CLICTD chip periphery (slow control, DACs) performs as expected
  - First results from the matrix readout obtained
- Next steps:
  - Matrix equalisation
  - Study of the front-end performance
  - Timing and charge sharing studies in order to compare the two process options
  - First beam test with the CLICTD chip planned for late September 2019 at DESY