



Power pulsing with CLICpix2

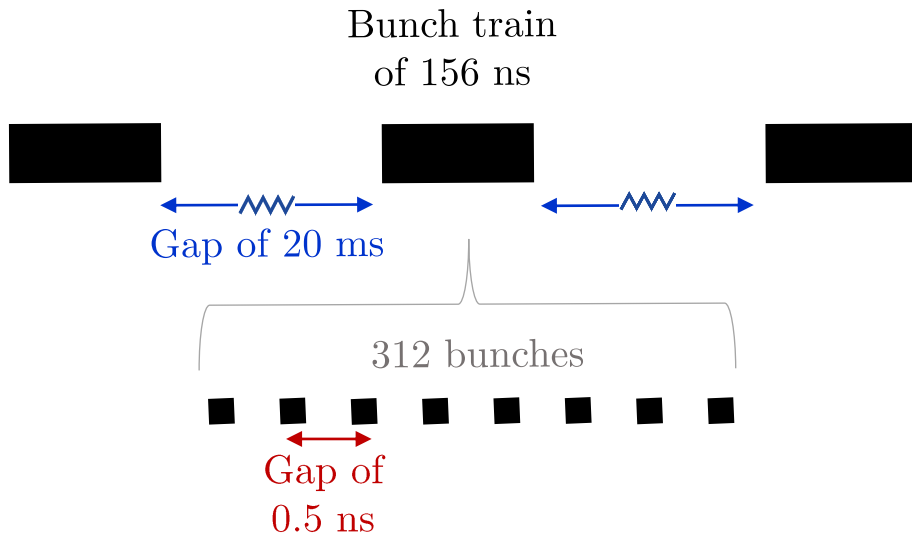
Sara Ruiz Daza, Magdalena Munker, Simon Spannagel, Iraklis Kremastiotis

Outline



- Introduction
- Power pulsing
- CLICpix2
- Analogue Power Pulsing results with CLICpix2
- Summary

Introduction



Beam structure

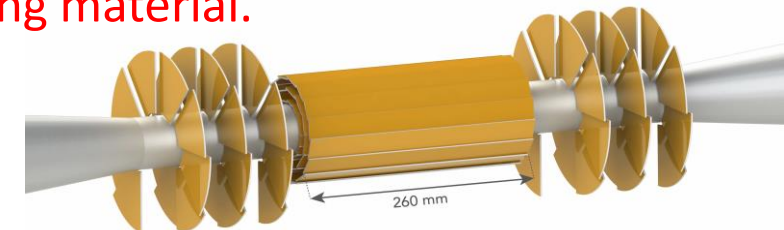
- e^+e^- collision
- Trains of 312 bunches
- Spacing between bunches: 0.5 ns
- **Gap between trains: 20 ms** (50 Hz rate)

- Important for power pulsing since the electronics can be switched off most of the time.
- Study of the power-off state.

Vertex detector requirements

- Single point resolution $\sigma \sim 3 \mu\text{m}$
- Time slicing of 10 ns
- **Power dissipation below 50 mW/cm²**
- **Ultra-low mass ($\sim 0.2 \% \chi_o$ per layer)**

Motivates power pulsing to reduce the heat dissipation and thus the cooling material.



Power pulsing



Power pulsing: Providing power only in small intervals, and the rest of the time keep the electronics in a low or off power mode.

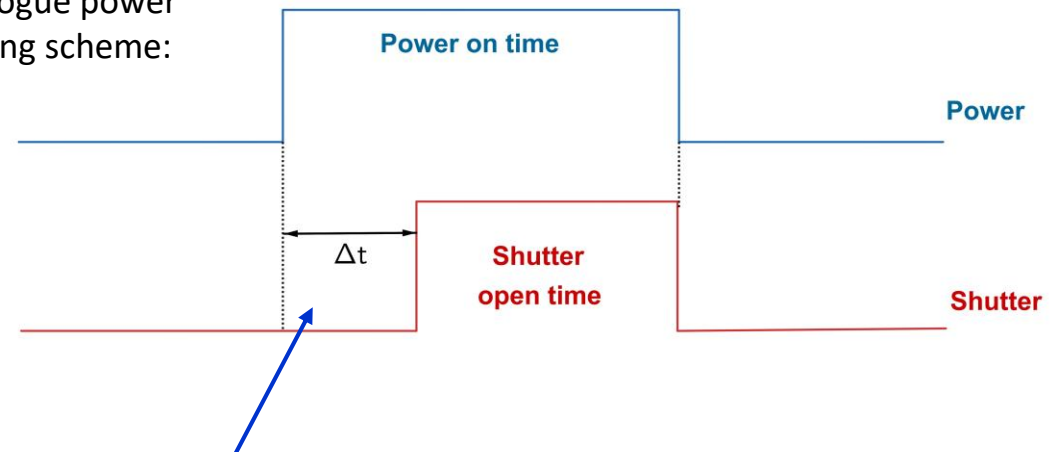
- Long gaps between bunch trains (**20 ms**) allow for power pulsing.

Advantages:

- Reduce average power consumption
 - Reduce heat dissipation
 - No need for cooling pipes
 - Air flow cooling sufficient to remove heat
- ⇒ Low power consumption and low material budget requirements are satisfied

The chip only acquires data when the shutter is open (**shutter-based readout**).

Analogue power pulsing scheme:



Delay time : $\Delta t = \Delta t$ (power on – shutter open)

Shutter open $\sim 2\text{ms}$

CLICpix2: Readout chip developed to meet the requirements of CLIC vertex detector, including analogue power pulsing functionality.

- Chip matrix: 128×128 pixels with a size of $25 \times 25 \mu\text{m}^2$
- It has shutter-based readout
- Simultaneous time (ToA) and energy (ToT) measurements
- Digital power pulsing is not implemented in CLICpix2

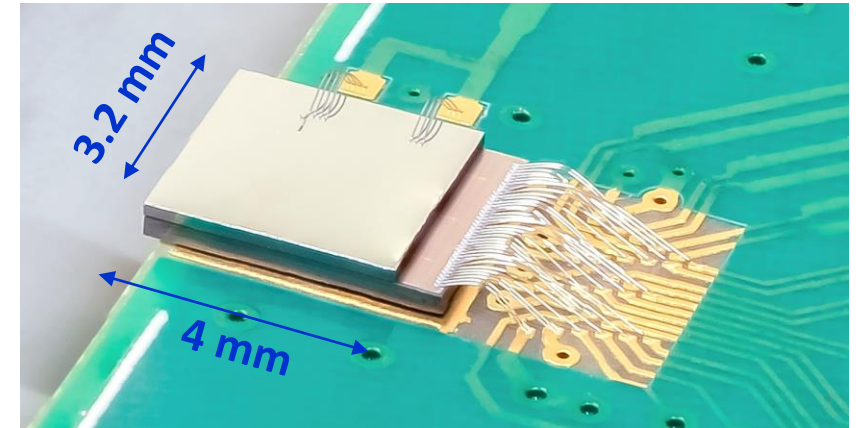


Photo: M.V. Barreto

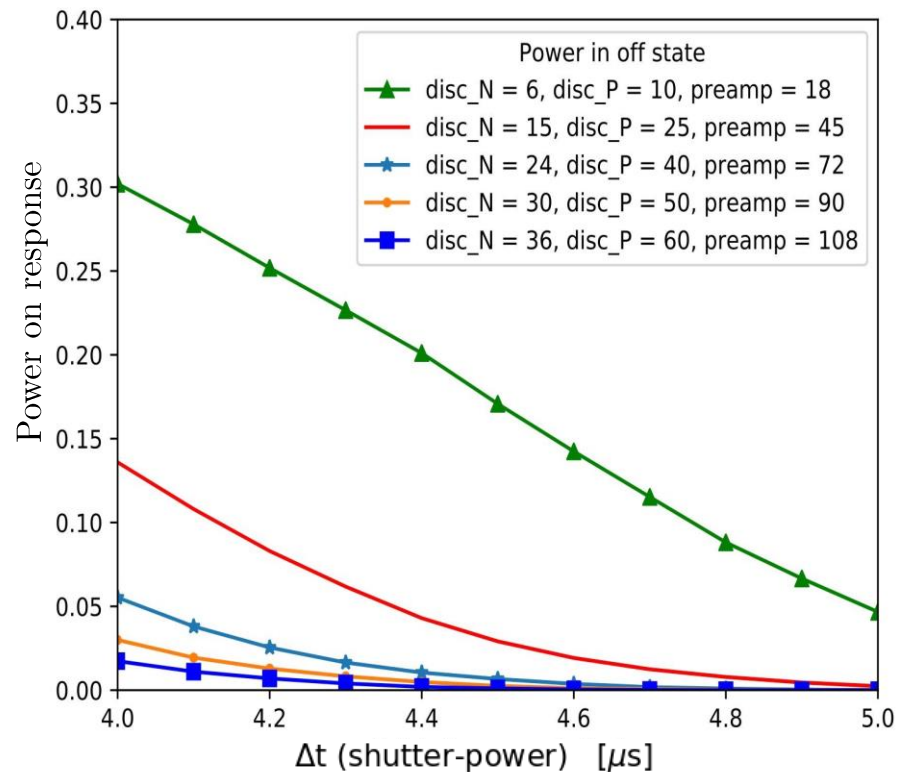
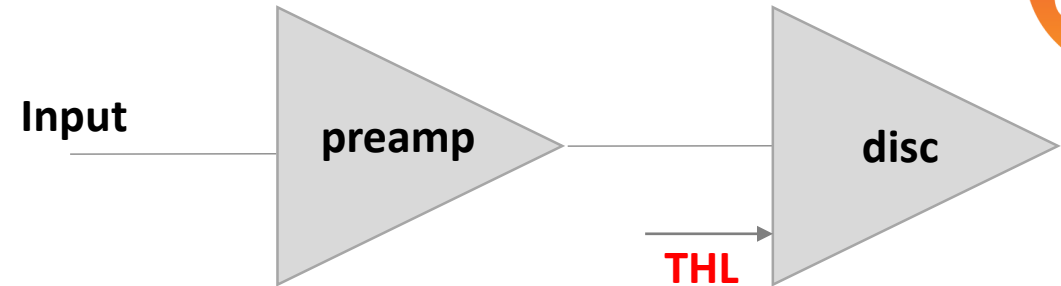
Analogue power pulsing with CLICpix2: turn off/low mode most power consuming nodes of the analogue circuitry (amplifier and discriminator)

Configurable parameters in the power-off state

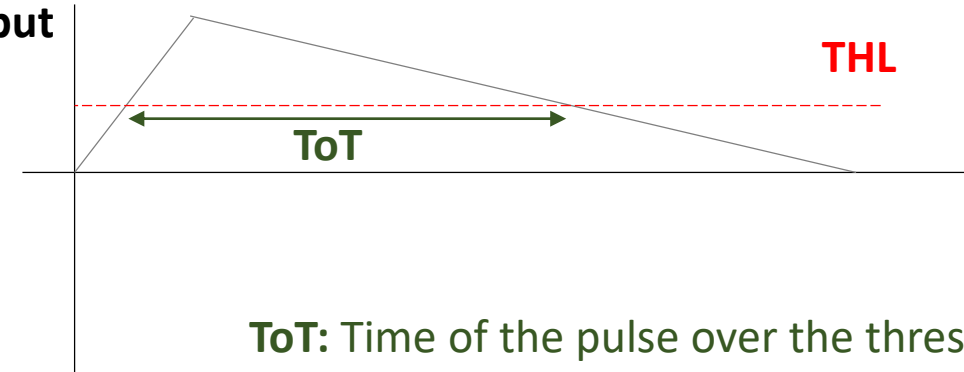


Configurable parameters in the power-off state:

- Bias of the pixel preamplifier: **preamp**
- Bias of the NMOS (PMOS) current source in the discriminator: **discN** (**discP**)



preamp
output

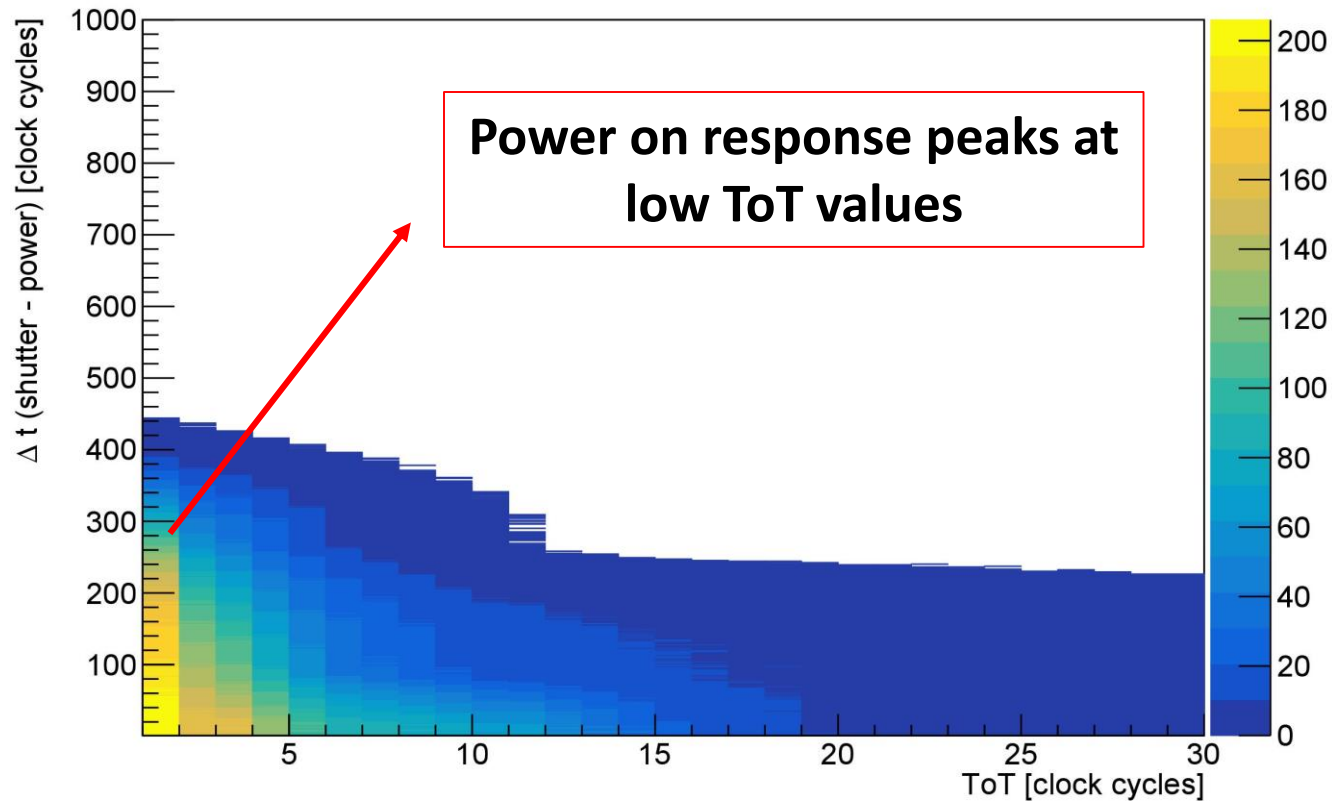


ToT: Time of the pulse over the threshold.

Power on response: fraction of pixels firing after turning on the power (no particle signal)

- The lower the off-state bias, the longer it takes the chip to become quiet
→ **A balance needs to be found between saving power and reducing Δt**

ToT of power on response



→ **Question:** Can we distinguish between the signal (real particle hit) and the power on response?

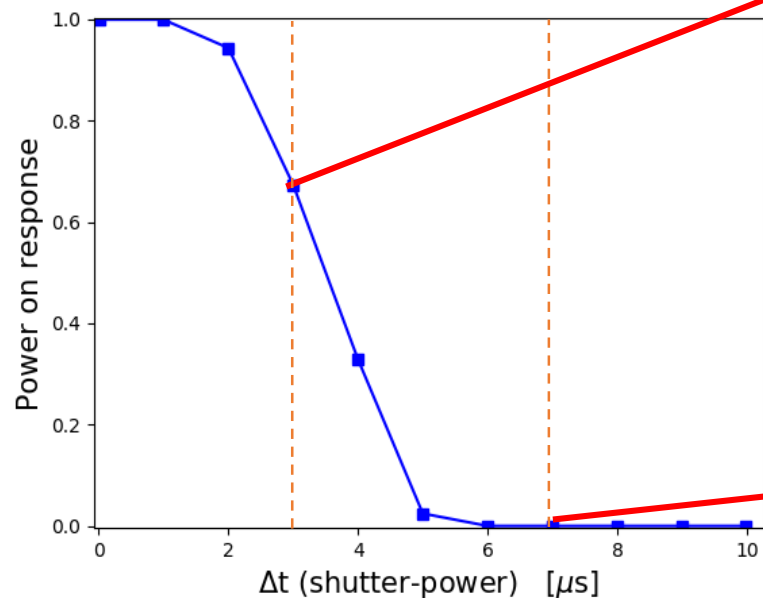
→ **Answer:** Yes!



Source measurements with Sr90

ToT of power on response and particle signal

The chip is quiet after $6 \mu\text{s}$

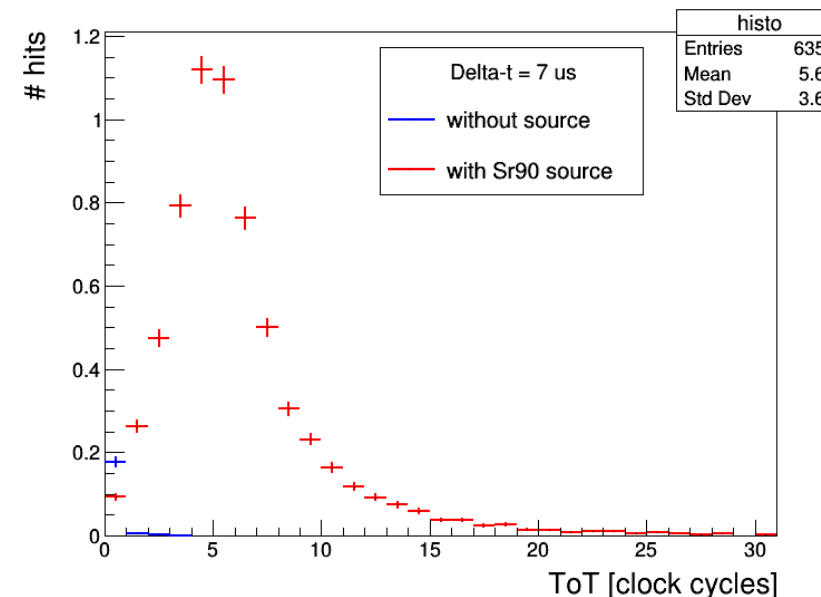
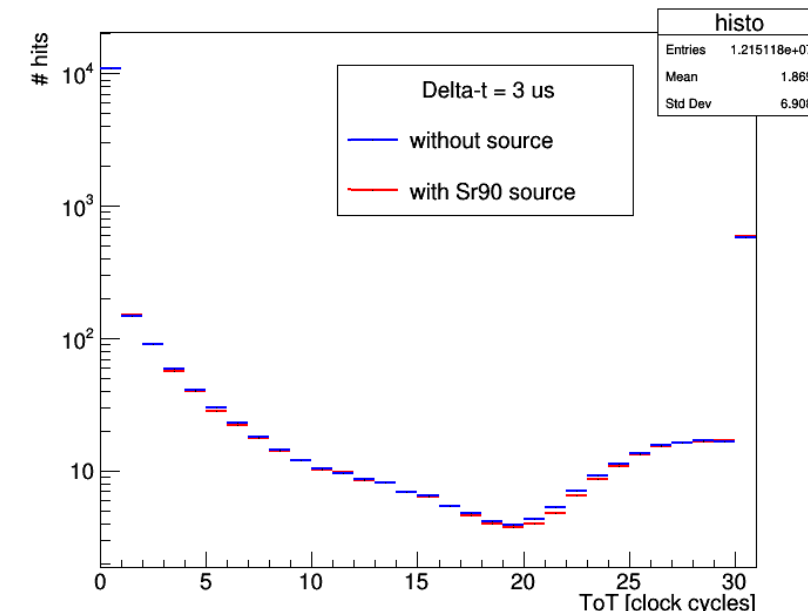


$\Delta t = 3 \mu\text{s}$
(within power on response)

- Power on response has a large peak at **ToT 0**.
- When the **chip is not quiet**, the signal is dominated by the power on response.

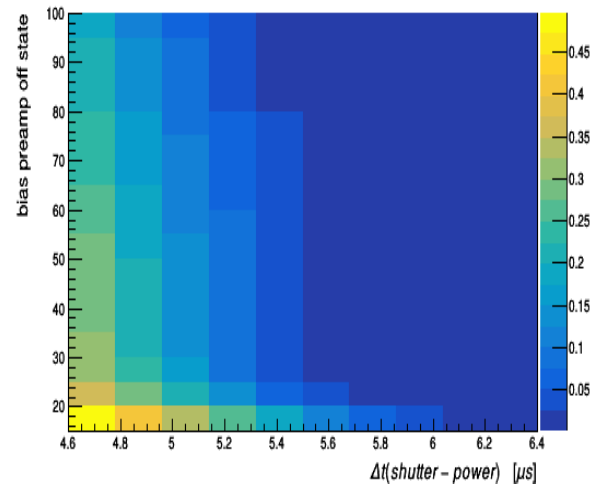
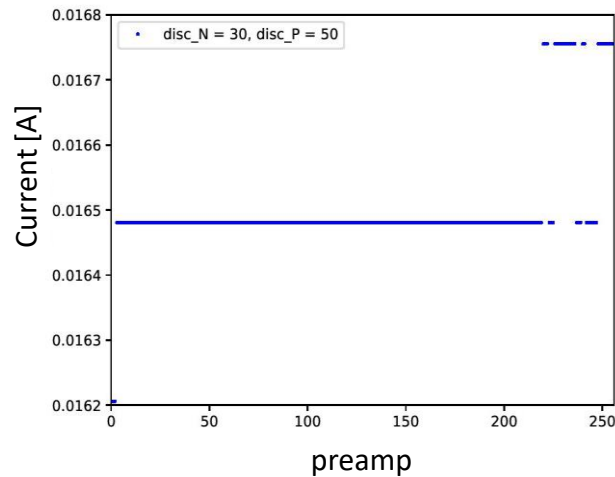
$\Delta t = 7 \mu\text{s}$
(out of power on response)

- There is not power on response.
- When the **chip is quiet**, the signal is well defined.

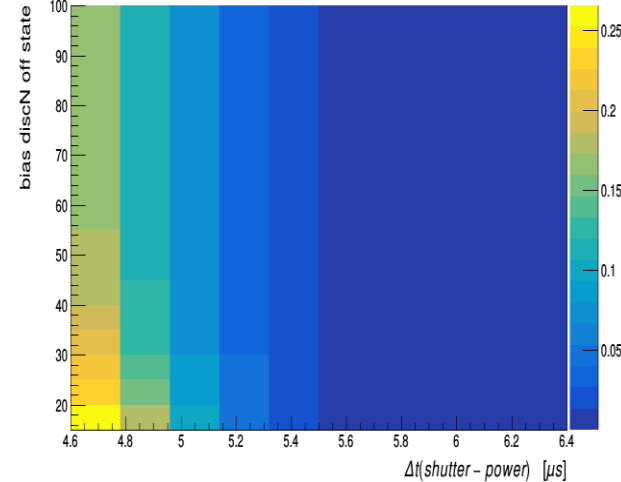
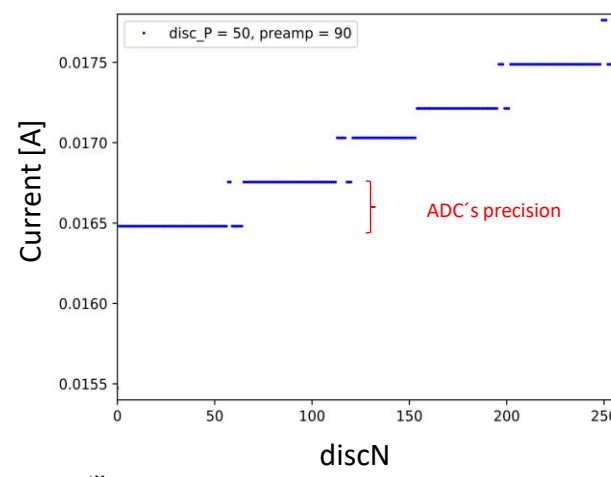


Power consumption for different power-off states

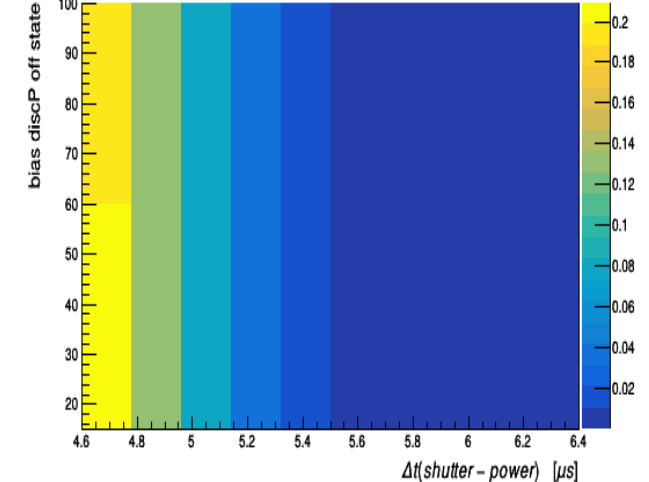
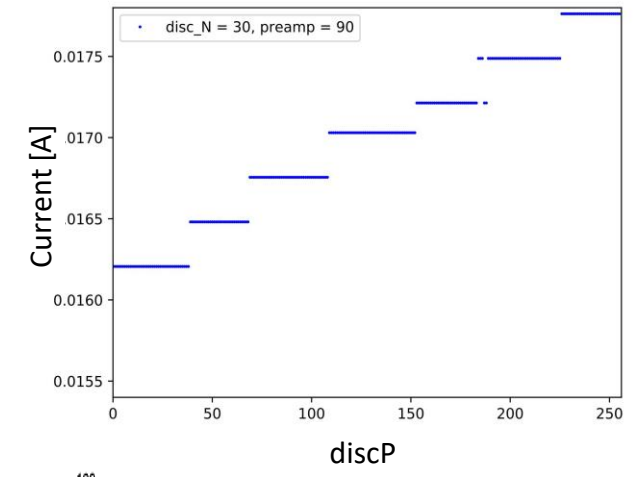
Scan of the preamp



Scan of the discN

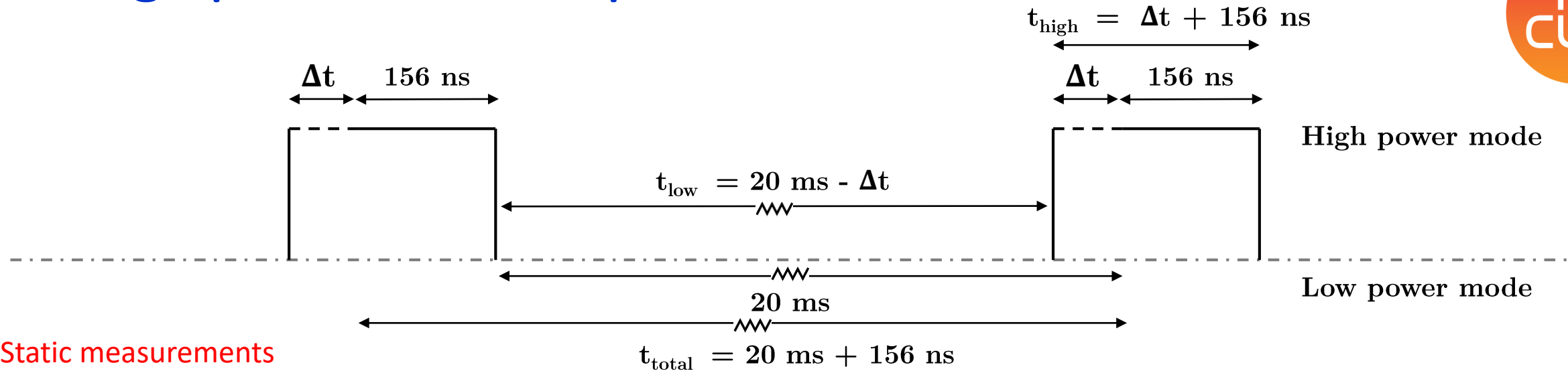


Scan of the discP



- By increasing the **bias of the preamplifier**, the power consumption change is negligible and Δt decreases few μs .
- The **bias of the discriminator** increases the power consumption significantly \rightarrow set at the lowest possible value

Average power consumption for CLIC conditions



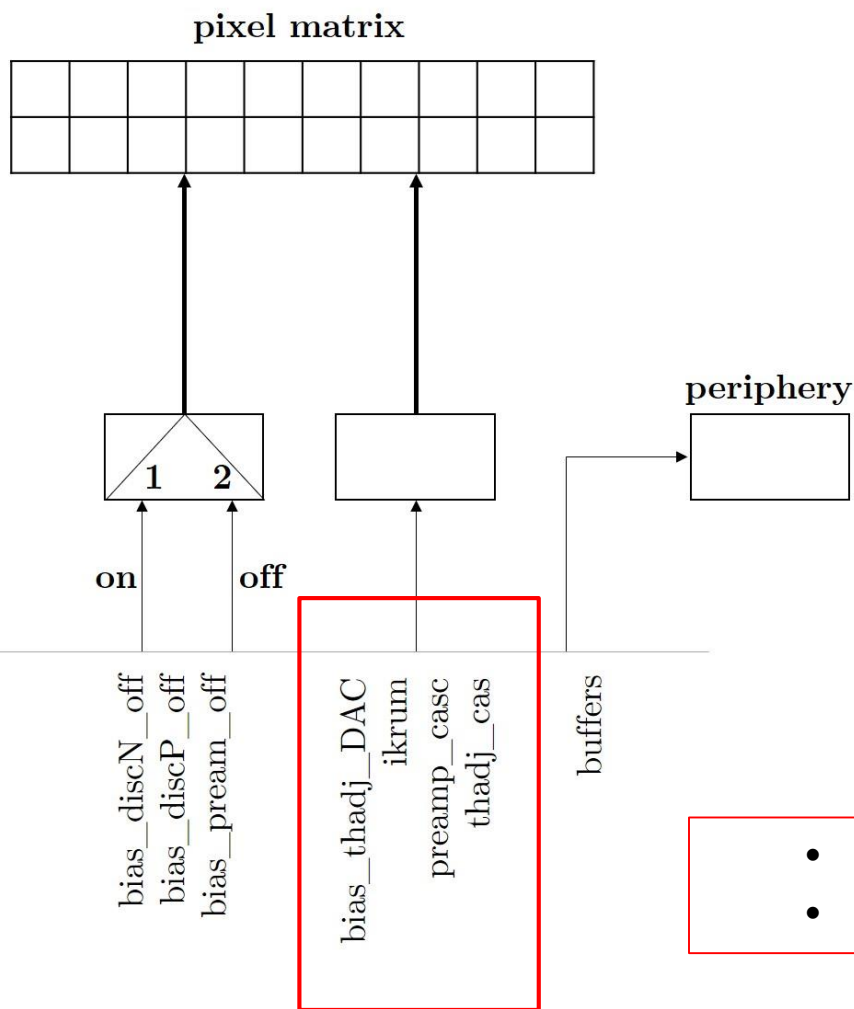
Static measurements

$$w_{high} = \frac{t_{high}}{t_{total}} \quad ; \quad w_{low} = \frac{t_{low}}{t_{total}} \quad ; \quad P_{aver/cycle} = w_{low} \cdot P_{low} + w_{high} \cdot P_{high} \quad ; \quad P_{high} = 984.4 \text{ mW/cm}^2$$

Power-off state	Δt [μs]	P_{low} [mW / cm^2]	W_{high}	W_{low}	$P_{aver/CLIC's \text{ cycle}}$ [mW / cm^2]
With nominal values (discN = 30, discP = 50, preamp = 90)	6	193.4	0.0003	0.9997	193.4
With nominal preamp and lowest power-off state of the discriminator (discN = 5, discP = 5, preamp = 90)	10	189.5	0.0005	0.9995	189.9
Lowest power-off state (discN = discP = preamp = 0)	55	187.5	0.0028	0.9972	187.7

→ The power off/low mode is the dominant state

New DAC candidates for analogue power pulsing



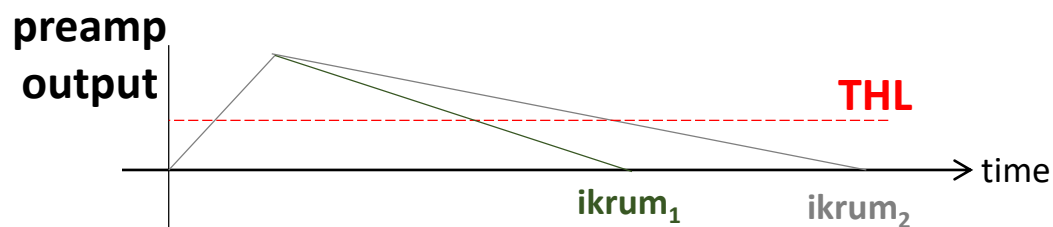
new candidates

- Bias for the pixel threshold adjustment DAC: **thadj_DAC**

Idea: Each pixel has its own local threshold and it needs to be set.

- Bias for the pixel feedback stage: **ikrum**

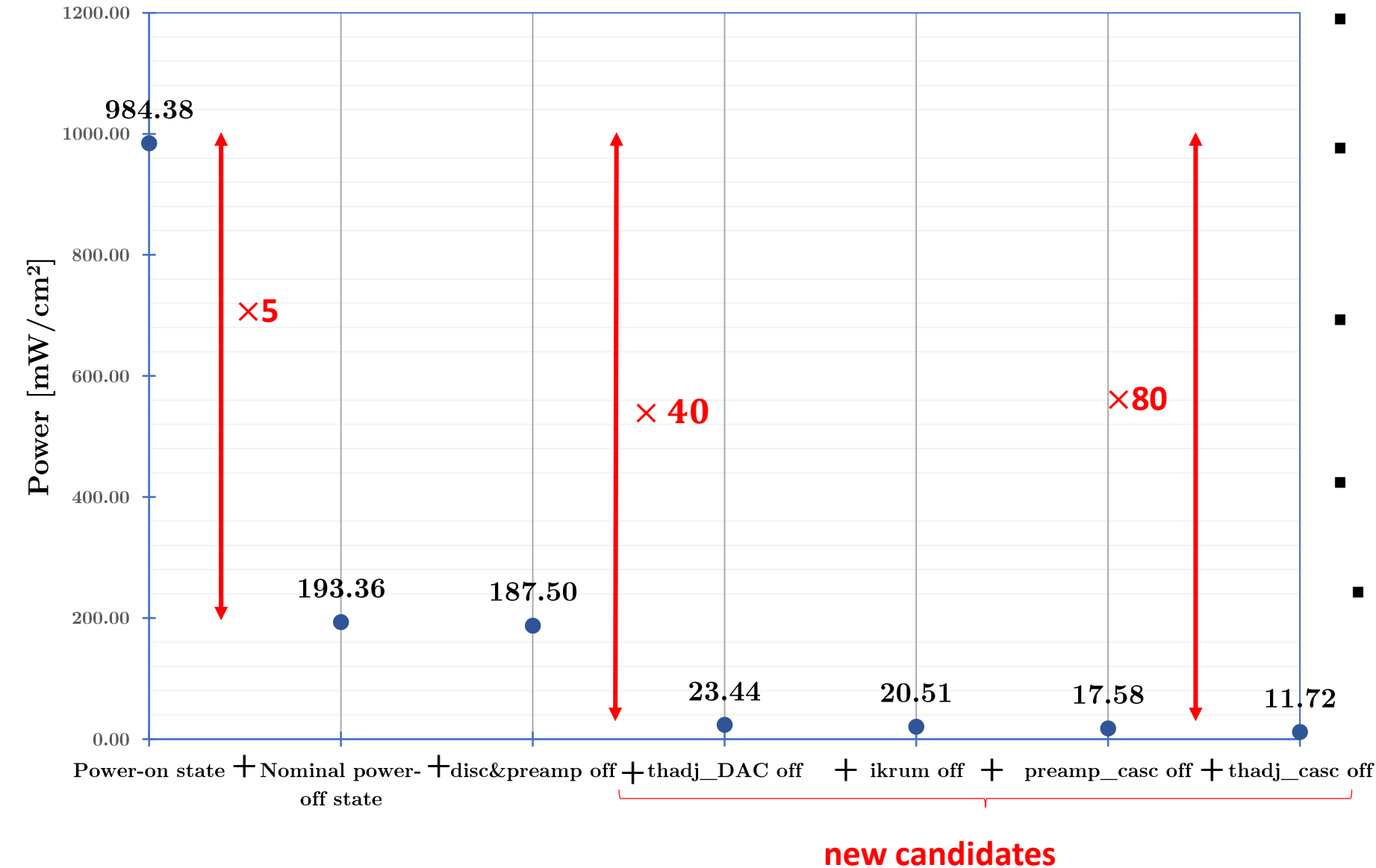
ikrum: discharge time of a signal



- Voltage bias for the cascode of the pixel preamplifier: **preamp_casc**
- Voltage bias for the cascode of the pixel threshold adjustment DAC: **thadj_casc**

They can not be power pulsed in CLICpix2! Static measurements on/off power

New DACs candidates for analogue power pulsing



- Found **4 new candidates** for power pulsing.
- By power pulsing them, we **reduce the power consumption by a factor of ~ 80** .
- CLICTD** power pulses the bias of the threshold adjustment DAC (See talk by I. Kremastiotis).
- $P_{\text{aver/cycle}} = 22.5 \text{ mW/cm}^2$ (theoretical scenario for CLICpix2)
- 11.72 mW/cm^2** will be the offset of the periphery (the periphery does not scale with the chip size, thus the power consumption of the periphery will be less significant for larger chips)

Summary & Outlook



□ Summary:

- **Analogue power pulsing** (to reach ultra low mass requirement) tested with **CLICpix2**
- Study of power on response from analogue power pulsing in CLICpix2: **chip is quiet** (ready to detect the particle) **after $\sim 6 \mu\text{s}$** .
- Source measurements with Sr90 to **distinguish between the signal and power on response**.
- Low CLIC duty cycle \rightarrow long **power off/low state**, which has **high contribution to the average power consumption**.
 - Analogue power pulsing reduces the total power consumption by a factor of 5.
- Found **new DAC's candidates for power pulsing...** power consumption could be reduced by a factor of 80.

Summary & Outlook



□ Next steps:

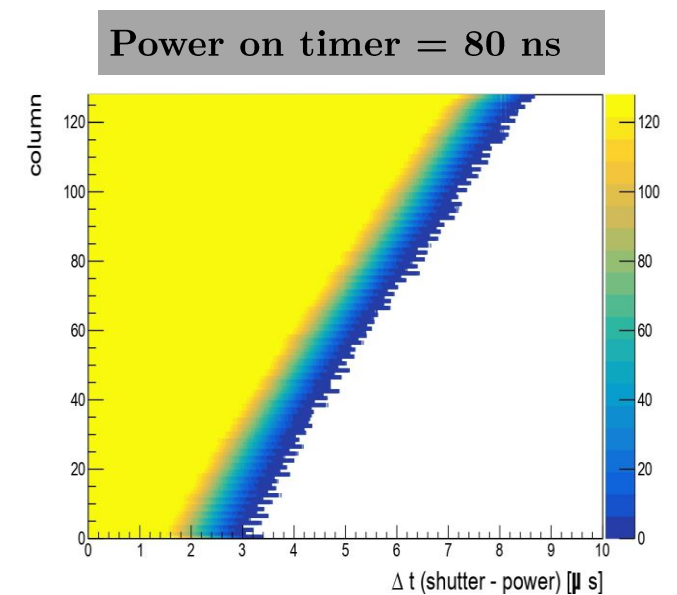
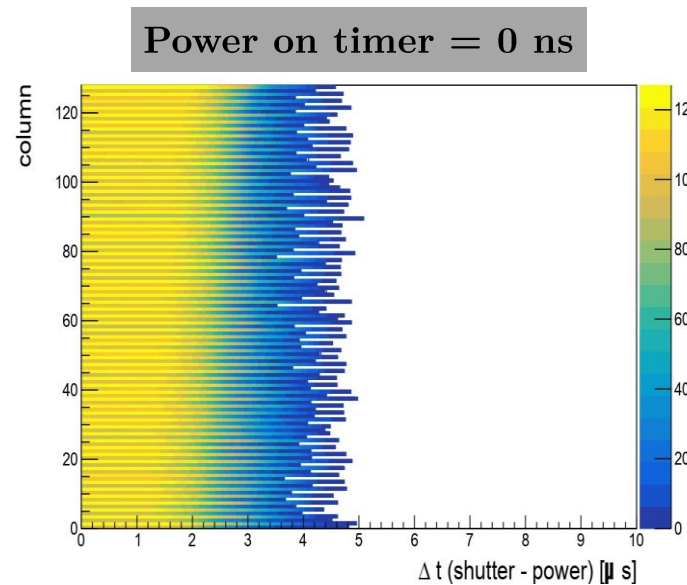
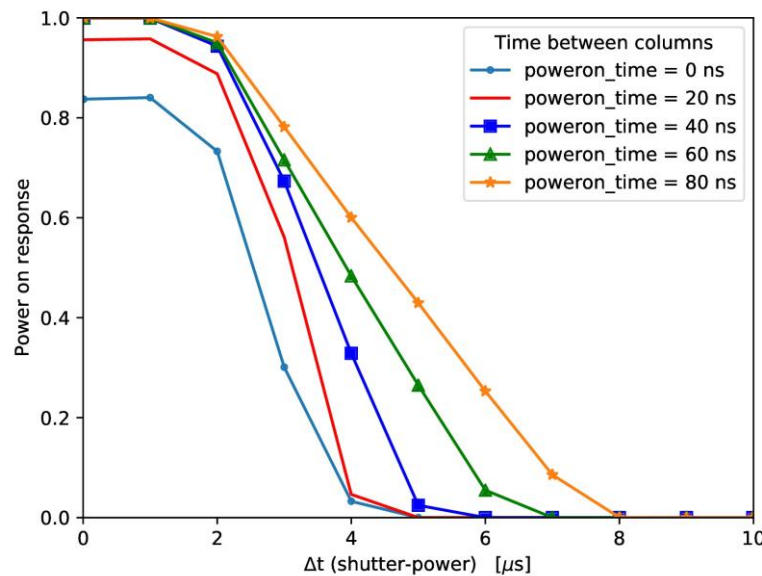
- **Test-beam data analysis** to calculate efficiency during power pulsing
- Study of power pulsing with **CLICTD chip**: includes features for digital power pulsing (clock gating) and more advanced analogue power pulsing features

Backup:

Optimum delay time

$$\Delta t = \Delta t (\text{power on} - \text{shutter open})$$

- **Power on response:** fraction of pixels firing after turning on the power (no particle signal)
- Pixel columns can be powered on with delay between consecutive columns to avoid peaks in power. Delay defined as: **power on timer**



- Different delays (power on timers) visible in power on response over the pixel matrix.

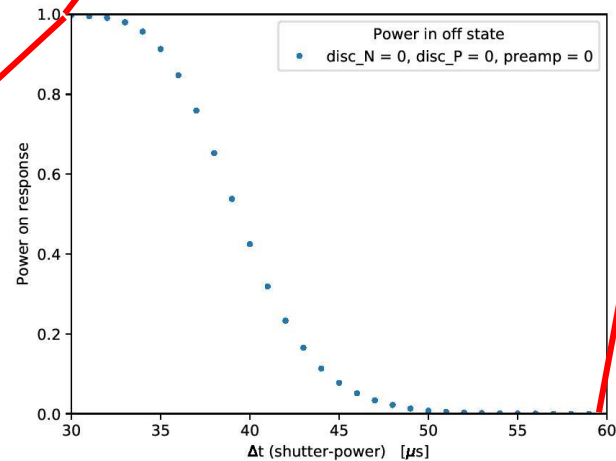
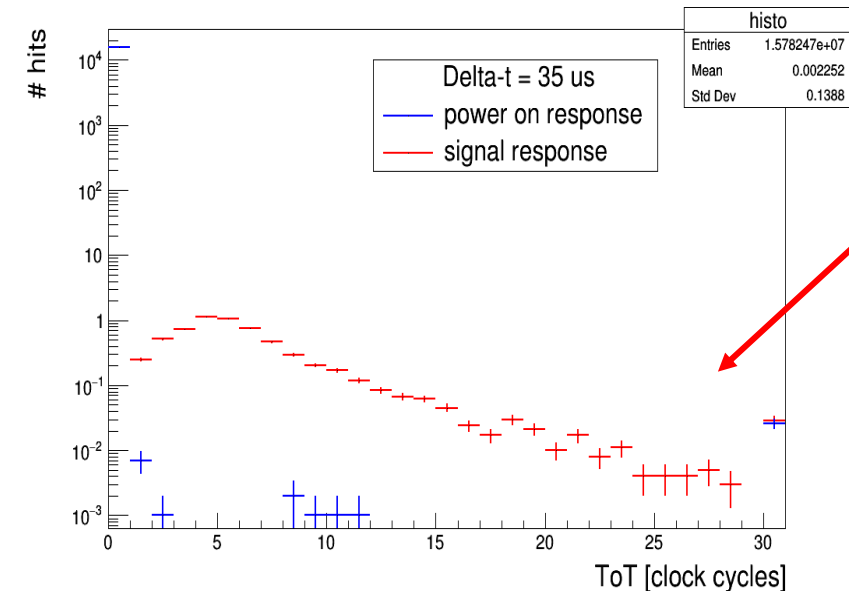
- For power on timer 40 ns the chip is quiet (ready to detect a particle) after $\sim 6 \mu$ s.

Lowest power-off state

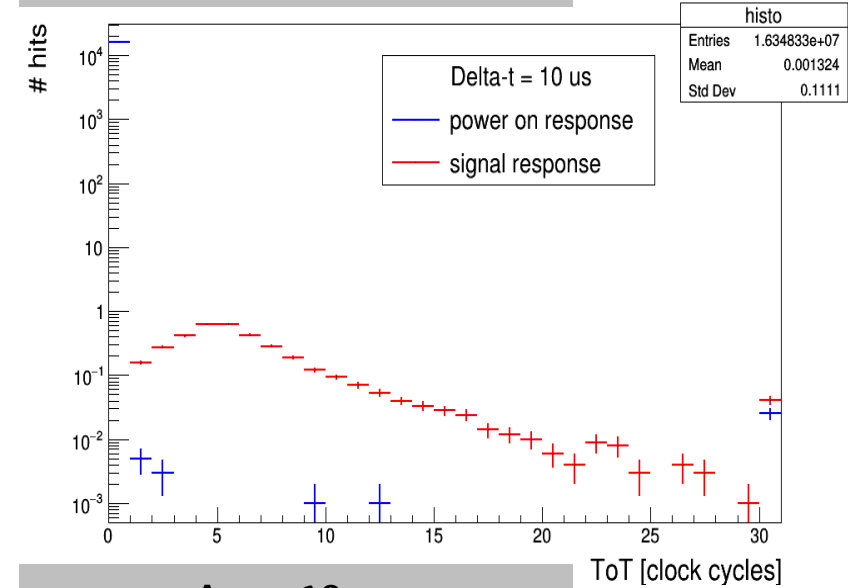
The chip is quiet after $55\ \mu\text{s}$

- It is still possible to distinguish between signal and power on response when we are at low Δt .
- However, this is not feasible from data taking point of view (will increase our amount of data)

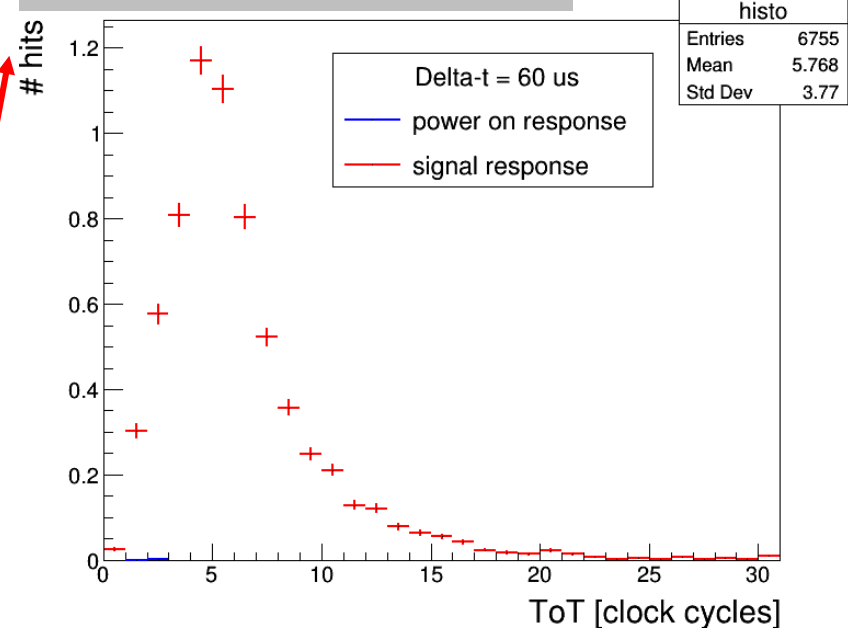
$\Delta t = 35\ \mu\text{s}$
(within power on response)



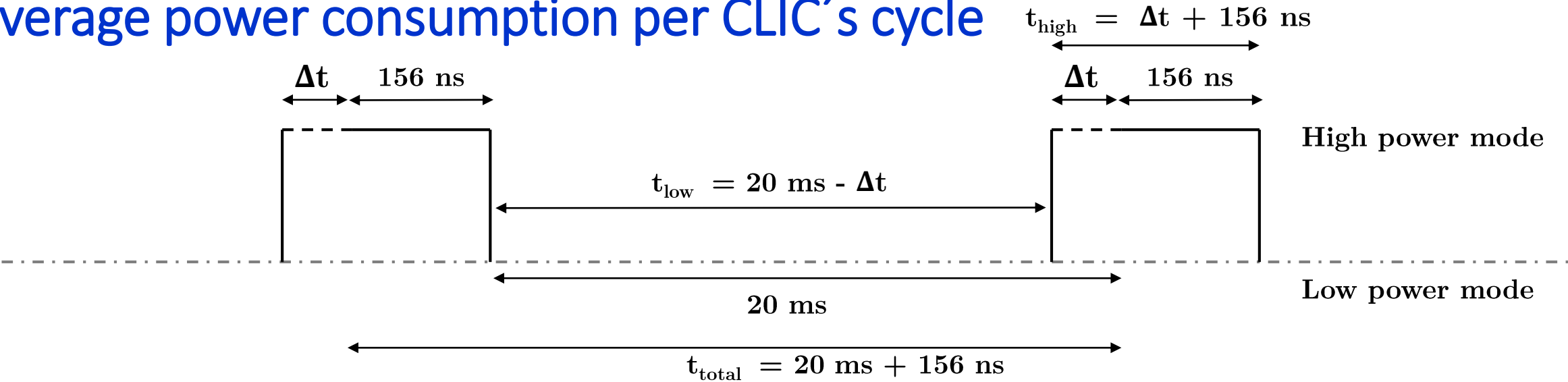
$\Delta t = 10\ \mu\text{s}$
(within power on response)



$\Delta t = 60\ \mu\text{s}$
(out of power on response)



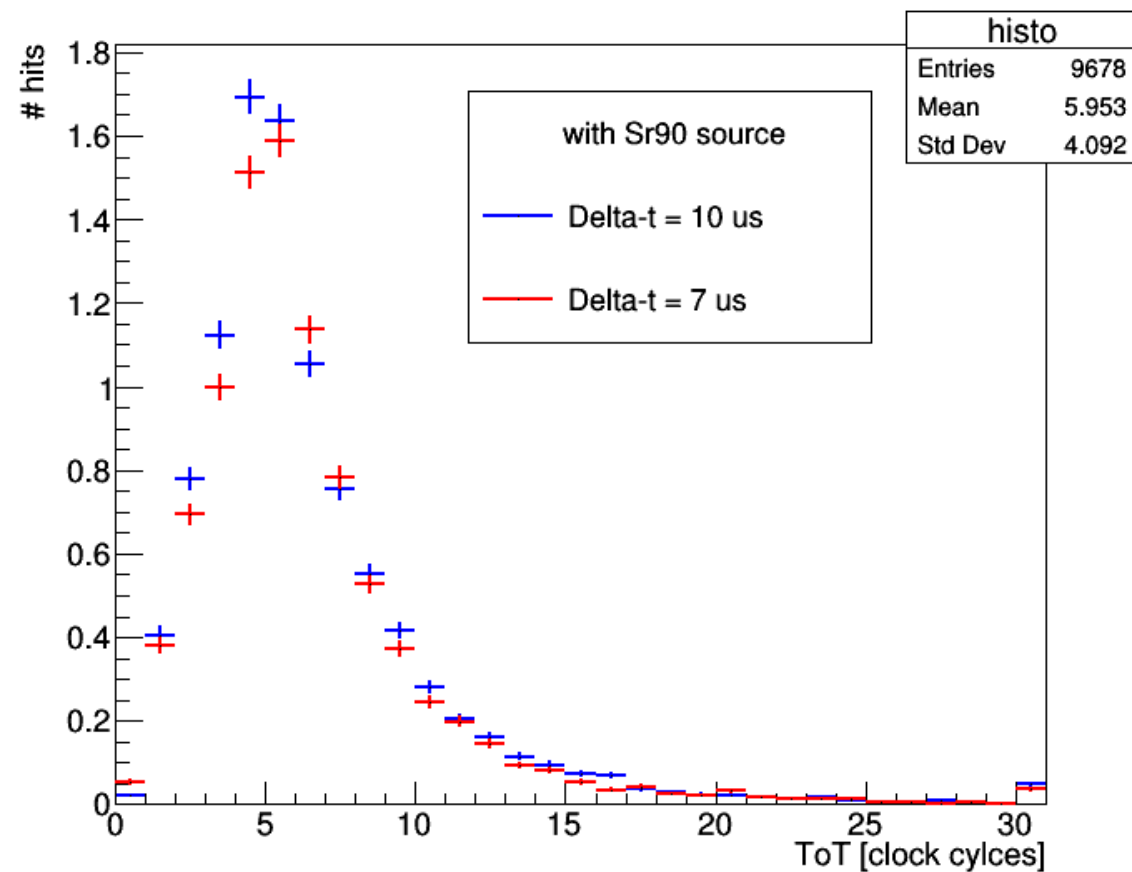
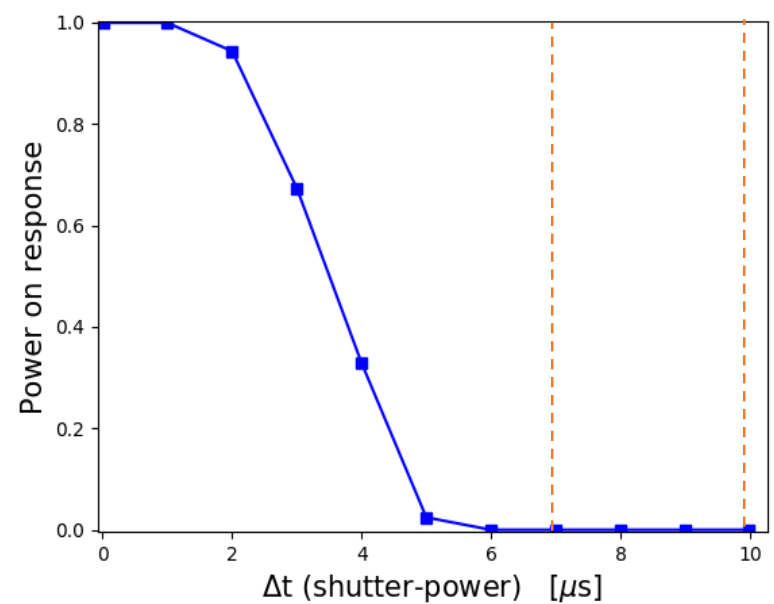
Average power consumption per CLIC's cycle



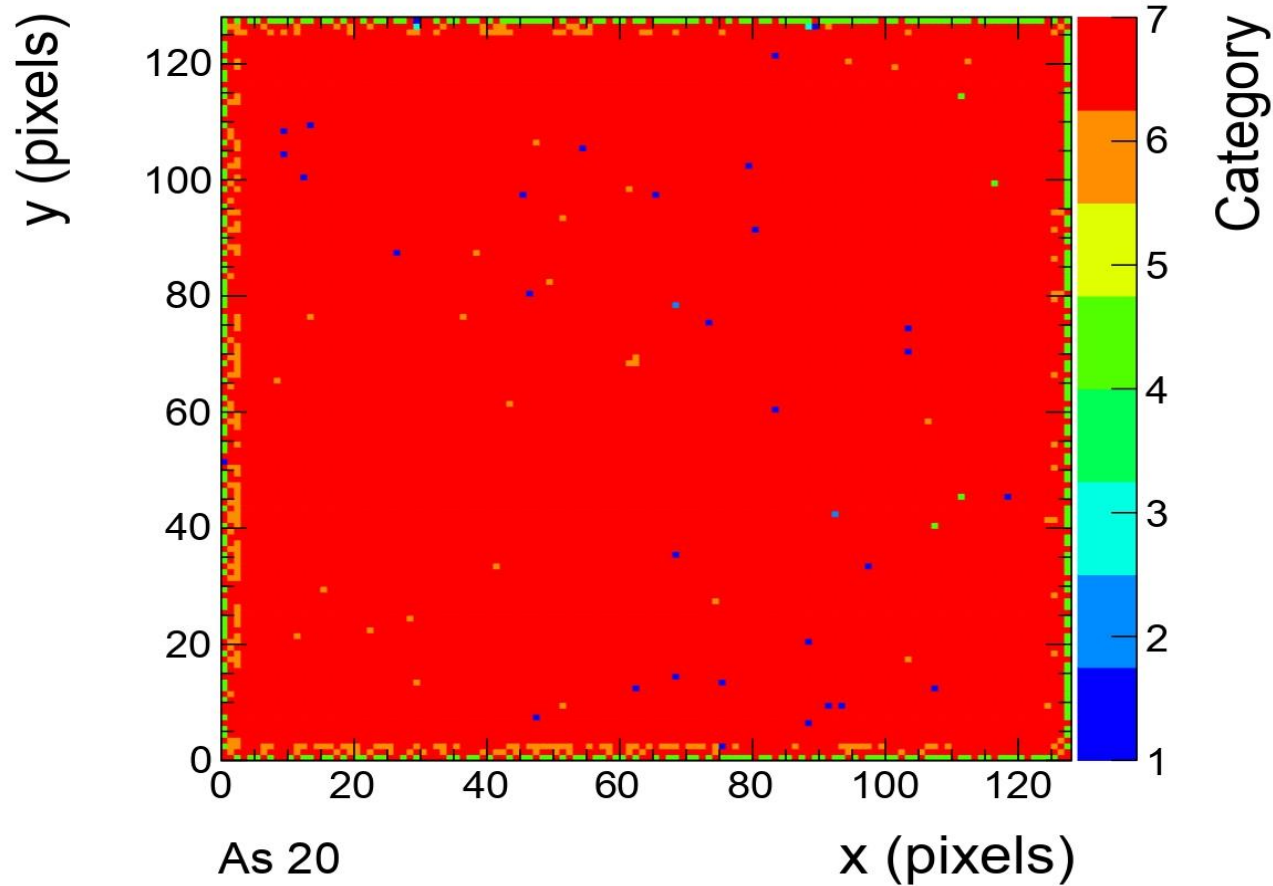
$w_{high} = \frac{t_{high}}{t_{total}}$ $;$ $w_{low} = \frac{t_{low}}{t_{total}}$ $;$ $P_{aver/cycle} = w_{low} \cdot P_{low} + w_{high} \cdot P_{high}$ $;$ $P_{high} = 0.1008\text{ W}$

Power-off state	Δt [μ s]	P_{low} [mW/ cm ²]	W_{high}	W_{low}	$P_{aver/CLIC's\ cycle}$ [mW / cm ²]
With nominal values (discN =30, discP = 50, preamp = 90)	6	193.4	0.0003	0.9997	193.4
With nominal preamp and lowest power-off state of the discriminator (discN =5, discP = 5, preamp = 90)	10	189.5	0.0005	0.9995	189.9
Lowest power-off state (discN = discP = preamp= 0)	55	187.5	0.0028	0.9972	187.7
Theoretical scenario (discN = discP = preamp = thadj_DAC = ikrum = preamp_casc = thadj_casc =0)	55	11.7	0.0028	0.9972	22.5

$\Delta t = 7$ and $10\ \mu\text{s}$
(out of power on response)



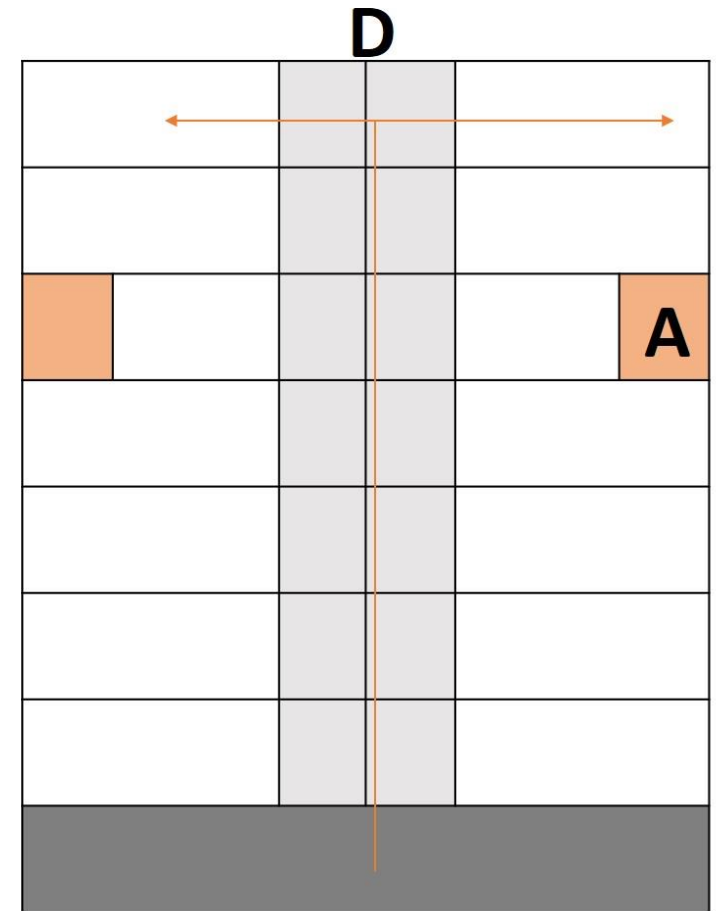
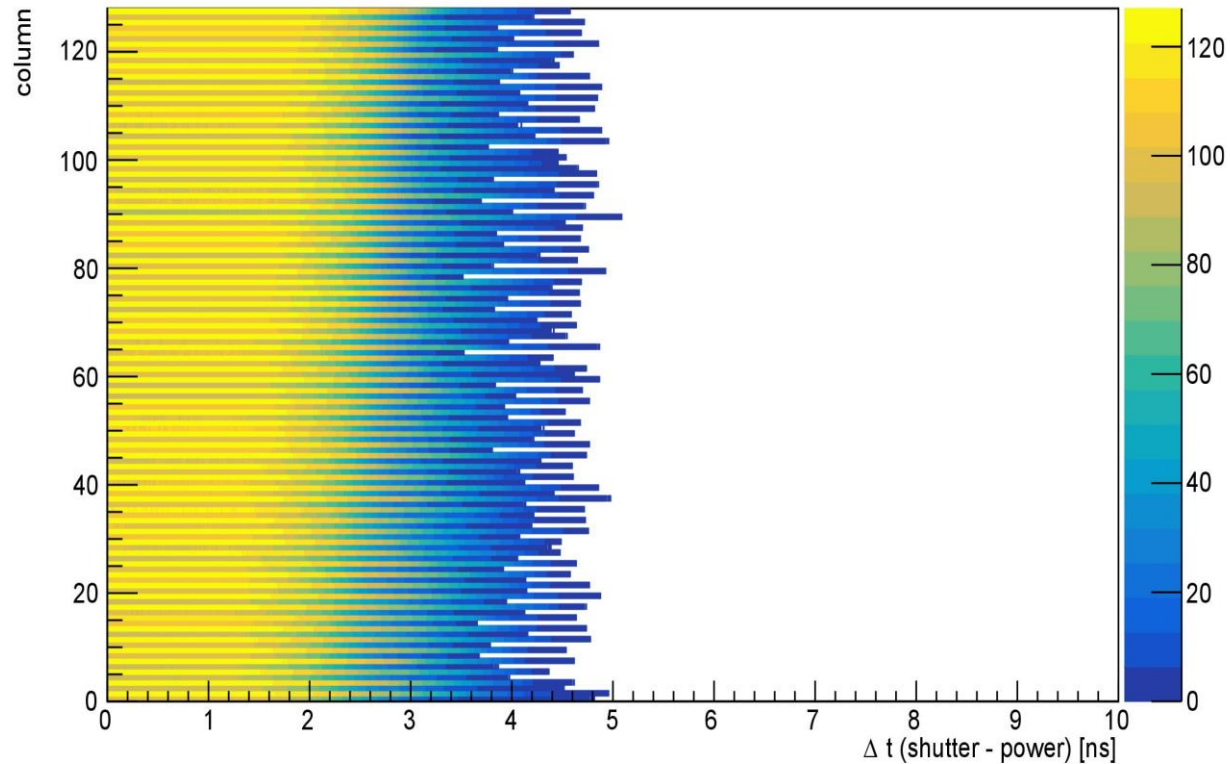
Assembly tested:



1. Masked
2. Dead
3. Shorted
4. Bonding or sensor issue
5. Weakly responding
6. Strongly responding
7. Normally responding

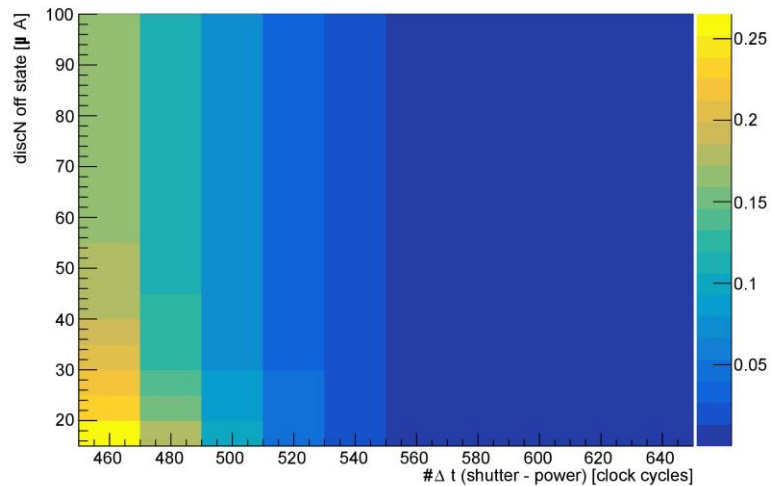
Morag Williams studies

Odd-even pattern:

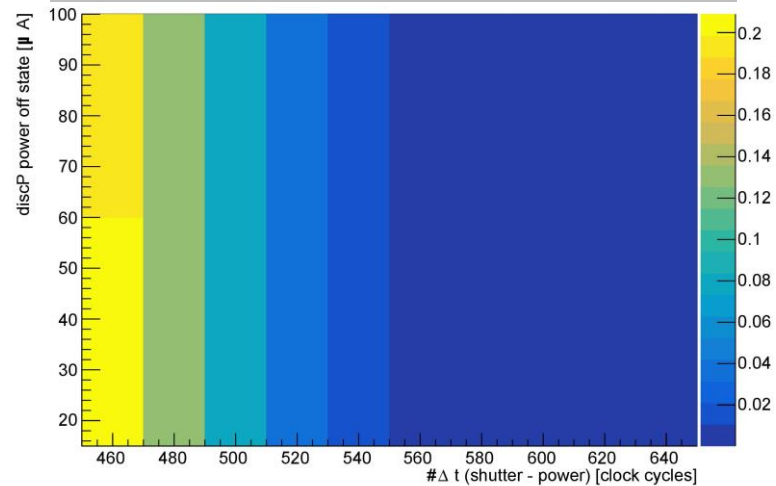


- Columns are powered externally, and the same wire is shared in a double-column.

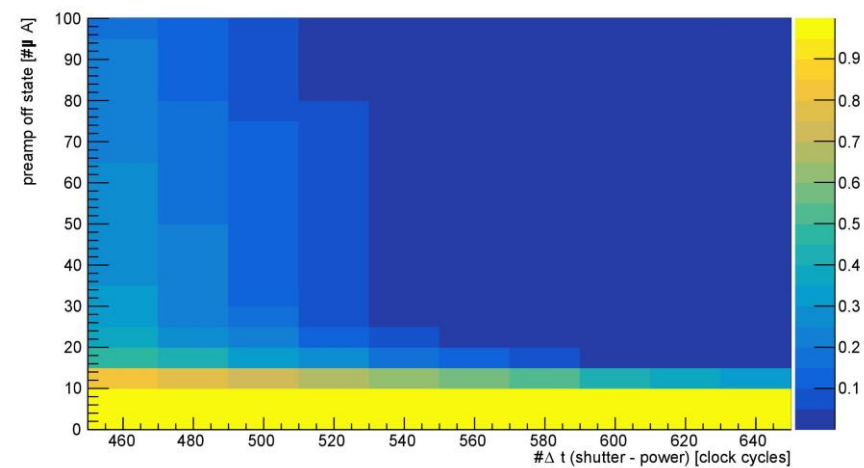
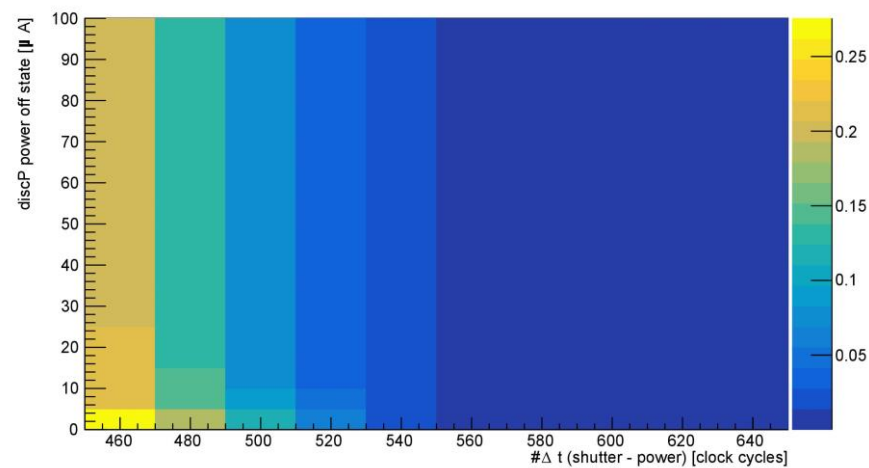
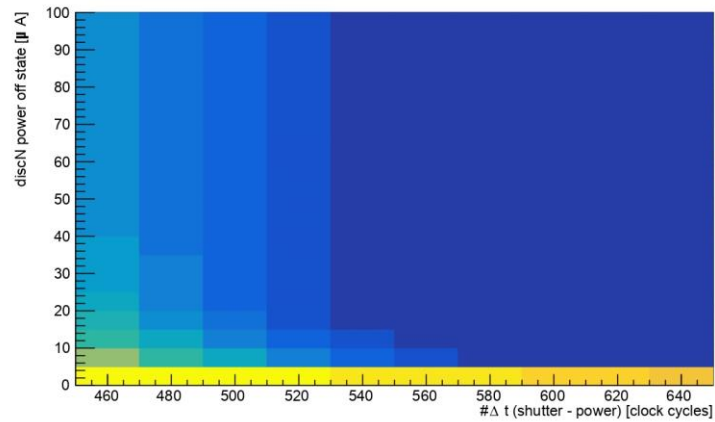
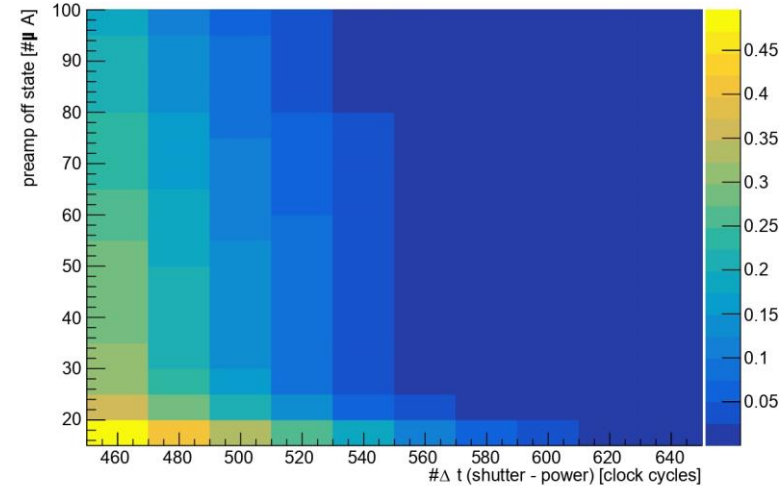
discP = 50 preamp = 90



discN = 30 preamp = 50



discN = 30 discP = 90



Nominal values DACs:

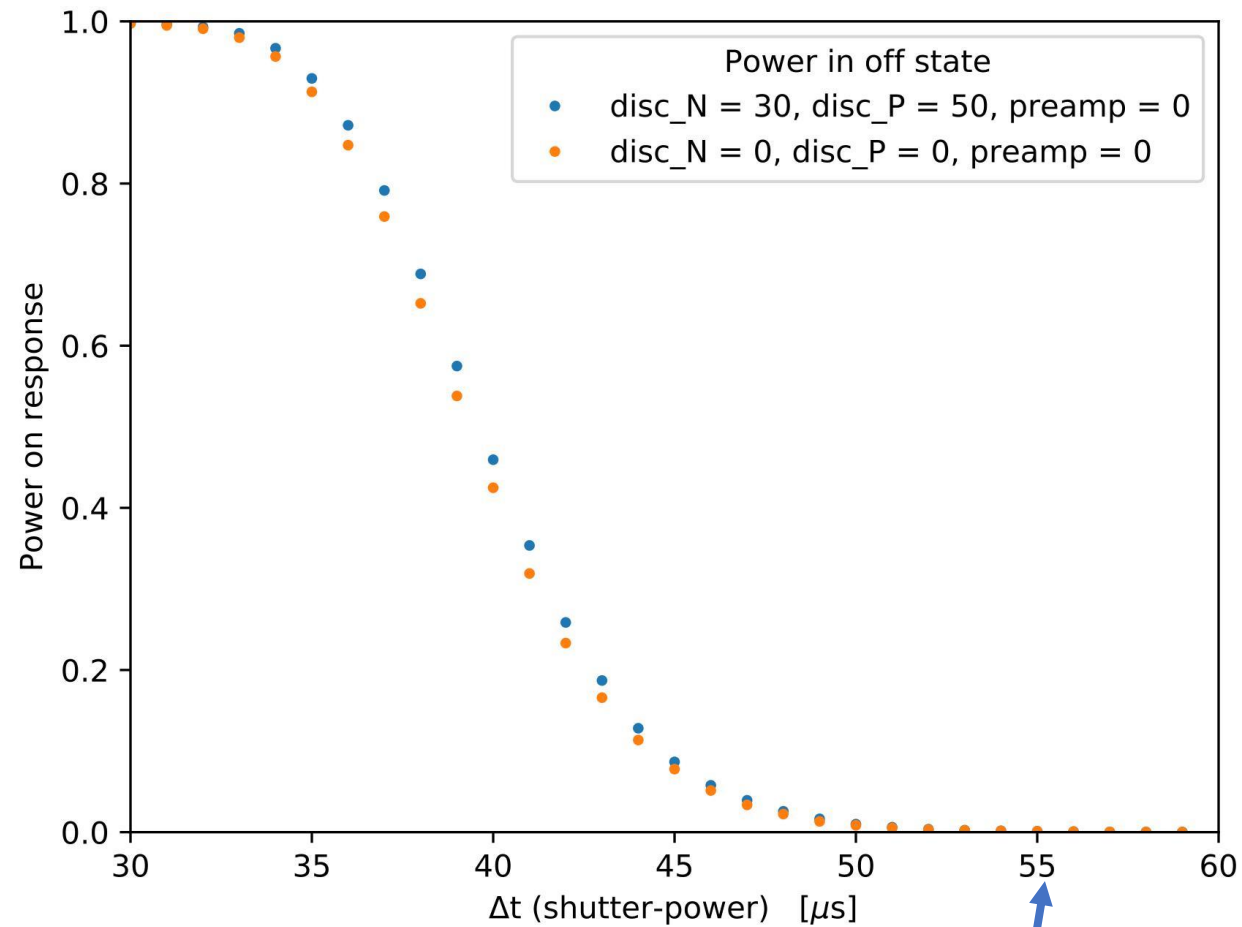
Table 1: Analogue pixel front-end DACs summary.

	Resolution	Range	Nominal current per pixel	Default code $(\cdot)_{10}$
bias_disc_N_OFF	0.5 nA	0 - 127.5 nA	15 nA	30
bias_disc_P_OFF	0.5 nA	0 - 127.5 nA	25 nA	50
bias_preamp_OFF	0.17 nA	0 - 42.5 nA	15 nA	90

Table 2: Analogue pixel front-end DACs summary.

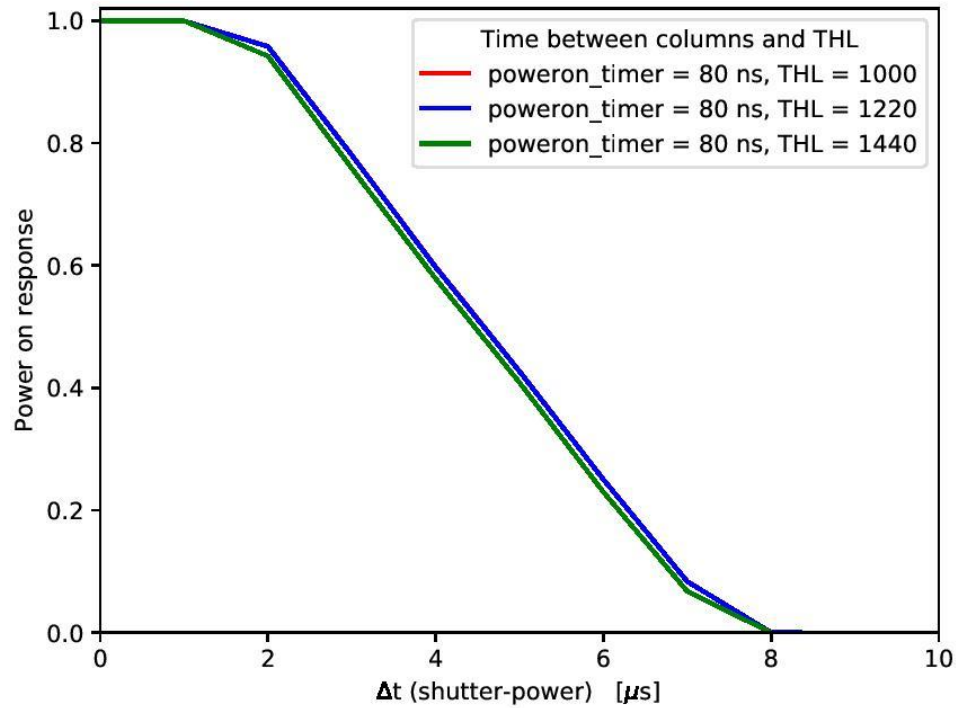
	Resolution	Range	Nominal	Default code $(\cdot)_{10}$
bias_thadj_DAC	0.78 nA	0 - 200 nA	50 nA	64
ikrum	0.1 nA	0 - 25.5 nA	8 nA	80
bias_preamp_casc	4.5 mV	0.05 - 1.2 V	601.5 mV	133
bias_thadj_casc	4.5 mV	0.05 - 1.2 V	601.5 mV	133

$\text{discN} = \text{discP} = \text{preamp} = 0$

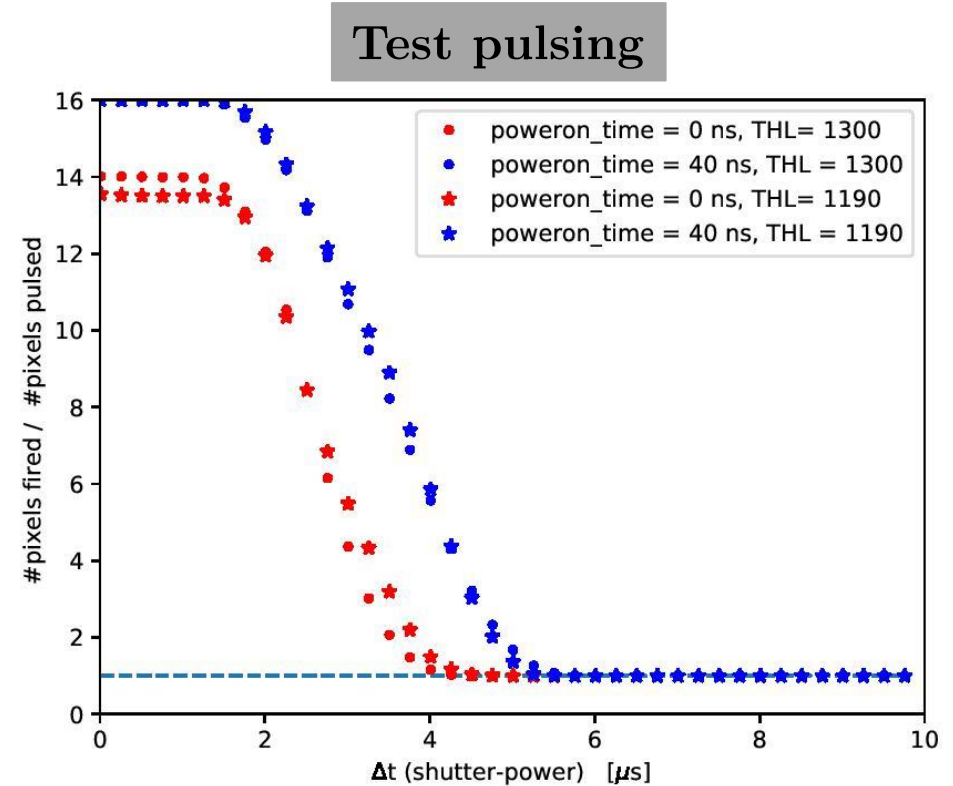


The chip is quiet after **55 μs**

Threshold scans



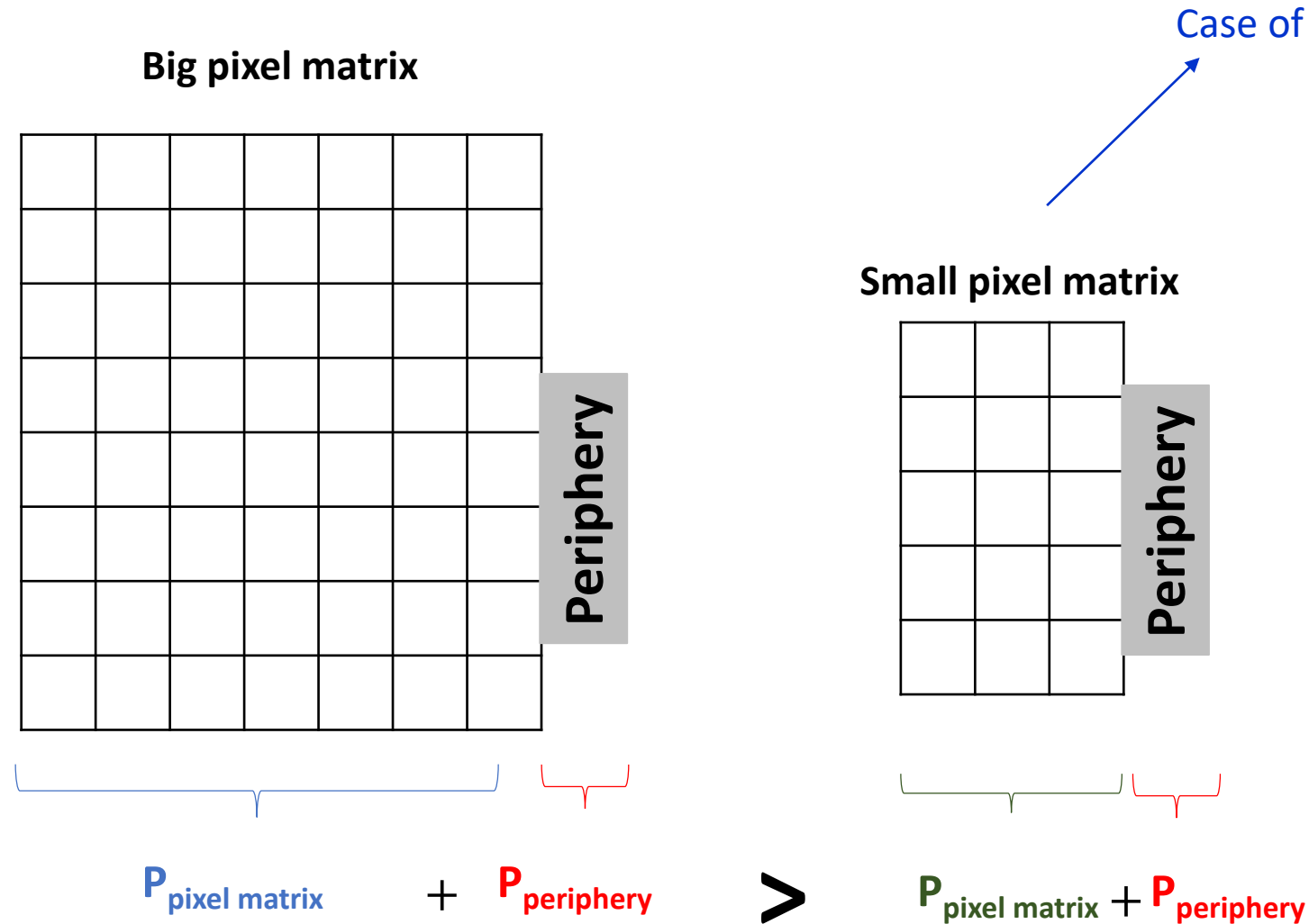
Chip: Nominal THL = 1220 DAC



Assembly: Nominal THL = 1990 DAC

- Low THL dependence.
- By increasing the THL, we do not cut in the power on response.

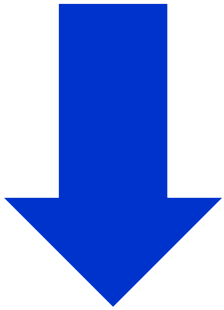
Periphery power consumption



- The size and power consumption of the periphery does not scale with the chip size.
- The power consumption of the periphery will be less significant for larger chips.

Digital power pulsing (clock gating):

Average **digital power consumption** per CLIC's cycle : 49.5 mW/cm^2



Power pulsing the clock

- In the digital part we are not multiplexing between biasing points (as with the disc and preamp).
- The clock is gated (“stopped”) in the part of the circuitry when it is not used