Improving timing and spatial resolution for CMOS sensors with a small collection electrode

M. Munker, T. Kugathasan, W. Snoeys

CLICdp Collaboration meeting
28.08.2019

Outline

- Introduction of technology & challenges
- Optimisation to overcome challenges
- Summary & outlook

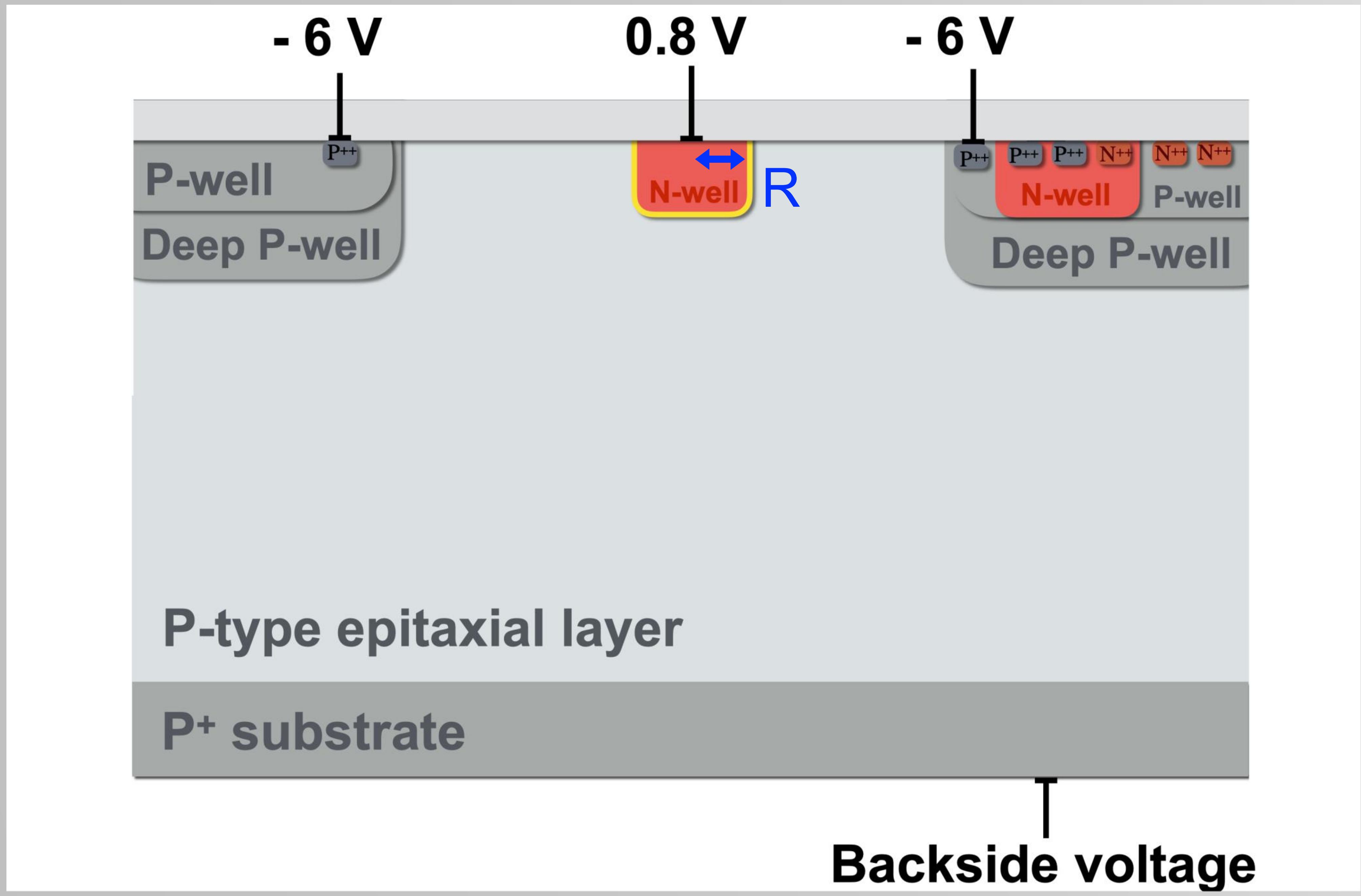
Introduction of technology & challenges

Small collection electrode CMOS - advantages

Monolithic CMOS:

- Standard CMOS technology —> low costs
- No interconnects between readout chip & sensor —> facilitate large scale production effort

Monolithic CMOS sensors with a small collection electrode:



Circuitry placed in shielding p-wells separated from collection electrode:

—> Minimise **radius R** of collection electrode

—> Minimise sensor **capacitance C ∝ R**

—> Maximise readout **charge Q = I/C, I = induced current**

—> Maximise **signal/noise**

—> Minimise **threshold** (below 100 electrons)

—> Minimise **analogue power P ∝ $(C/S)^4$**

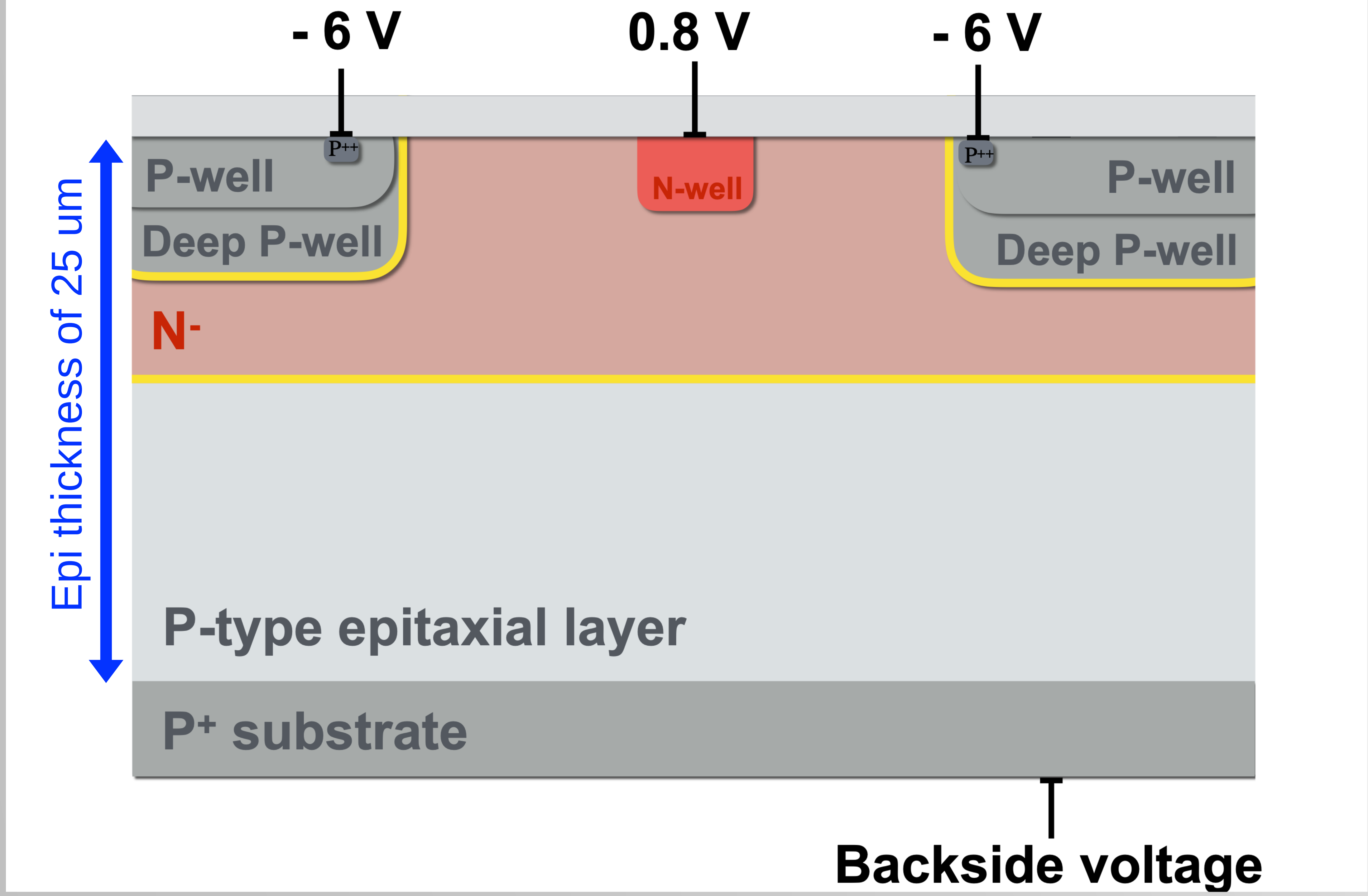
↳ Combine advantages of monolithic CMOS with advantages of small collection electrode.

Small collection electrode CMOS sensors - challenges

Challenge = electric field:

- Placement of circuitry in sensor (p-wells) alters the electric field
- Difficult to reach high field over full pixel area with very small collection electrode
- Especially relevant since bias on p-wells is connected to backside and limited by what circuitry can tolerate (< 6 V)

Modified process / baseline design for optimisation:



To reach higher field:

- **High resistivity** epitaxial layer
- Process modifications —> **deep planar n-implant**

W. Snoeys et al.: https://doi.org/10.1016/j.nima.2017.07.046

—> Deep planar junction results in **full depletion**

—> Isolation of circuitry in p-wells from backside substrate

—> **Higher bias on substrate** possible

* Epi thickness fixed to 25 um for following talk

How do the p-wells alter the field? - the electric field minimum

Origin of electric field minimum:

- Placement of p-wells with circuitry at pixel border

—> **Two bias terminals** on front & backside of sensor

—> Between both, **maximum potential** crossed

—> Local point of **zero electric field**

—> Electric field streamlines (and as such collected charge)

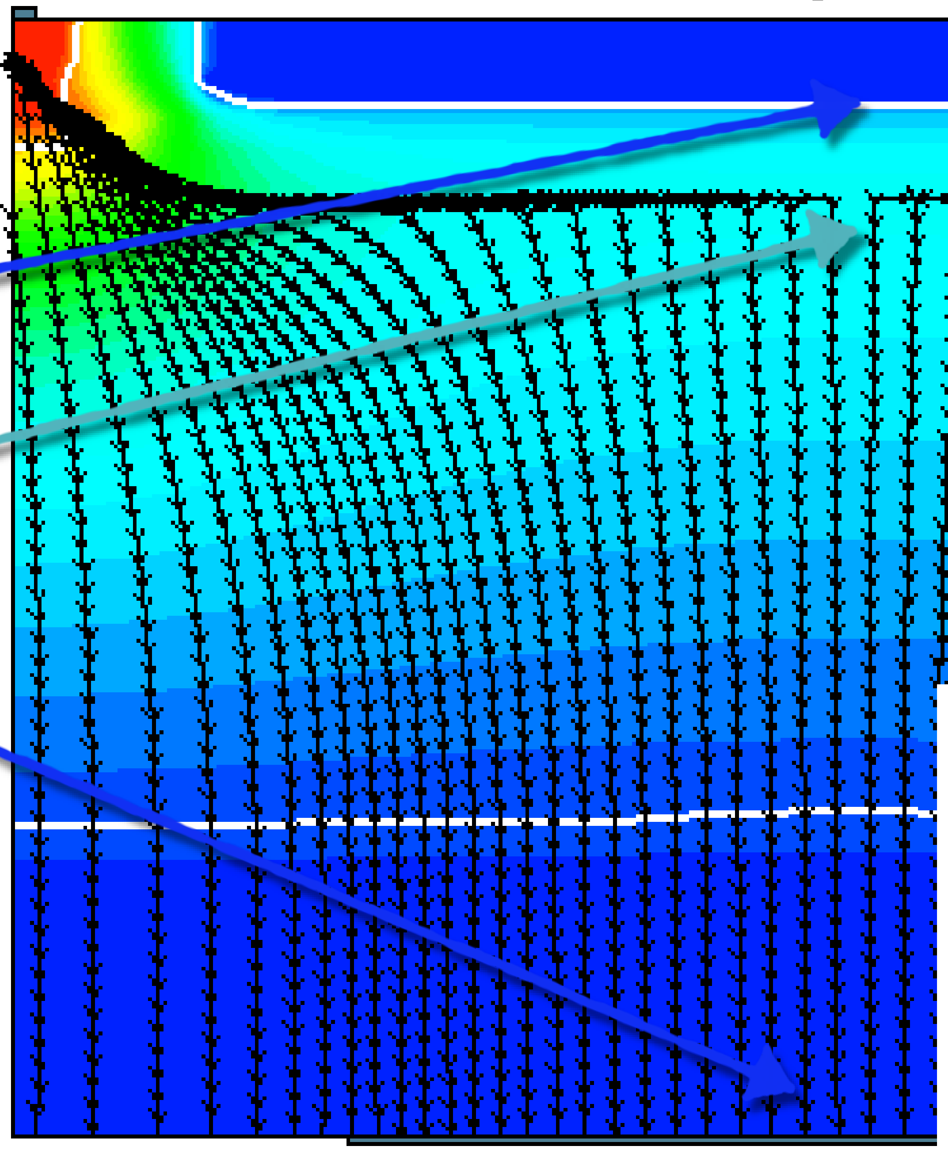
go first through minimum before they are bend towards

collection electrode

—> Significantly longer drift path

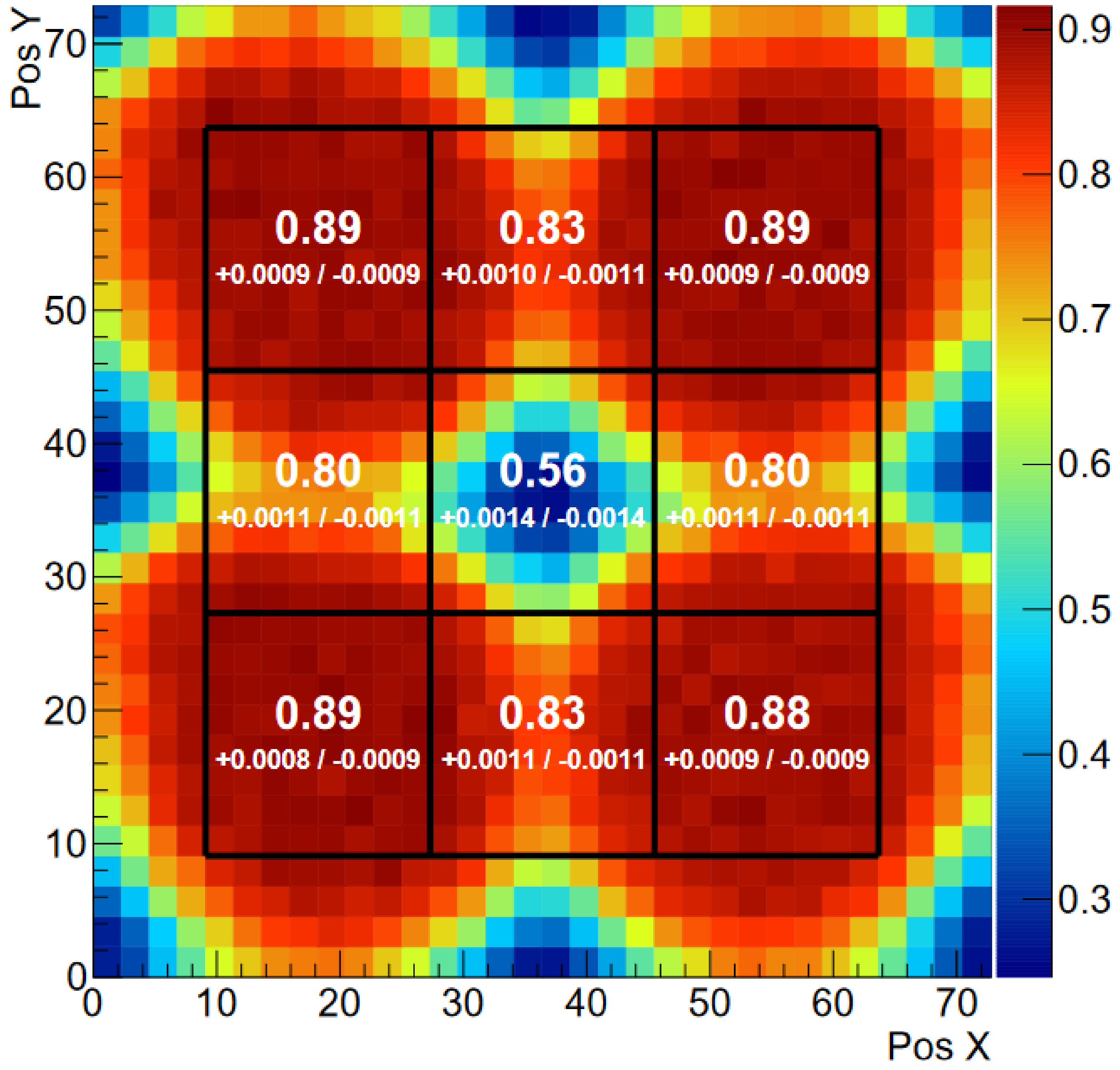
—> Less precise timing & charge loss after irradiation

Pixel size of 36.4 um, potential & streamlines:



Modified process, bias of -6 V

Pixel size of 36.4 um, efficiency in pixel cell:



Measured charge loss in pixel corners of Mini-Malta after irradiation with dose of $1e^{15}$ neq/cm^2:

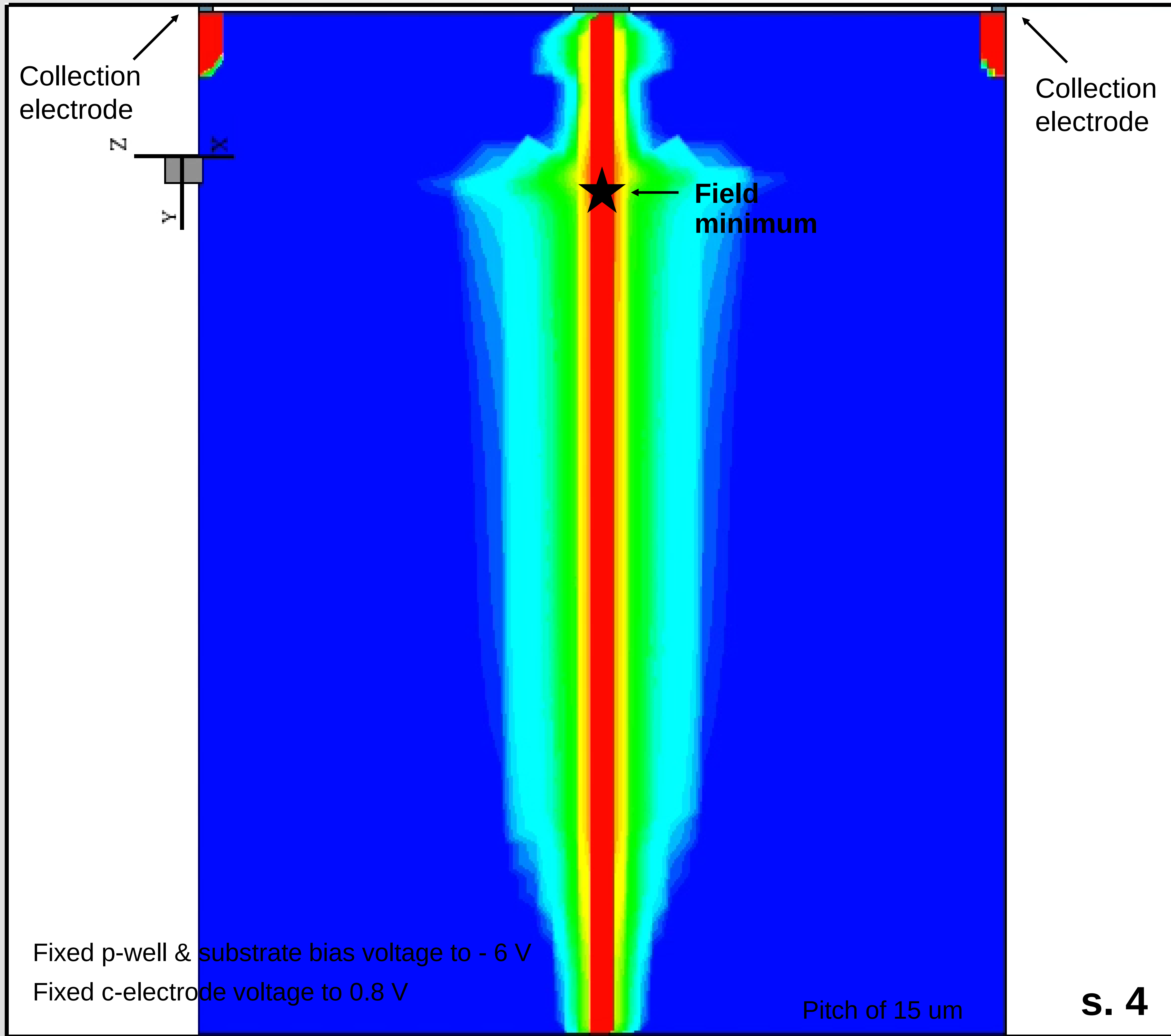
https://doi.org/10.1088/1748-0221/13/01/C01023

Main challenges & differences with standard planar sensors

Signal charge density after particle incidence at pixel border (100 ps steps):

- **<u>Electric field minimum</u>**:

—> Crucial for **charge collection**.



Main challenges & differences with standard planar sensors

- **<u>Electric field minimum</u>**:

—> Crucial for **charge collection.**

- <u>Evolvement of **depletion**</u>: ⟶

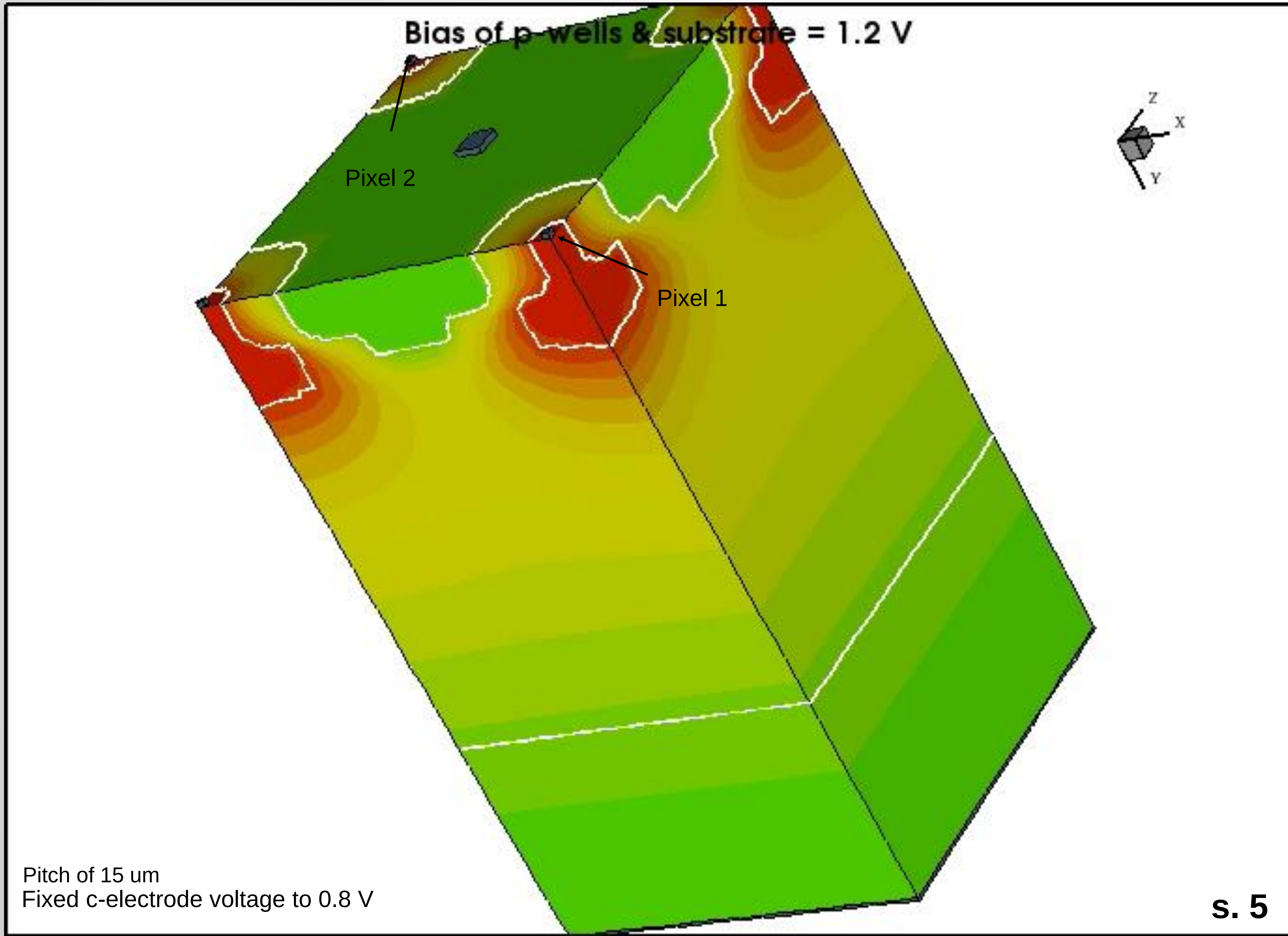
—> Crucial for **capacitance.**

Need to understand & optimise electrostatic solution

(electric field, depletion & capacitance)

Finite element 3d TCAD simulations necessary.

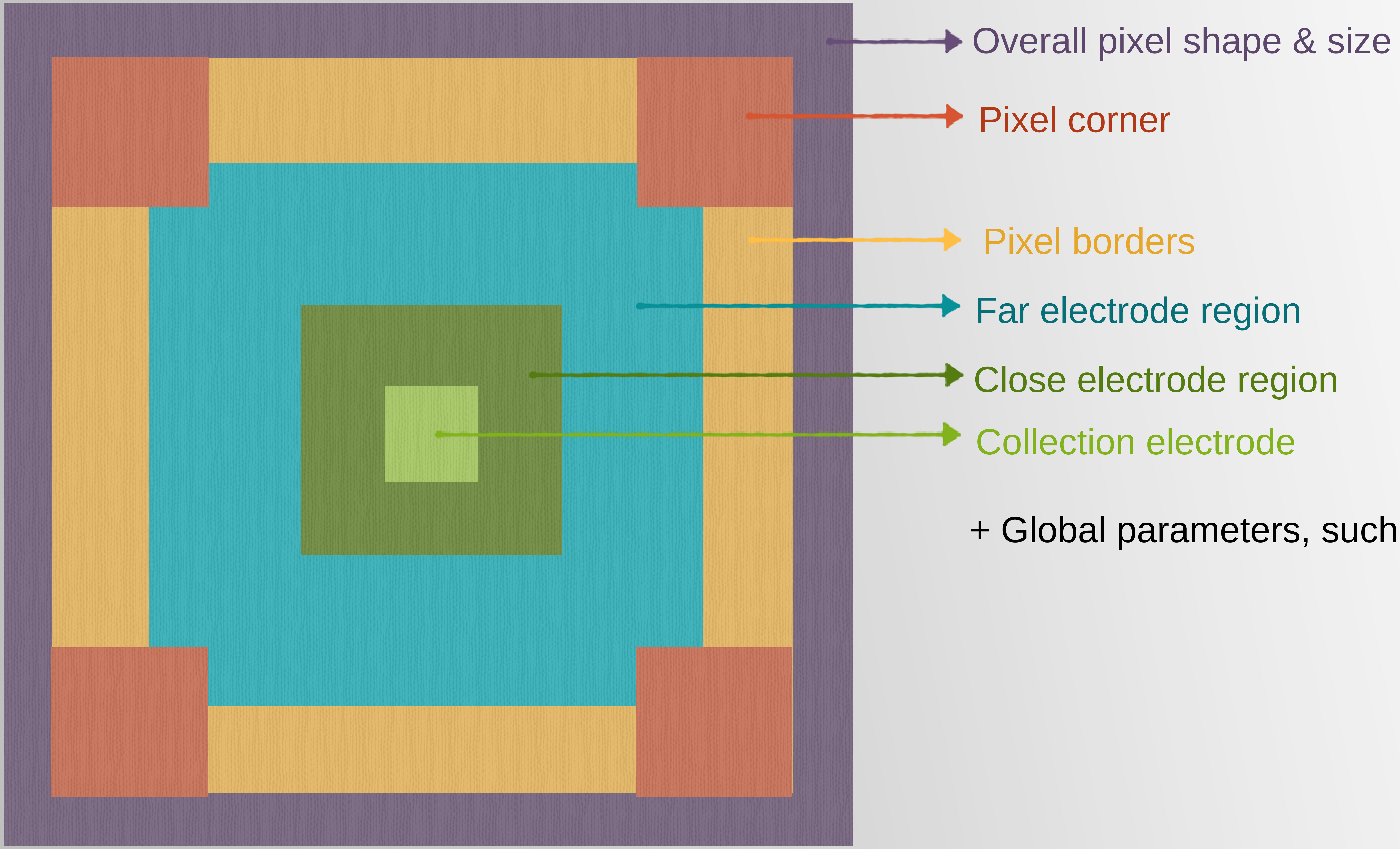
Electrostatic potential for different bias voltage on p-wellls & backside:



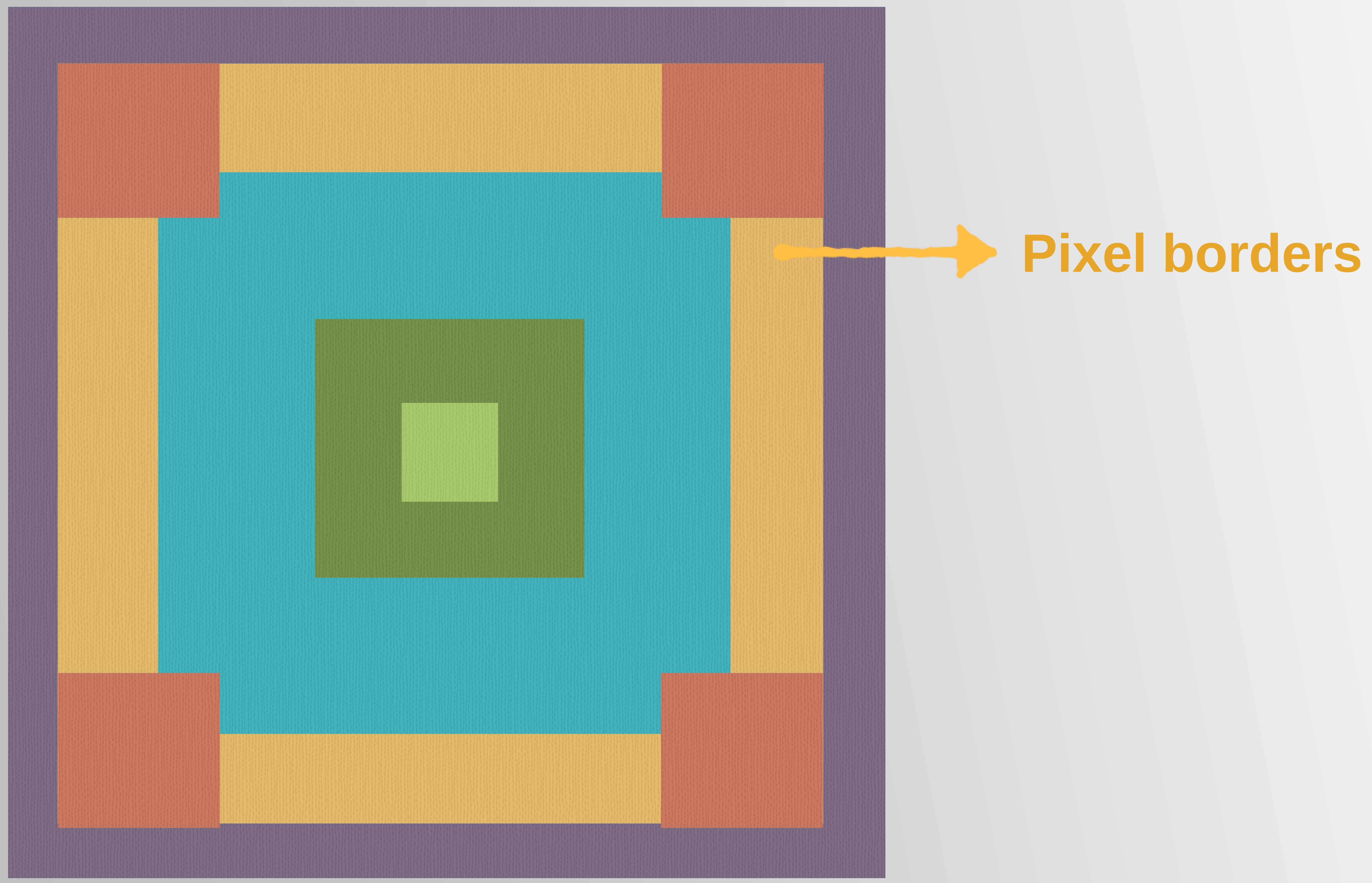
Optimisation to overcome challenges

Optimisations to overcome challenges

Schematic of top-view on pixel:

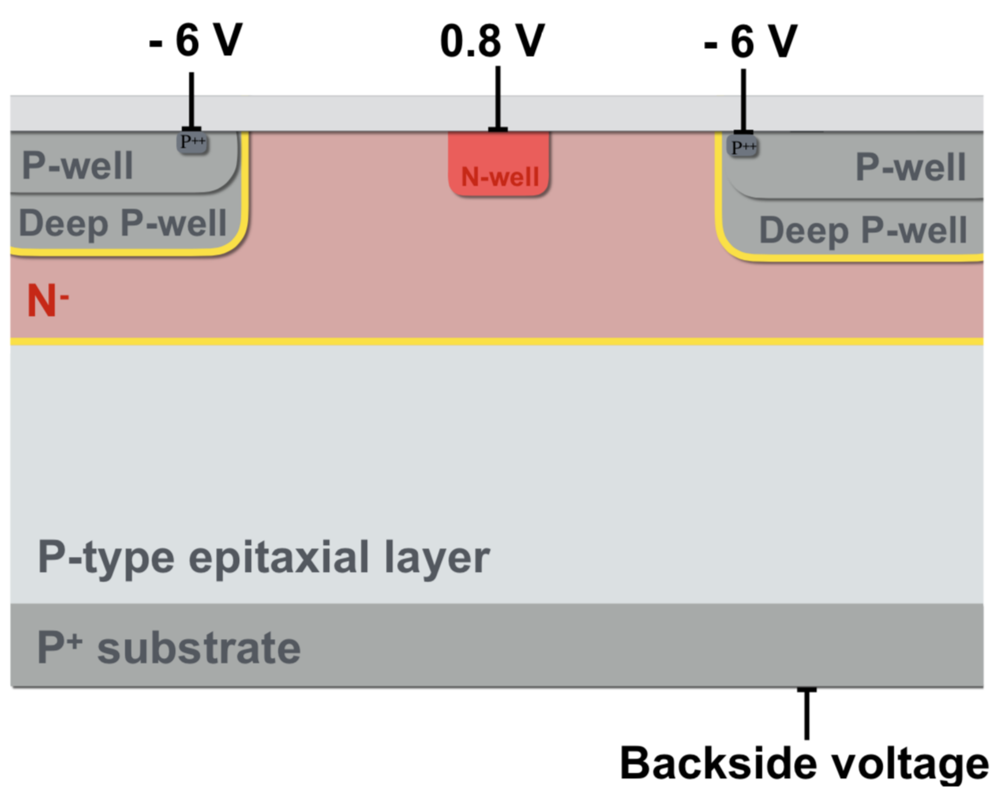


+ Global parameters, such as dose of n-layer.

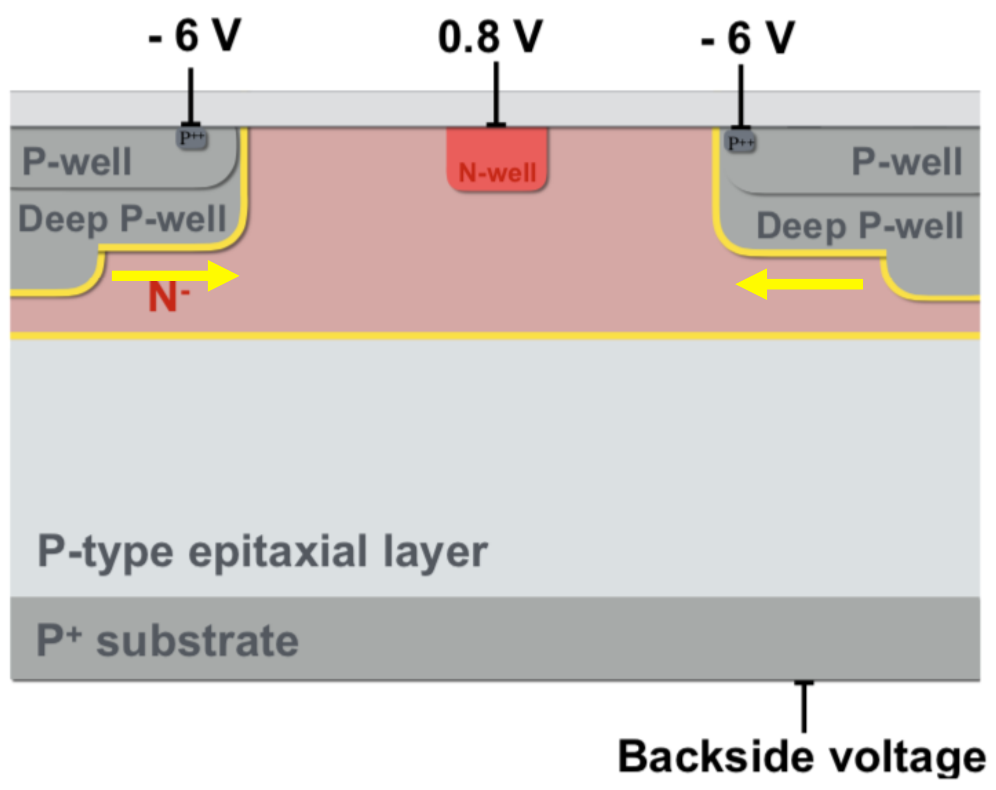

Pixel borders

Optimising the pixel borders - push charge out of minimum

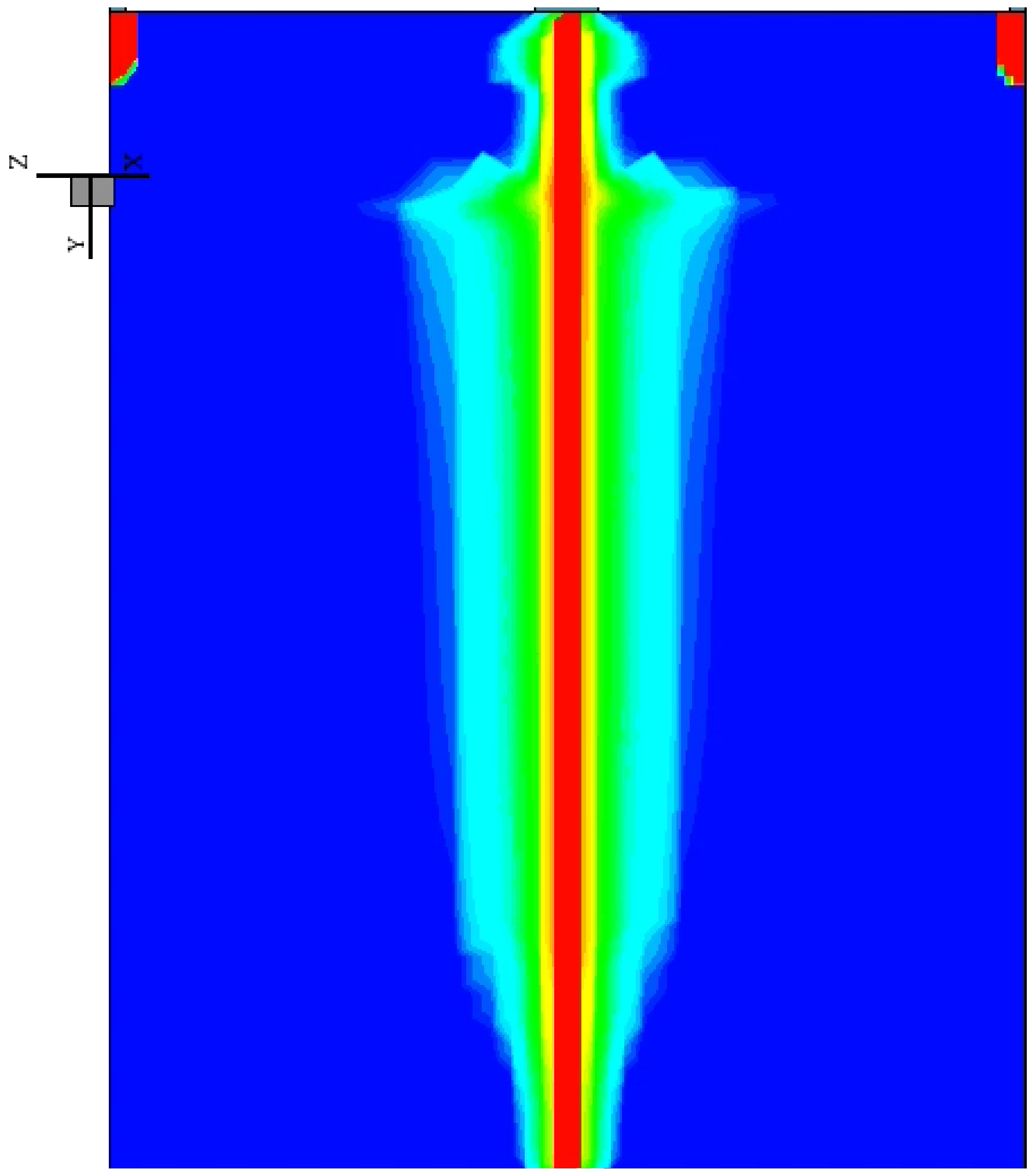
Blanked n-layer, modified process:



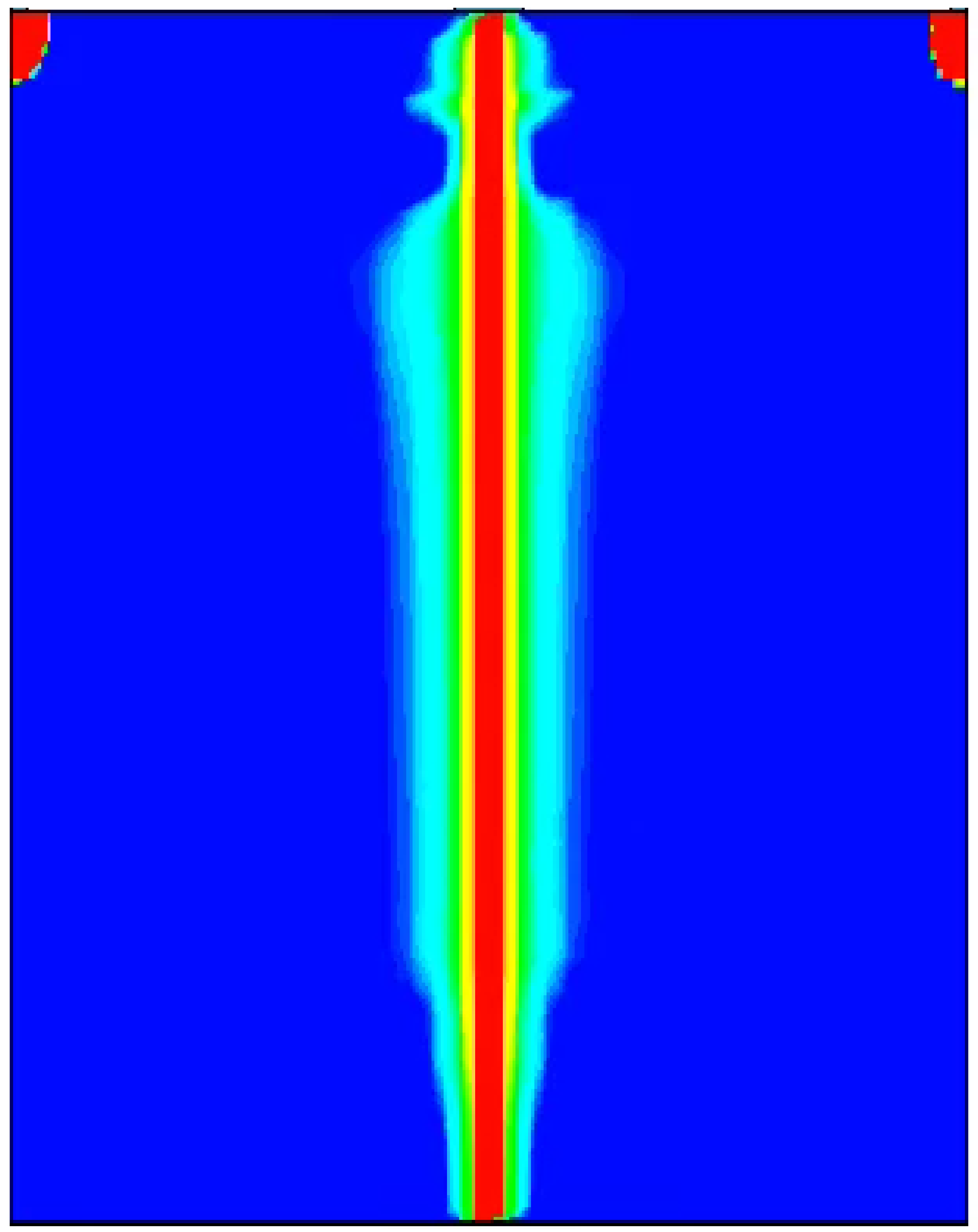
Additional p-implant:



Signal charge density after particle incidence (100 ns steps):



Signal charge density after particle incidence (100 ns steps):



Fixed p-well & substrate bias voltage to - 6 V

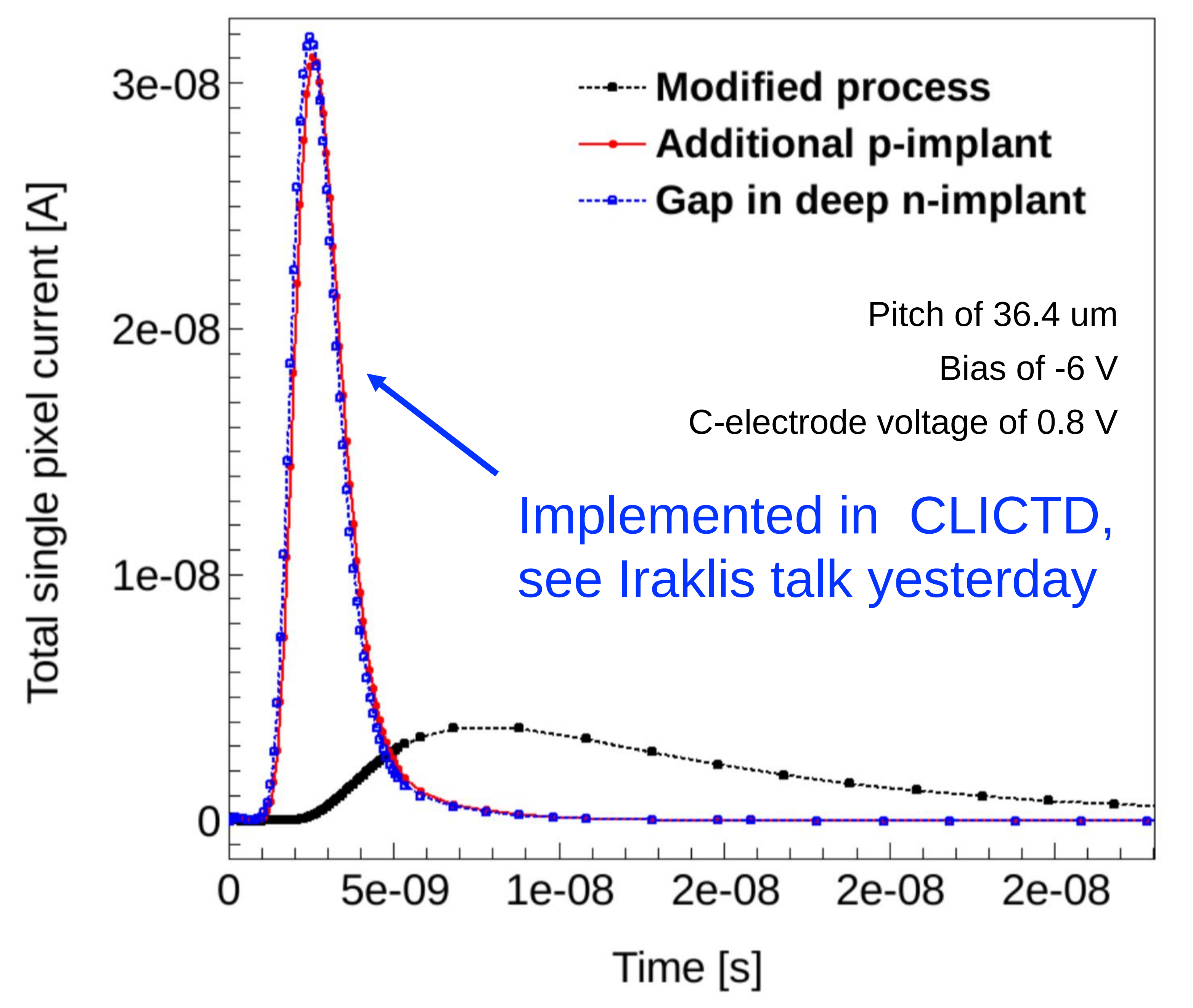
Fixed c-electrode voltage to 0.8 V

Pitch of 15 um

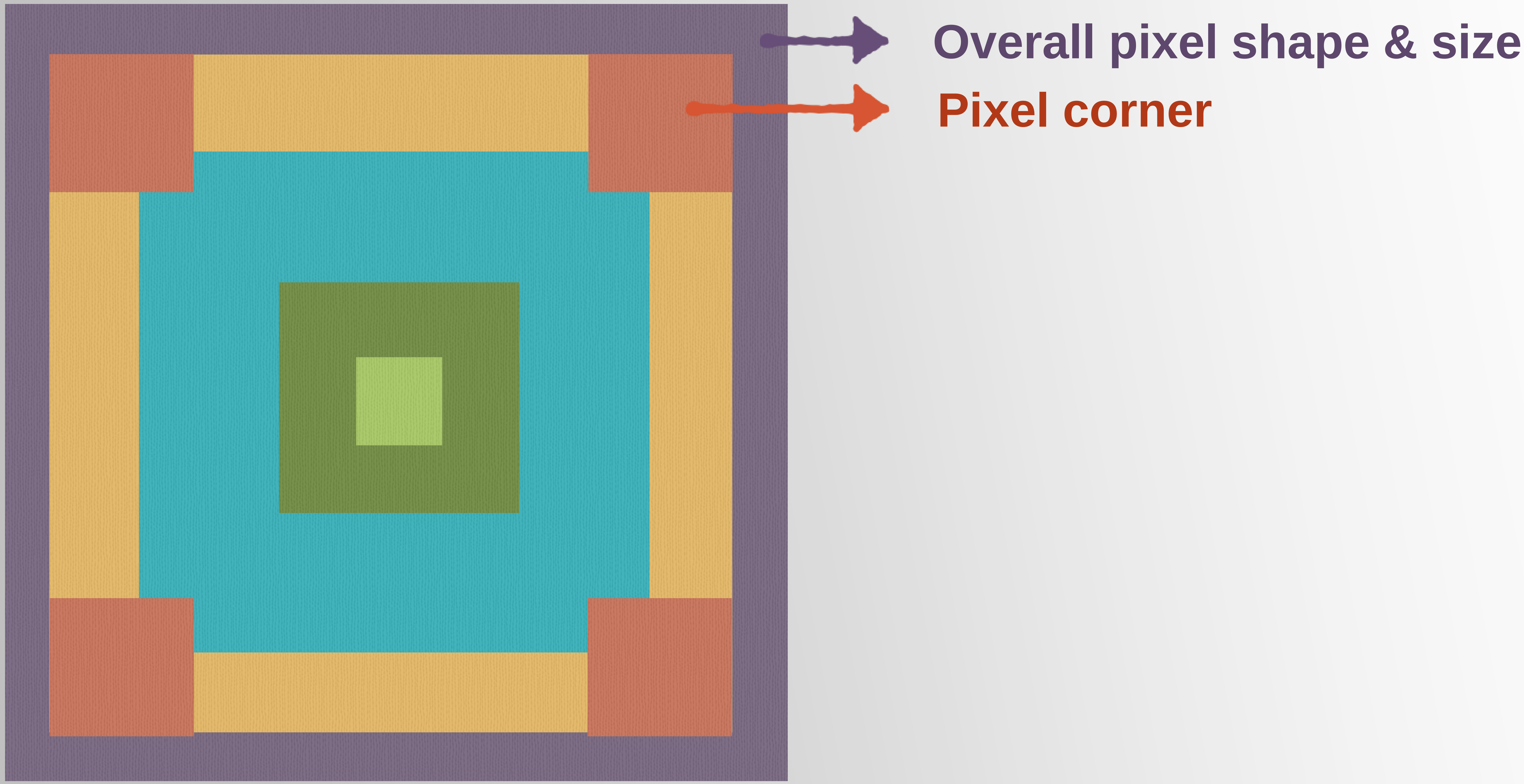
Sensor designs to push charge out of electric field minimum: M. Munker *et al* 2019 *JINST* **14** C05013

- **Additional p-implant** at pixel borders
- **Gap in n-layer** at pixel borders

—> **Lateral junction/electric field (yellow arrows)** pushes charge at pixel border towards collection electrodes



Fully efficient for pixel pitch of 36.4 um after irradiation of $1e^{15}$ neq/cm^2 —> proof of principle.


Overall pixel shape & size
Pixel corner

Optimising the overall pixel shape - hexagonal pixels

Why hexagonal pixels, especially for this technology?:

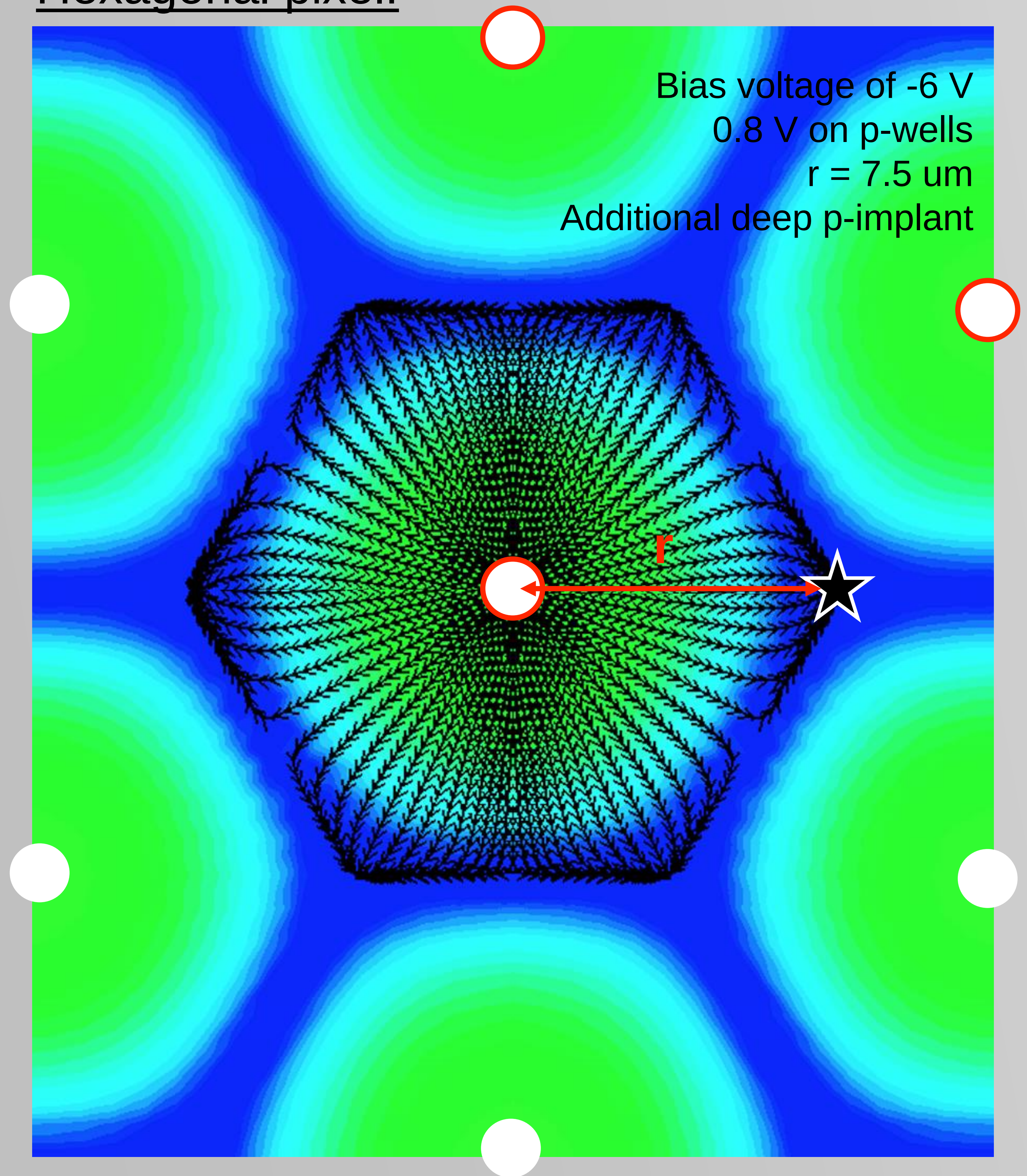
Keep pixel & circuitry area constant while further reducing the distance between the collection electrodes

1. Reduce low field edge regions
2. Reduce number of closest neighbours —> reduce charge sharing —> improved signal/noise in seed pixel

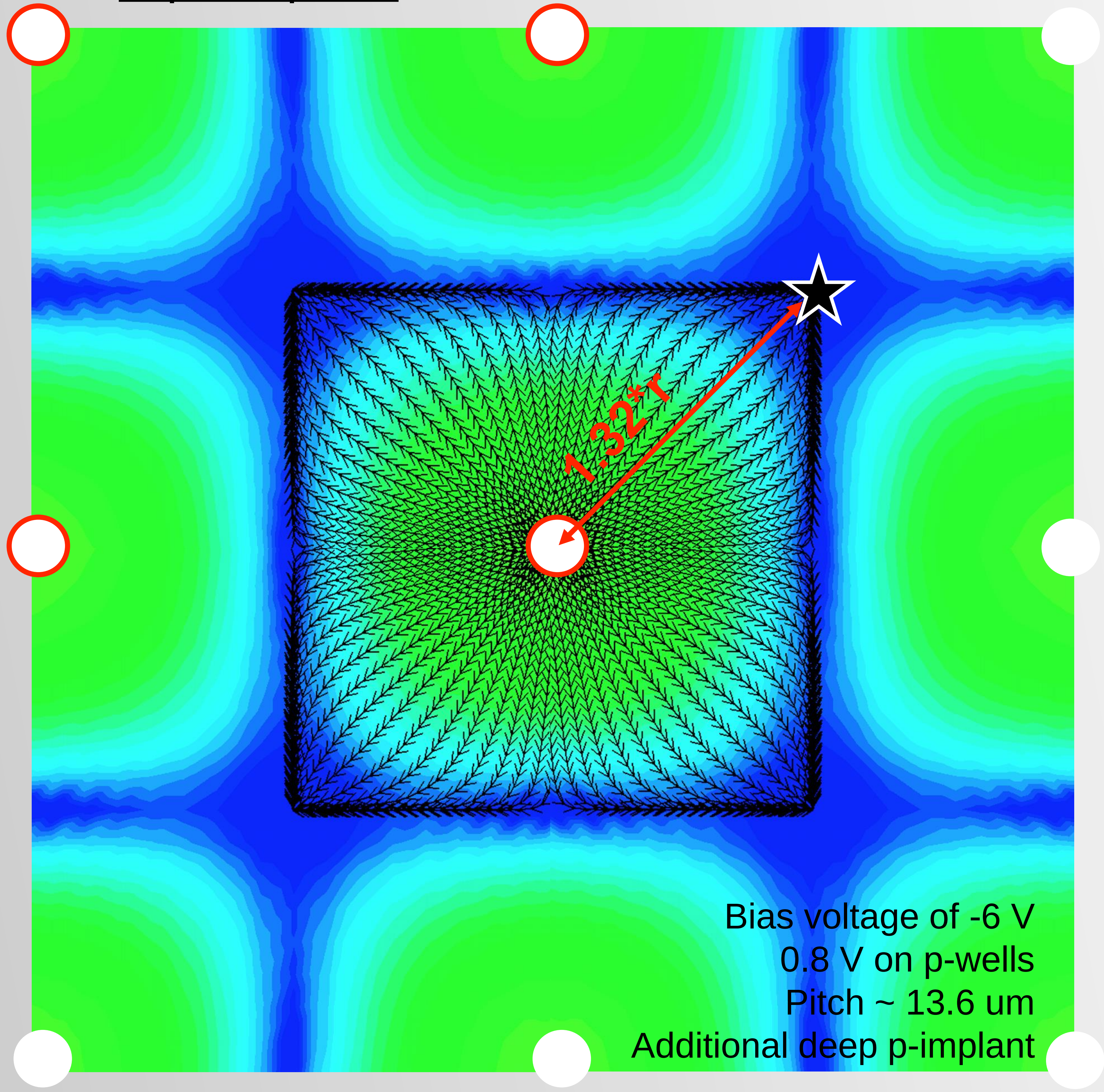
—> **Improve timing**

Absolute value & streamlines of electric field:

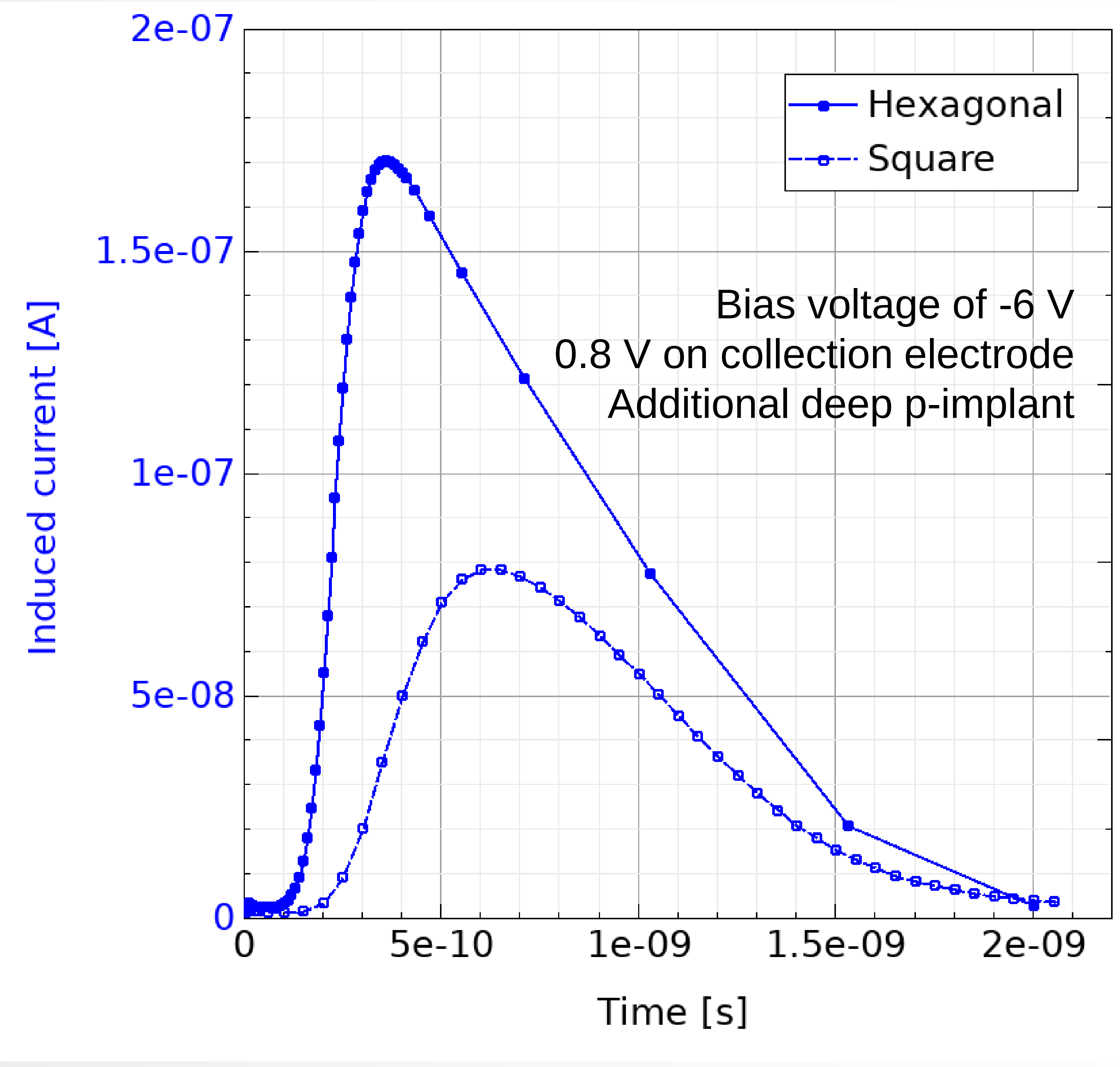
Hexagonal pixel:

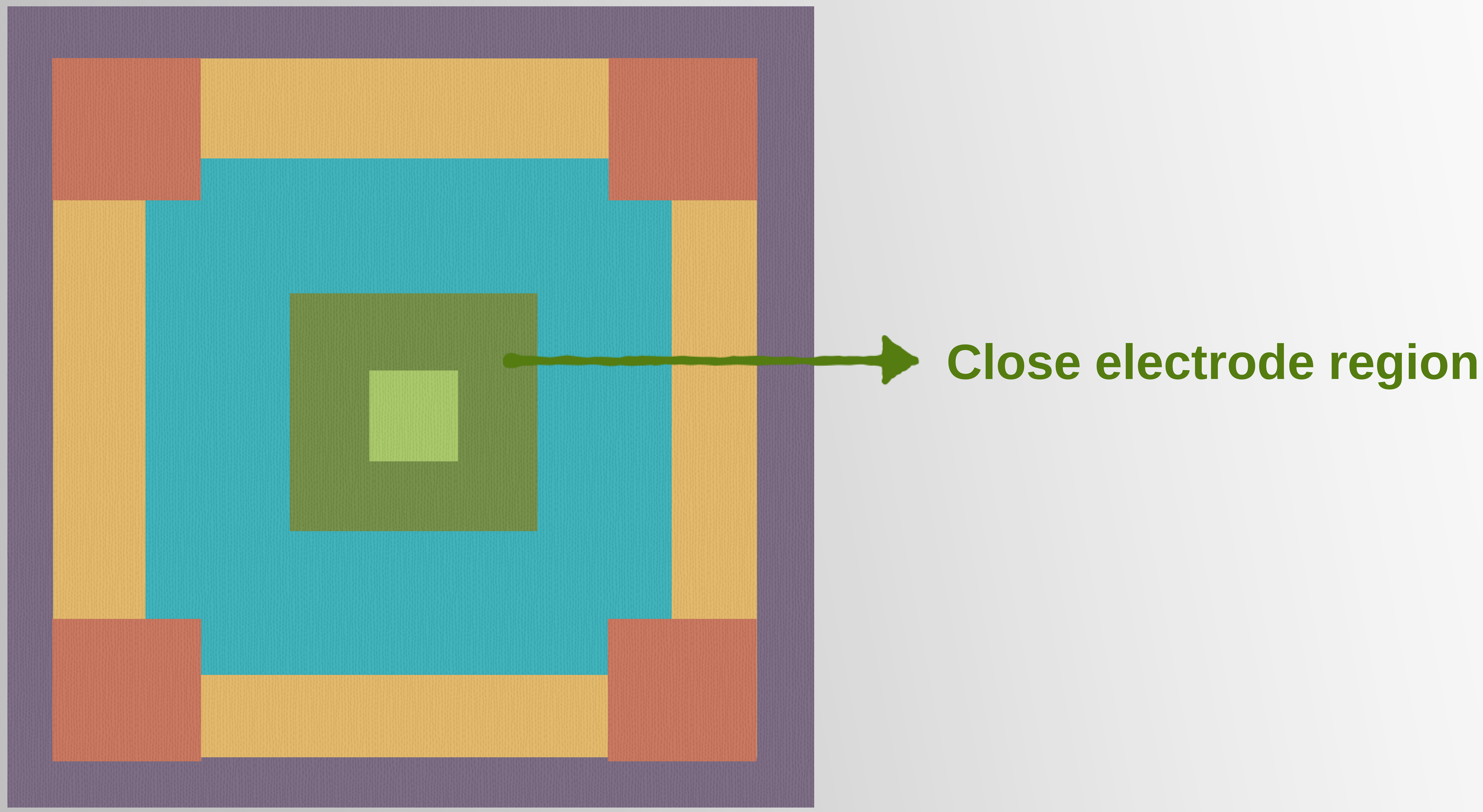


Square pixel:



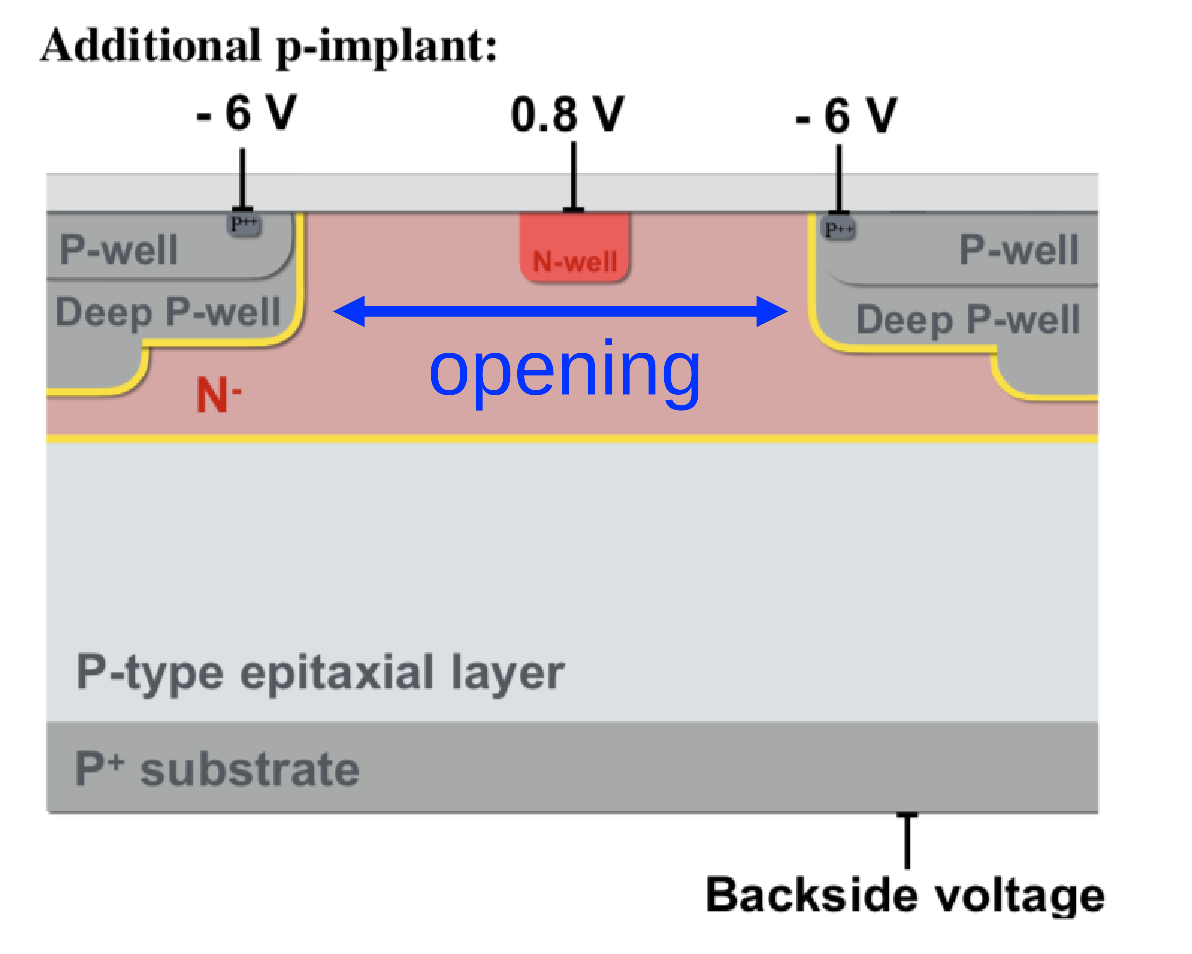
Induced current for particle incidence @ worst case ★ :



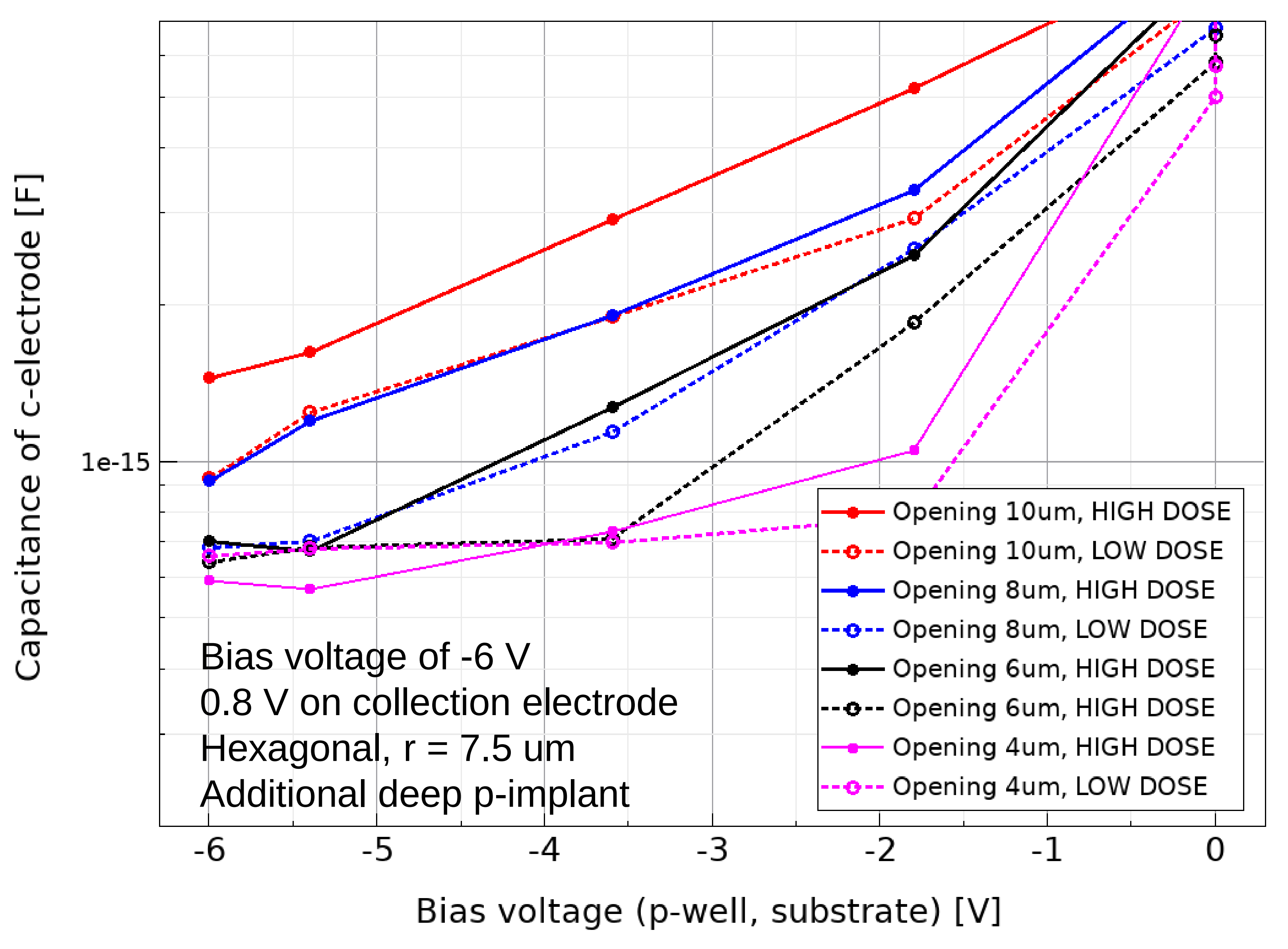

Close electrode region

Optimising the opening

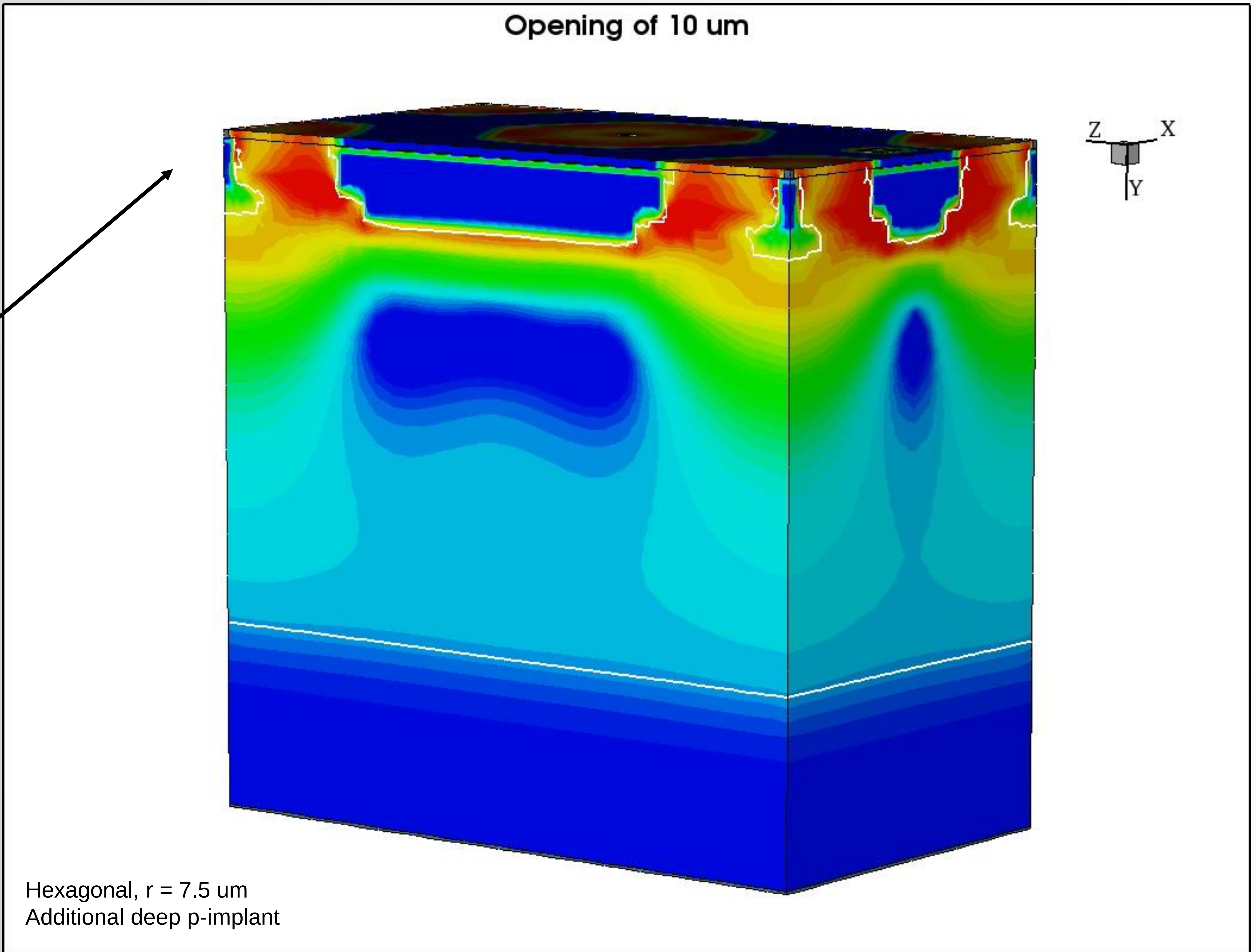
Definition of opening:



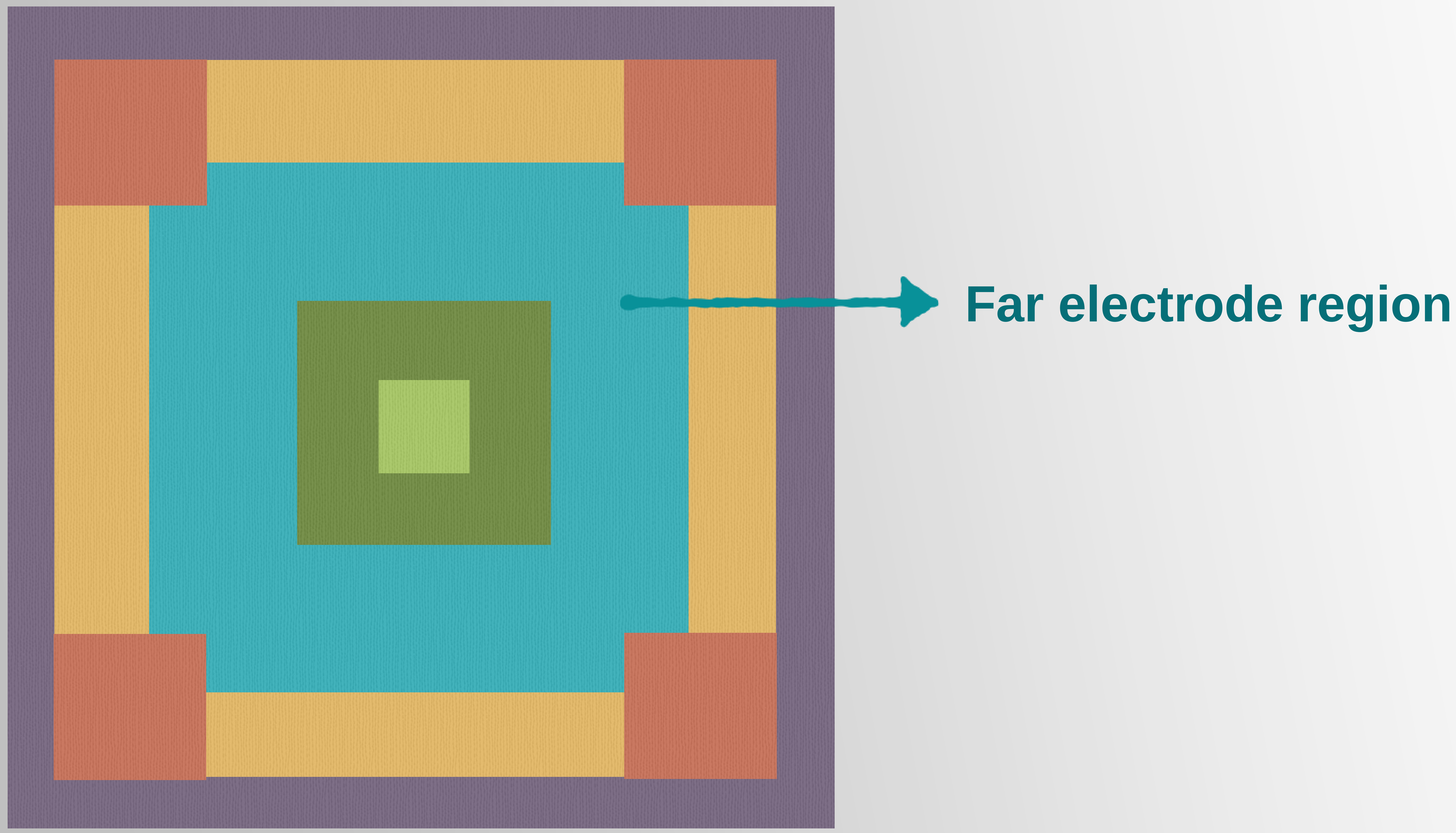
Capacitance for different n-layer doses:



Electric field & depletion around collection electrode for different openings:



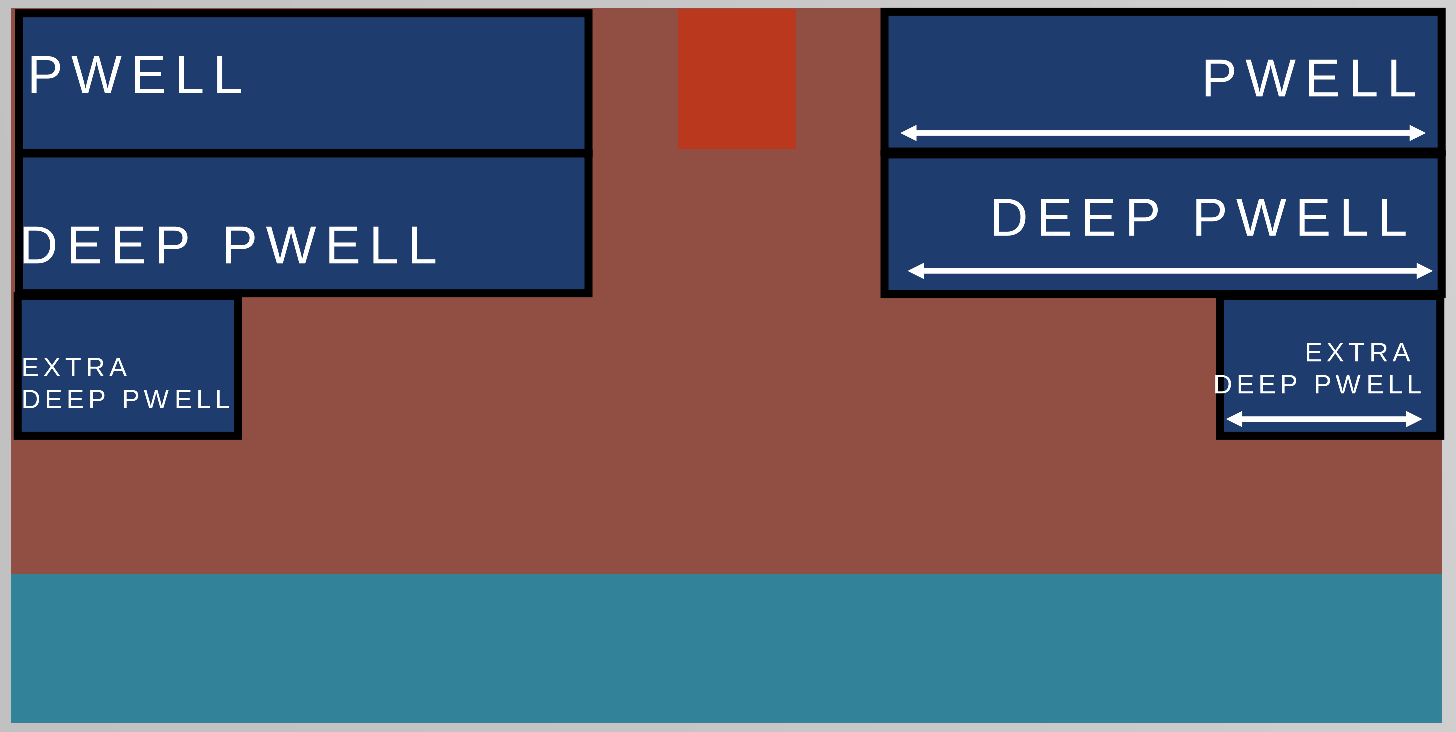
- **Trade off between small capacitance & high field**
- **Select largest opening that still fully depletes around collection electrode**


Far electrode region

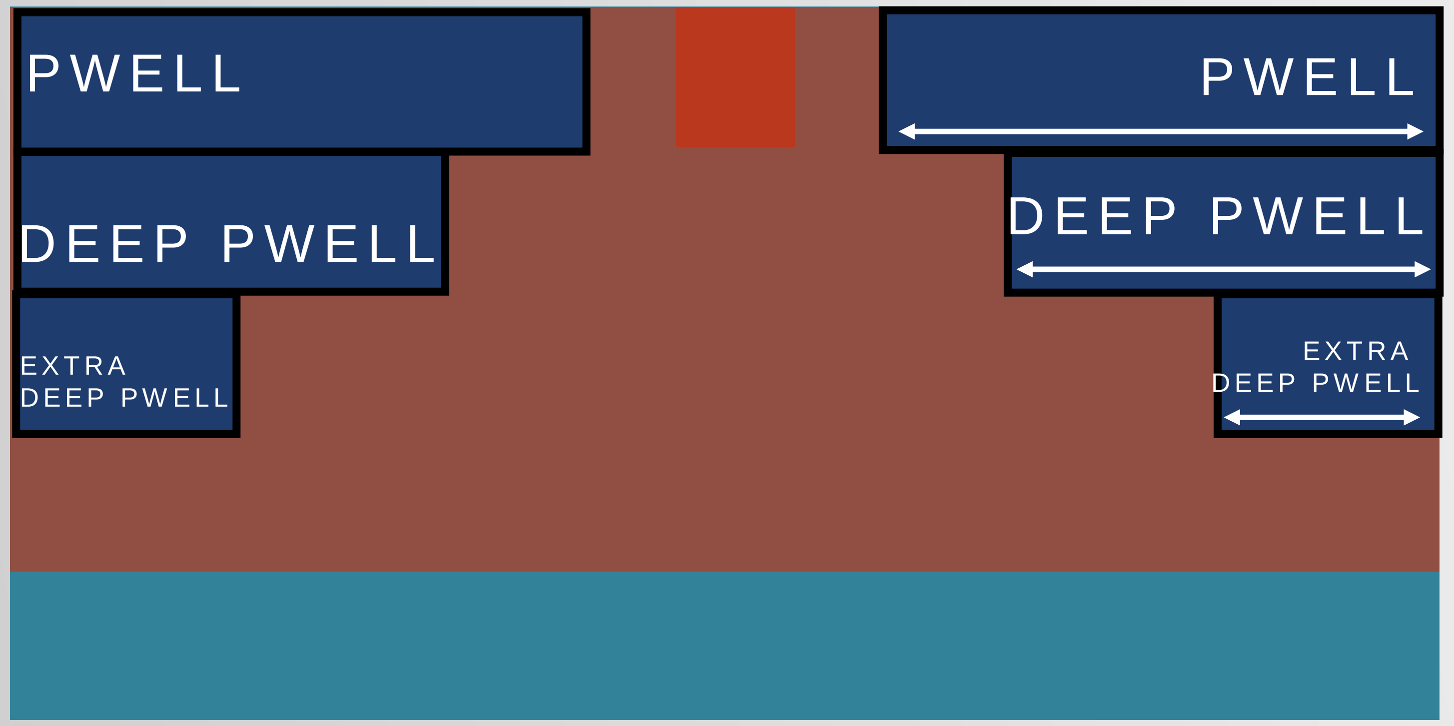
Retracing the deep p-well

Idea: can we at the same time optimise the field & capacitance by retracting the deep p-well?:

P-well & deep p-well with same distance to collection electrode:



Deep p-well with larger distance to collection electrode:



Deep p-well further away from c-electrode

—> Faster charge collection

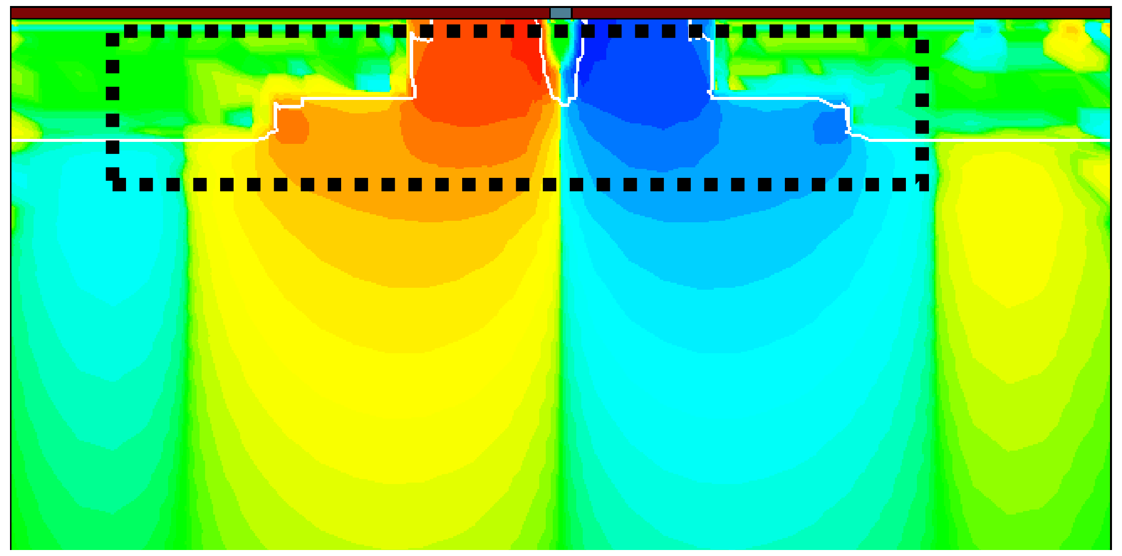
BUT:

- P-well stays close to deplete around collection electrode
- Deep p-well needs to shield circuitry (PMOS)

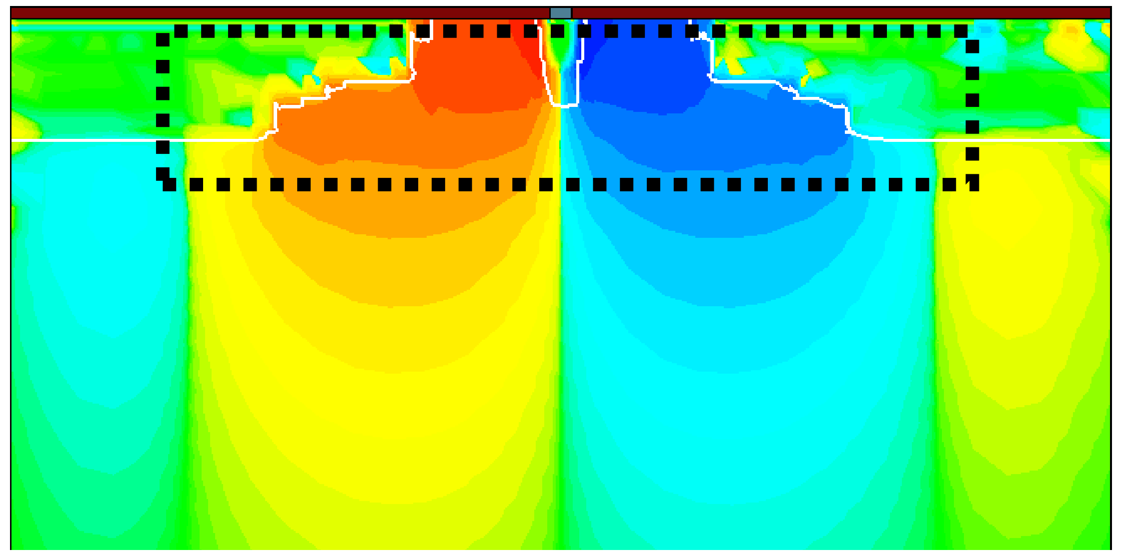
Lateral field:

Bias voltage of -6 V
0.8 V on collection electrode
Hexagonal, r = 7.5 um
Additional deep p-implant

P-well & deep p-well with same distance to collection electrode:

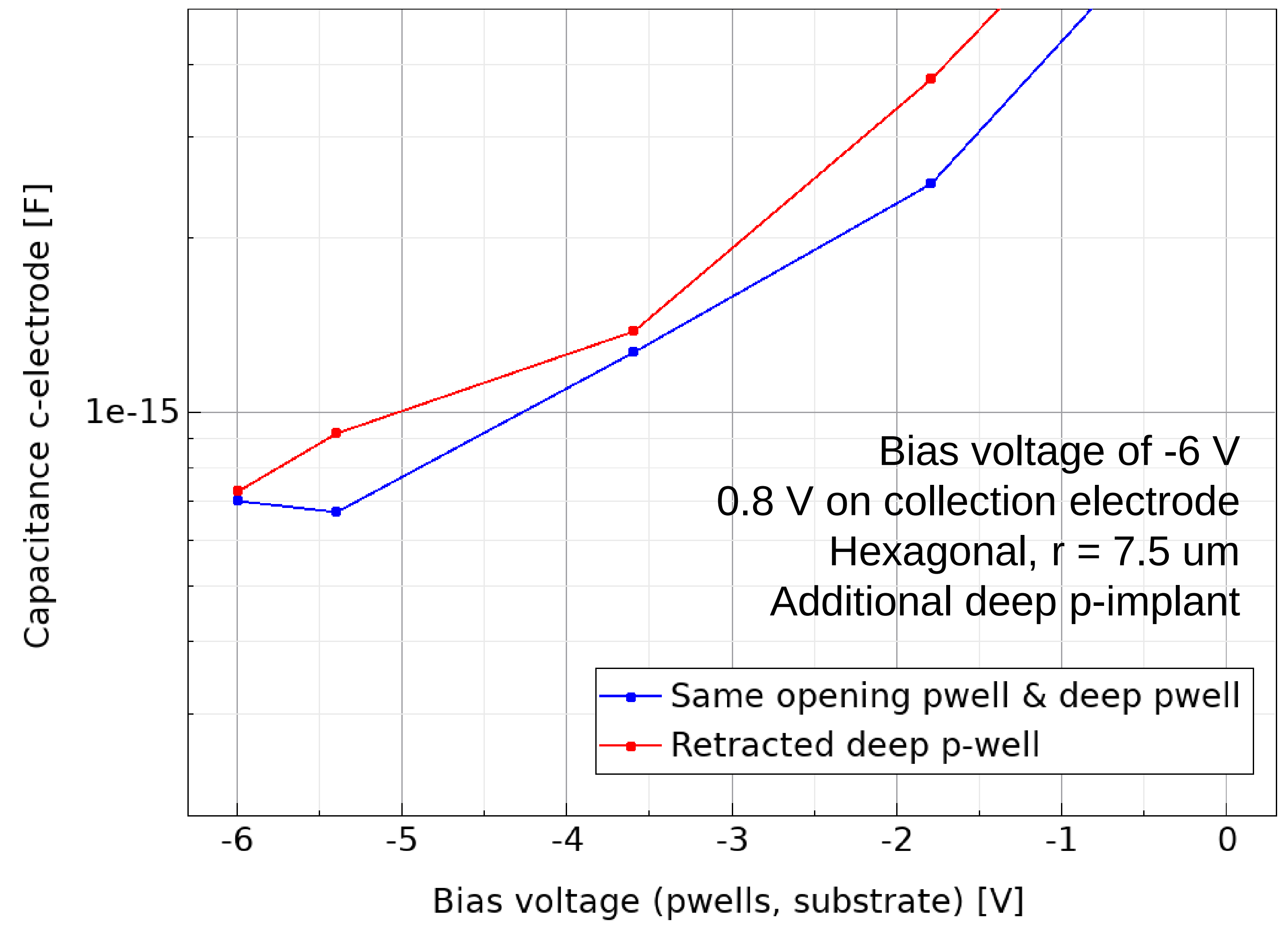


Deep p-well with larger distance to collection electrode:



—> Enhancement of lateral field by retracting deep p-well.

Capacitance:

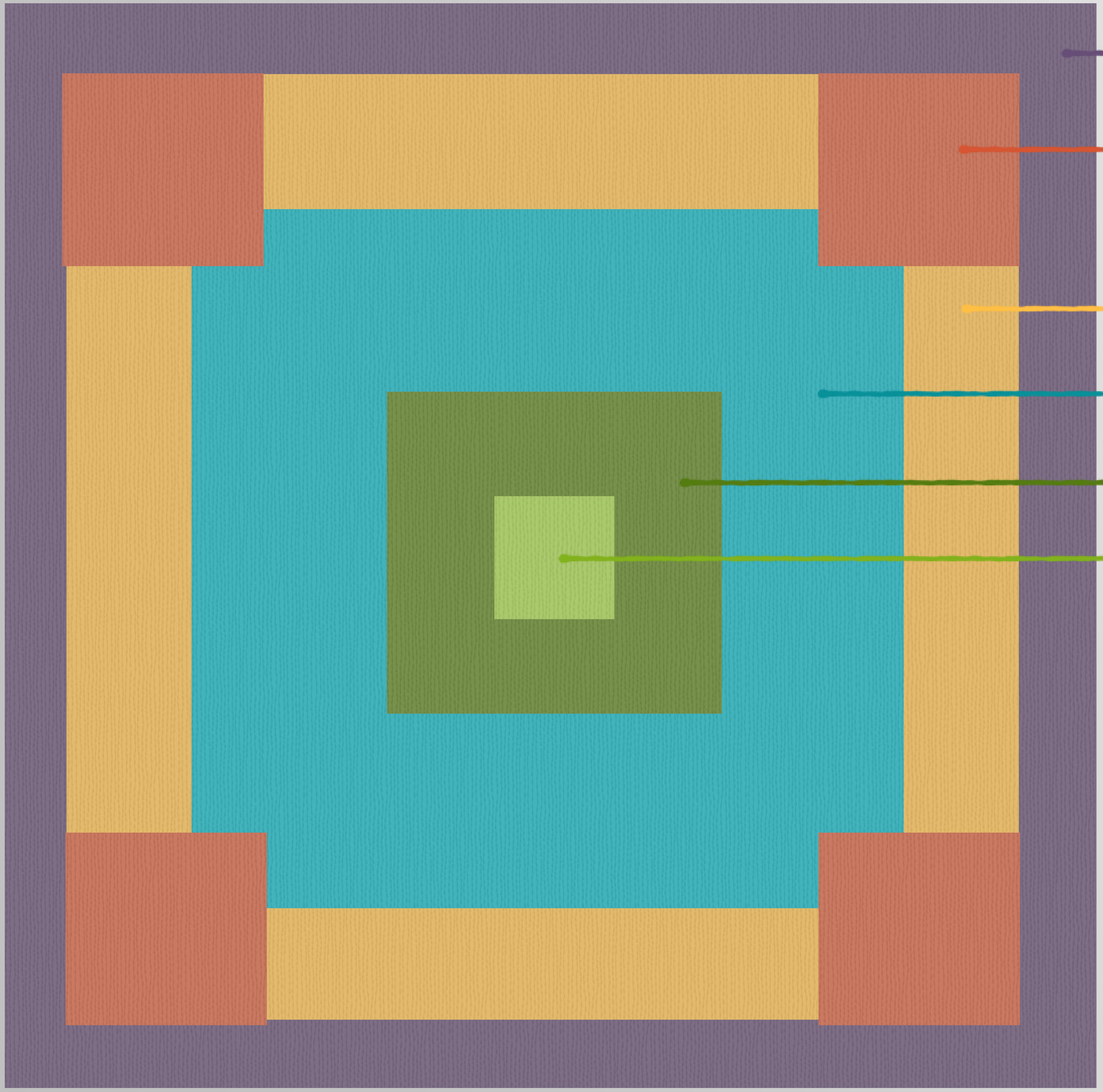


—> Retracted deep p-well does not harm capacitance.

↳ Retracting the deep p-well maximises the field while still guarantying full depletion around collection electrode & small capacitance.

Summary & outlook

<u>Optimised CMOS sensors with a small collection electrode w.r.t. fast charge collection, small sensor capacitance and precise spatial resolution:</u>

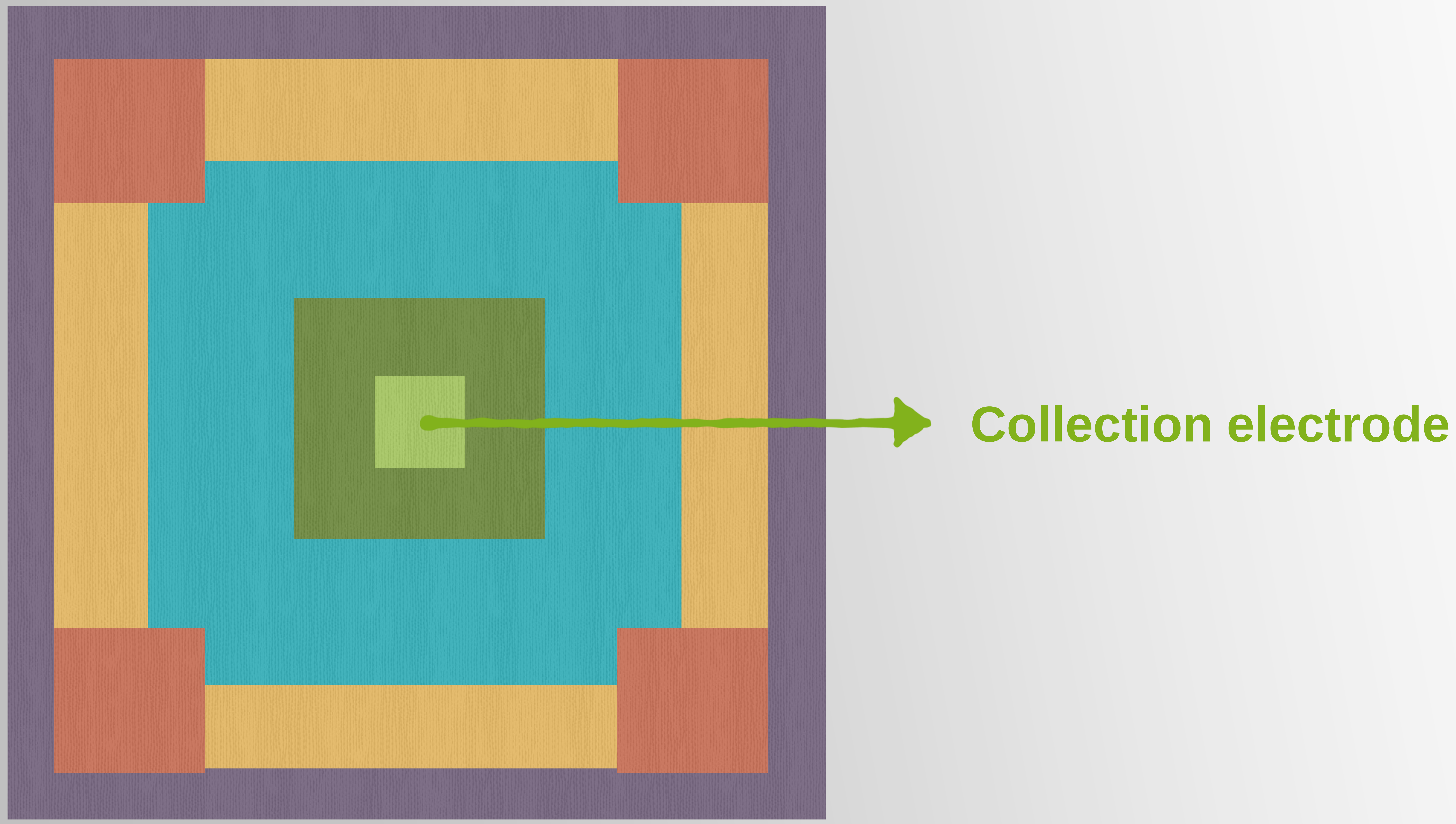


<u>Comprehensive optimisation, a few examples presented here.</u>

↳ Using these studies, an **analogue test chip will be submitted for ultra fast timing & very precise spatial resolution with pixel sizes down to < 10 um**, to investigate future prospects for smaller feature sizes (ATTRACT FASTPIX).

Thank you.

BACKUP


Collection electrode

Optimising the collection electrode

Minimisation of capacitance:

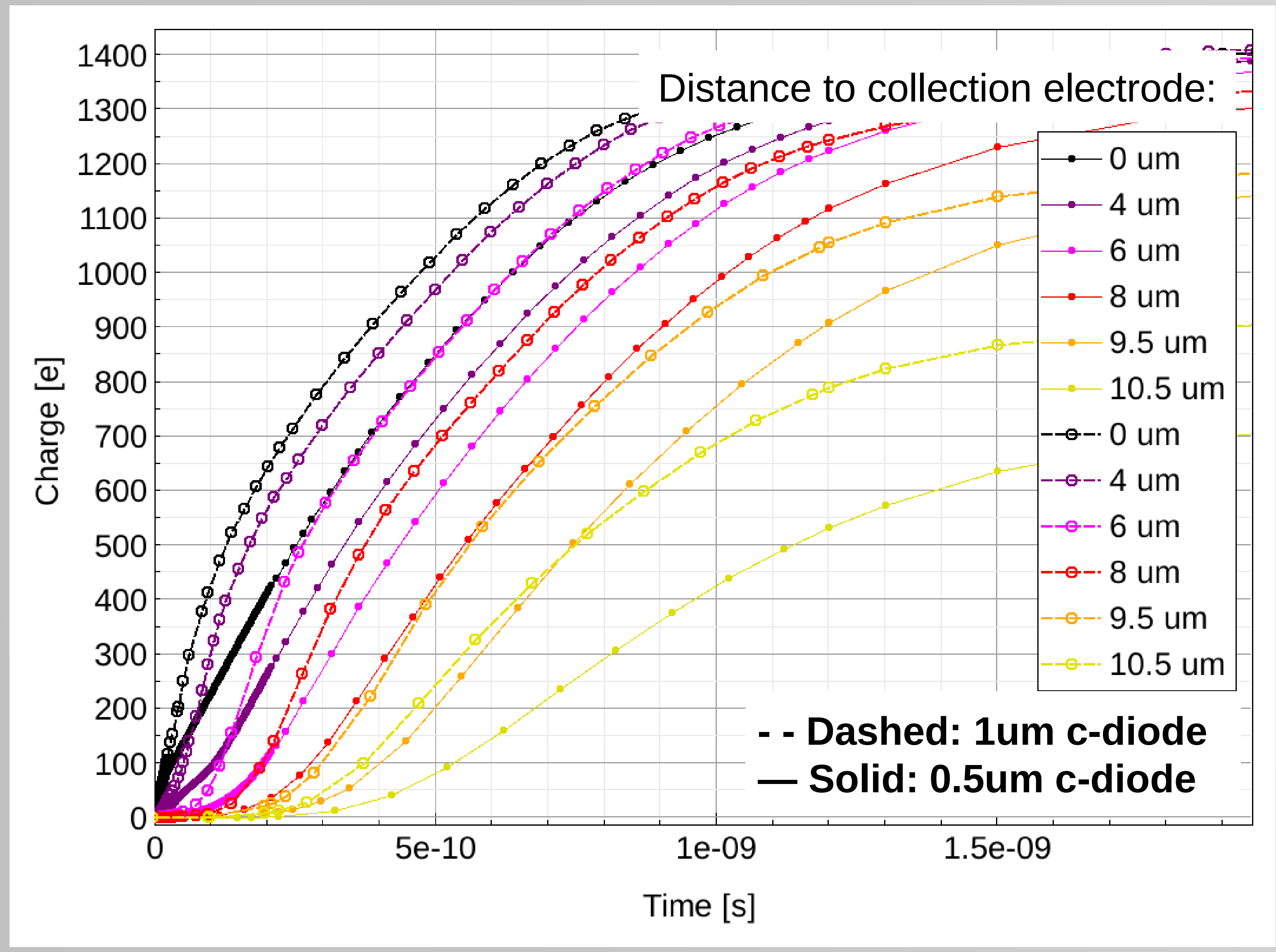
- Sensor **capacitance C ∝ radius of collection electrode**

—> Want collection electrode as **small** as possible to **minimise capacitance** (maximise readout **charge Q = I/C)**

Maximisation of electric field:

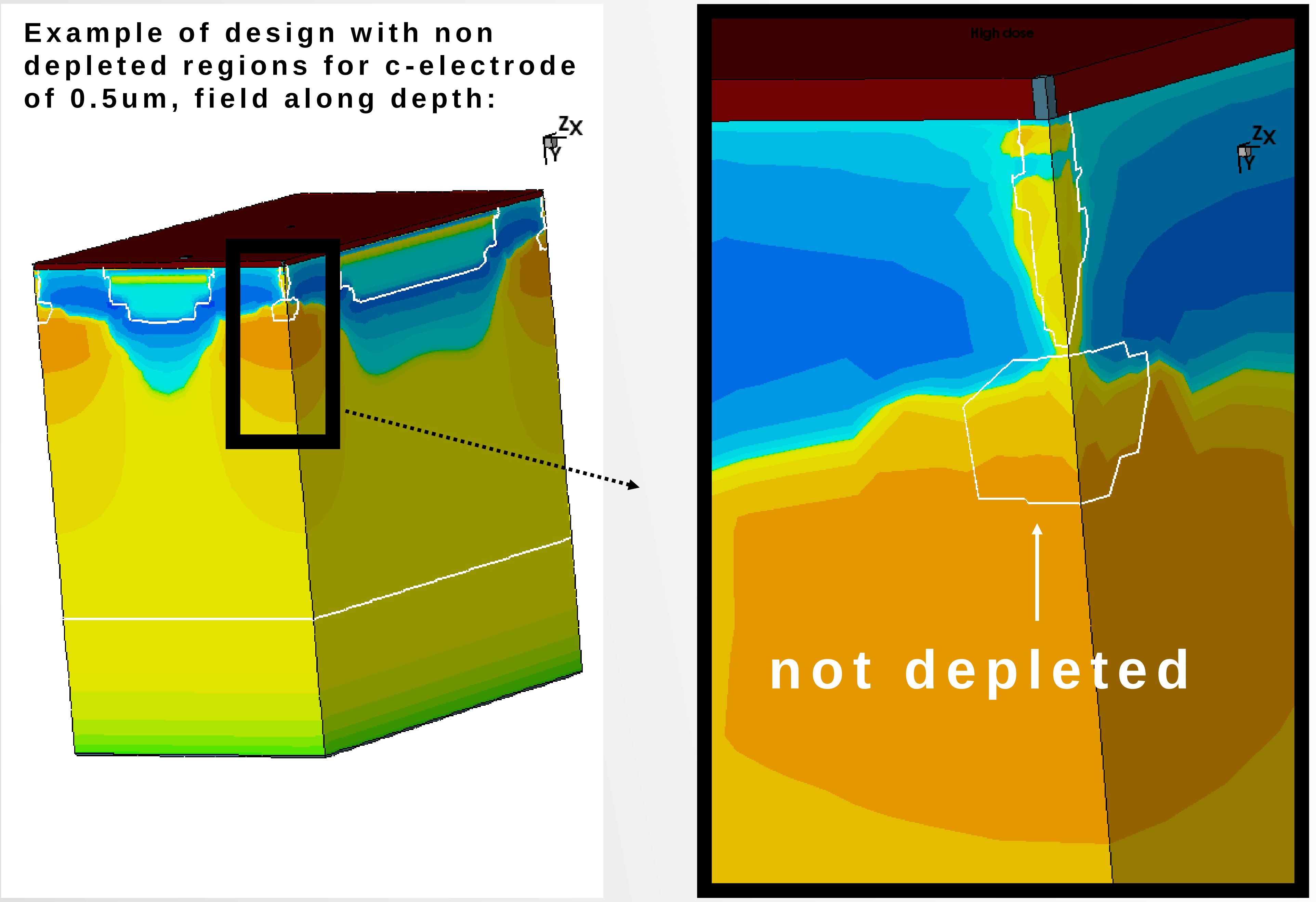
—> Want collection electrode as **large** as possible to

maximise electric field & charge collection speed



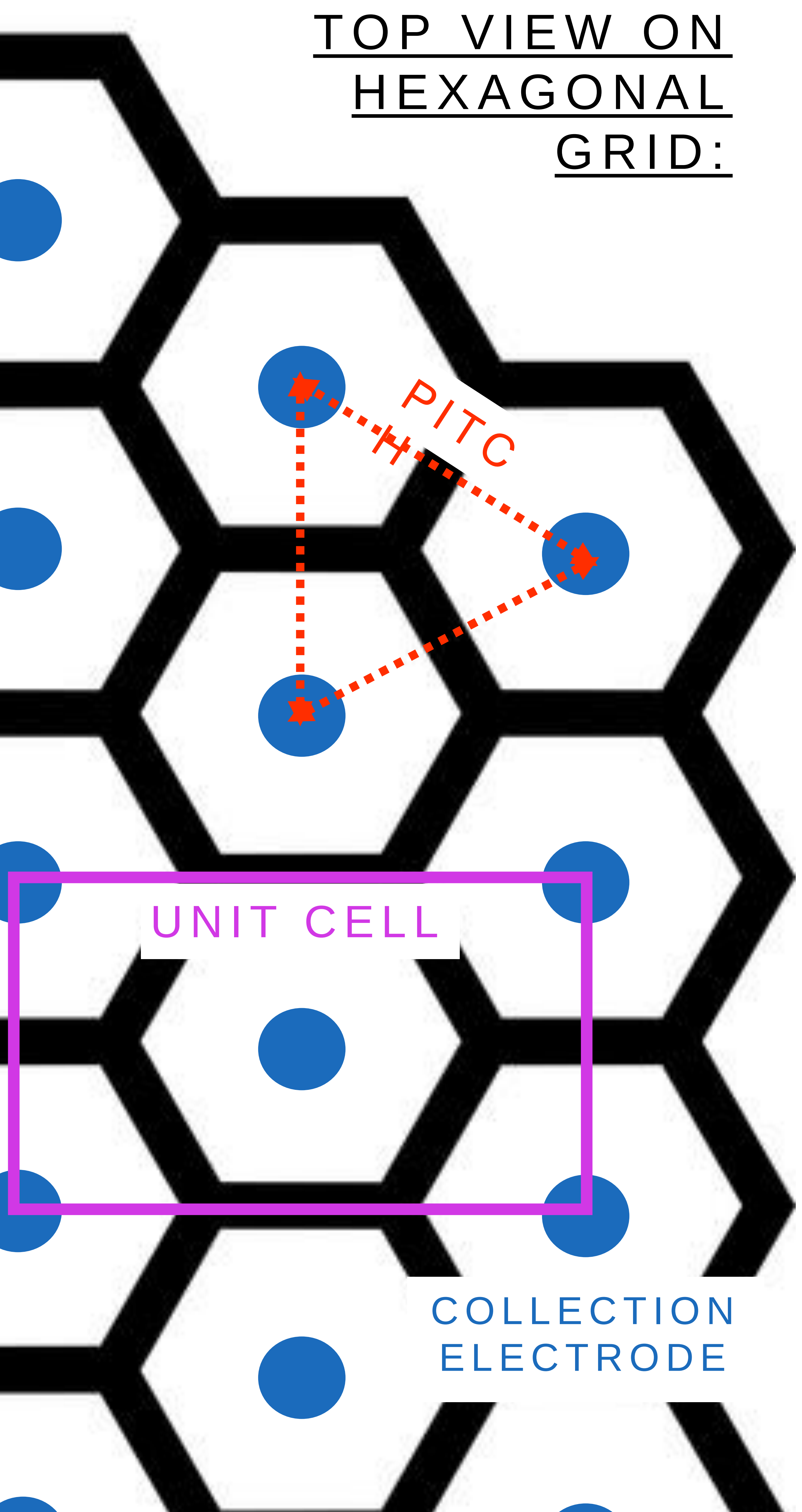
Guarantee full depletion:

—> Challenging to fully deplete for collection electrode sizes < 1 um



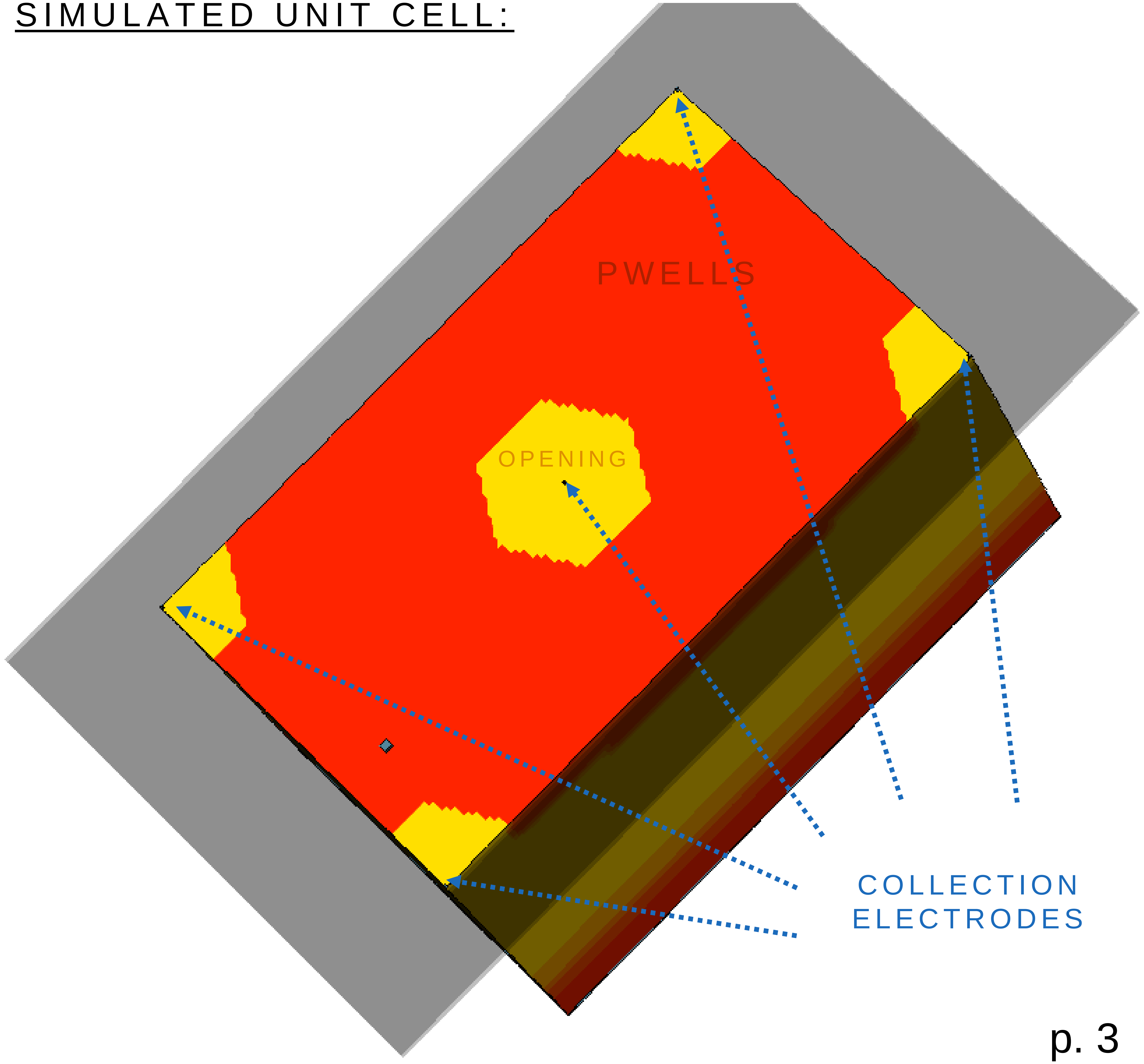
Select collection electrode size of 1um.

HEXAGONAL PIXELS - STUDIED DESIGN



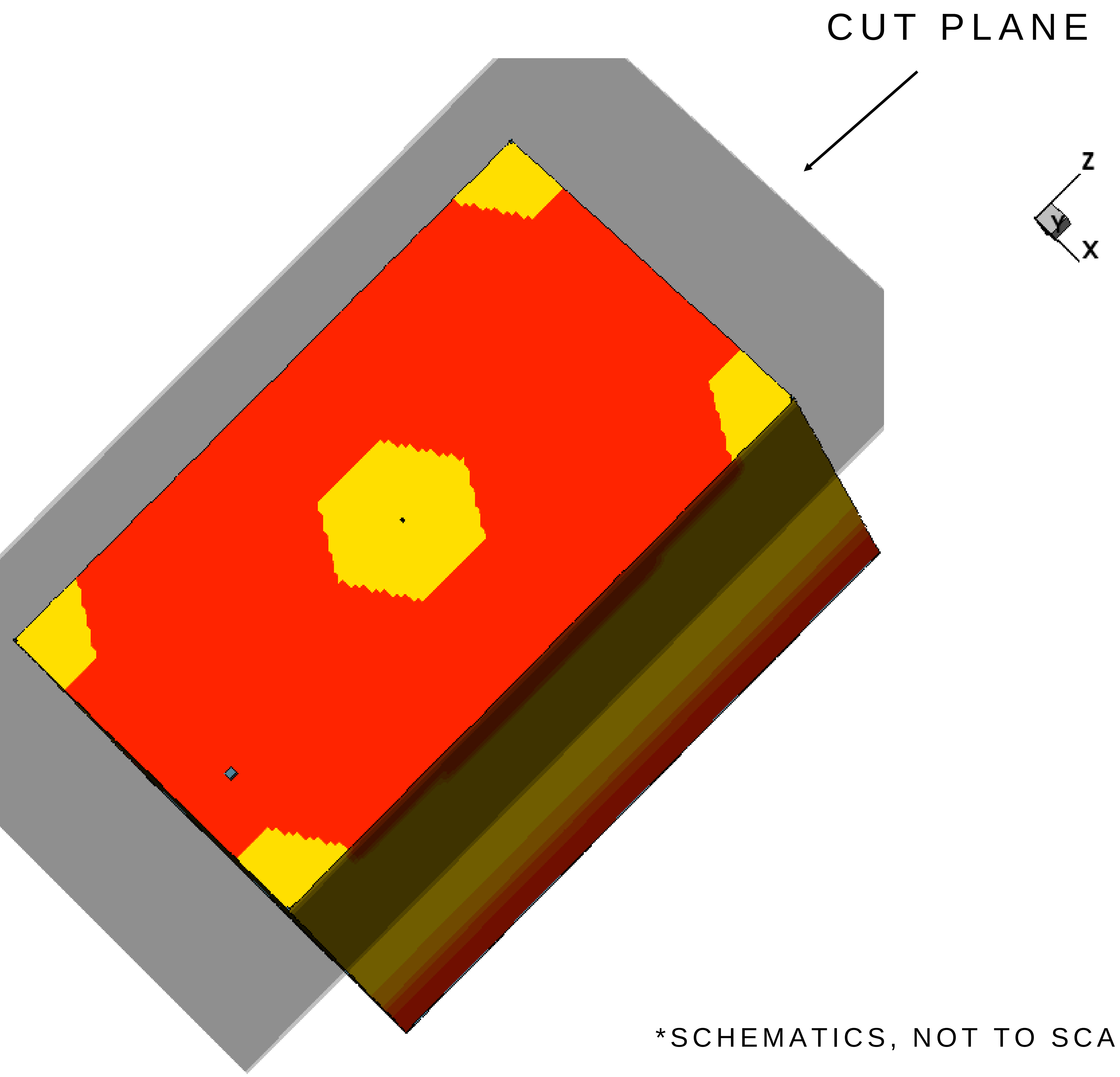
UNIT CELL:
Smallest cell that can periodically reproduce hexagonal grid and holds symmetry for transient study

SIMULATED UNIT CELL:



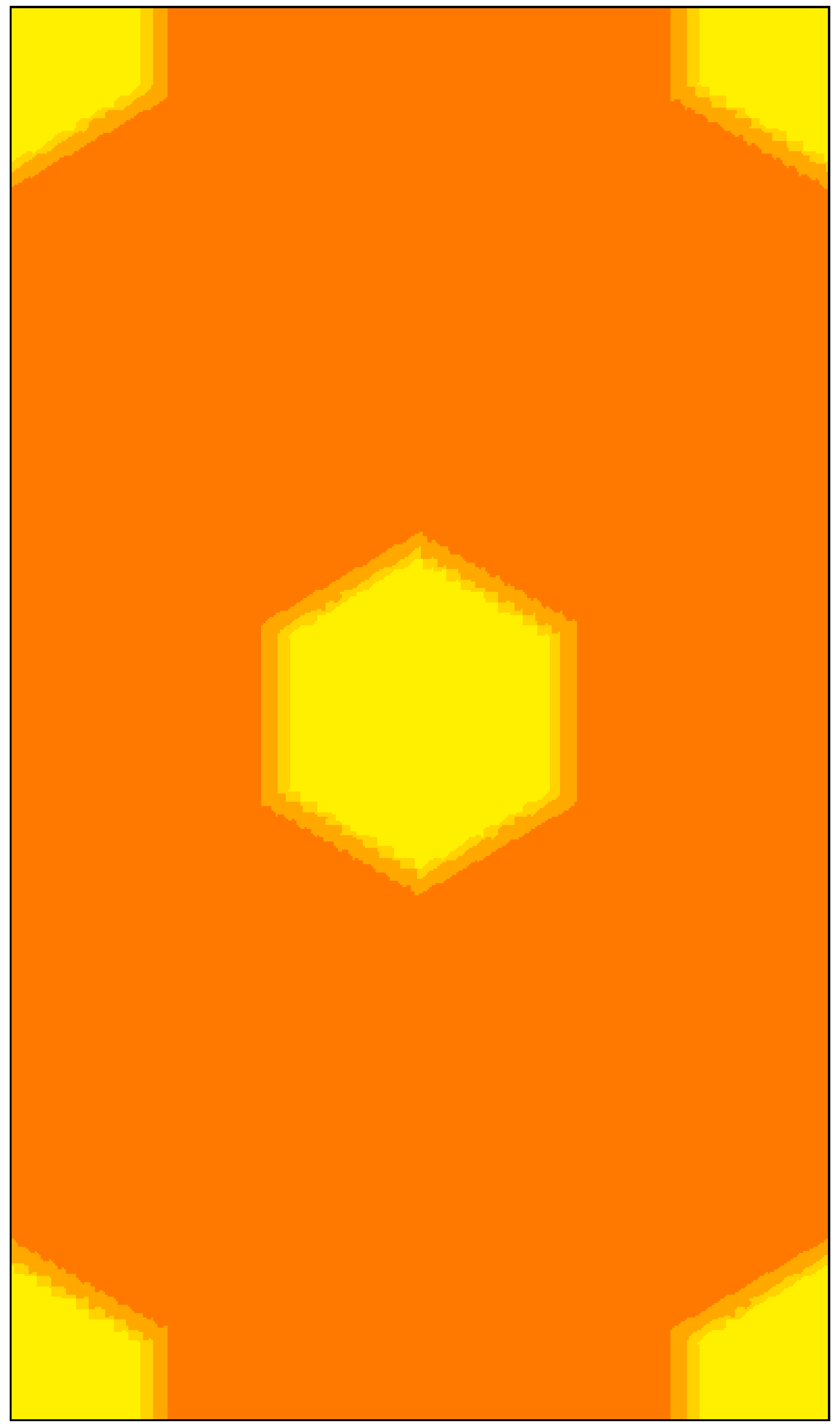
HEXAGONAL PIXELS - STUDIED DESIGN

Simulated unit cell:

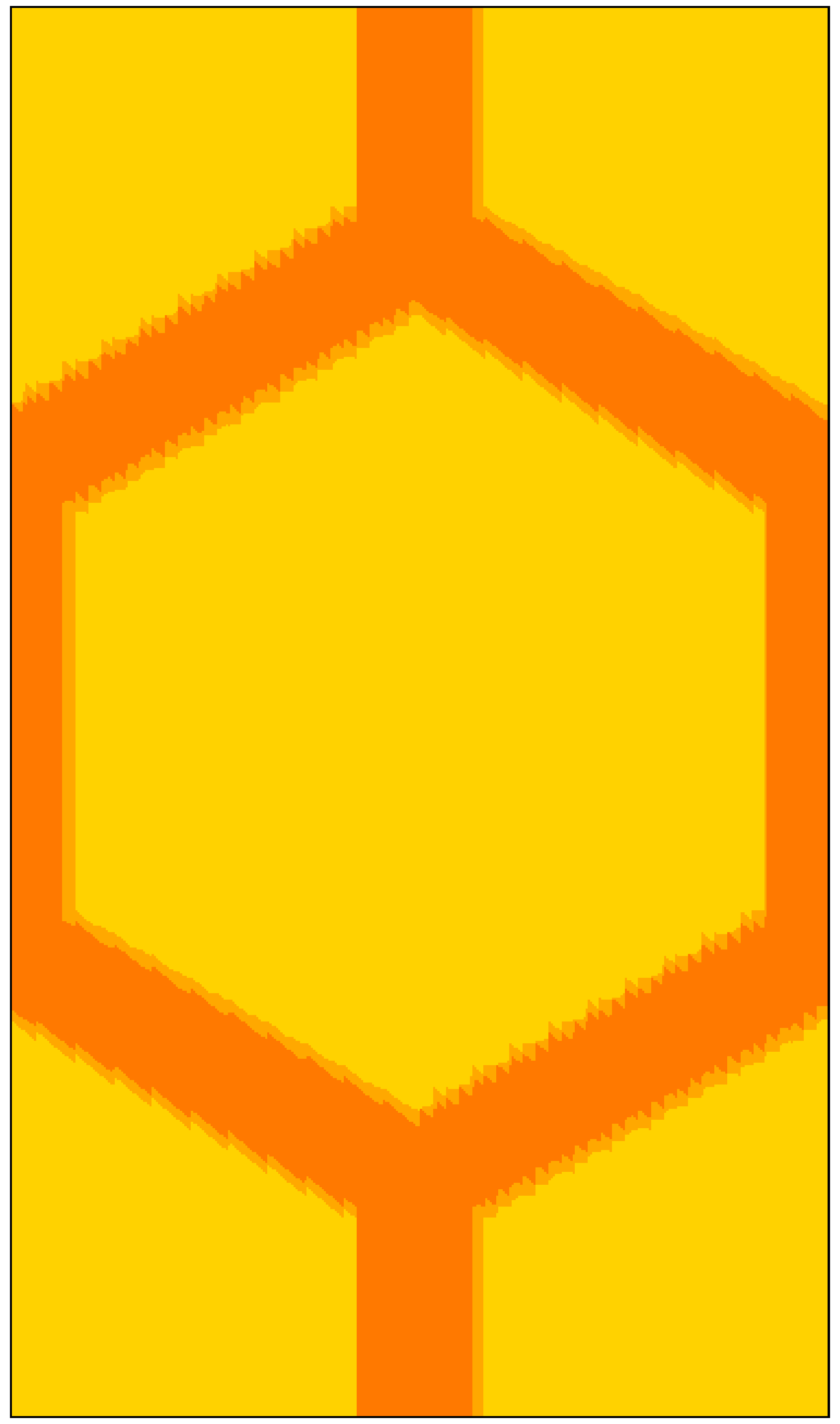


*SCHEMATICS, NOT TO SCALE

CUT @ DEPTH OF PWELLS:



CUT @ DEPTH OF ADDITIONAL P-IMPLANT:



Lesson learned

- Electric field fundamentally different w.r.t. standard planar sensors
- The lateral field is most important, especially in the pixel corners
- Implants at pixel edge help to increase lateral field & charge collection
- Trade off between high field & low capacitance:
  - A smaller opening is favourable to reduce the capacitance, while a larger opening is favourable for a fast charge collection
  - A smaller collection electrode is favourable for a minimised capacitance, while a large collection electrode is favourable for a higher field
- Retracting the deep p-well helps to simultaneously optimise capacitance & field

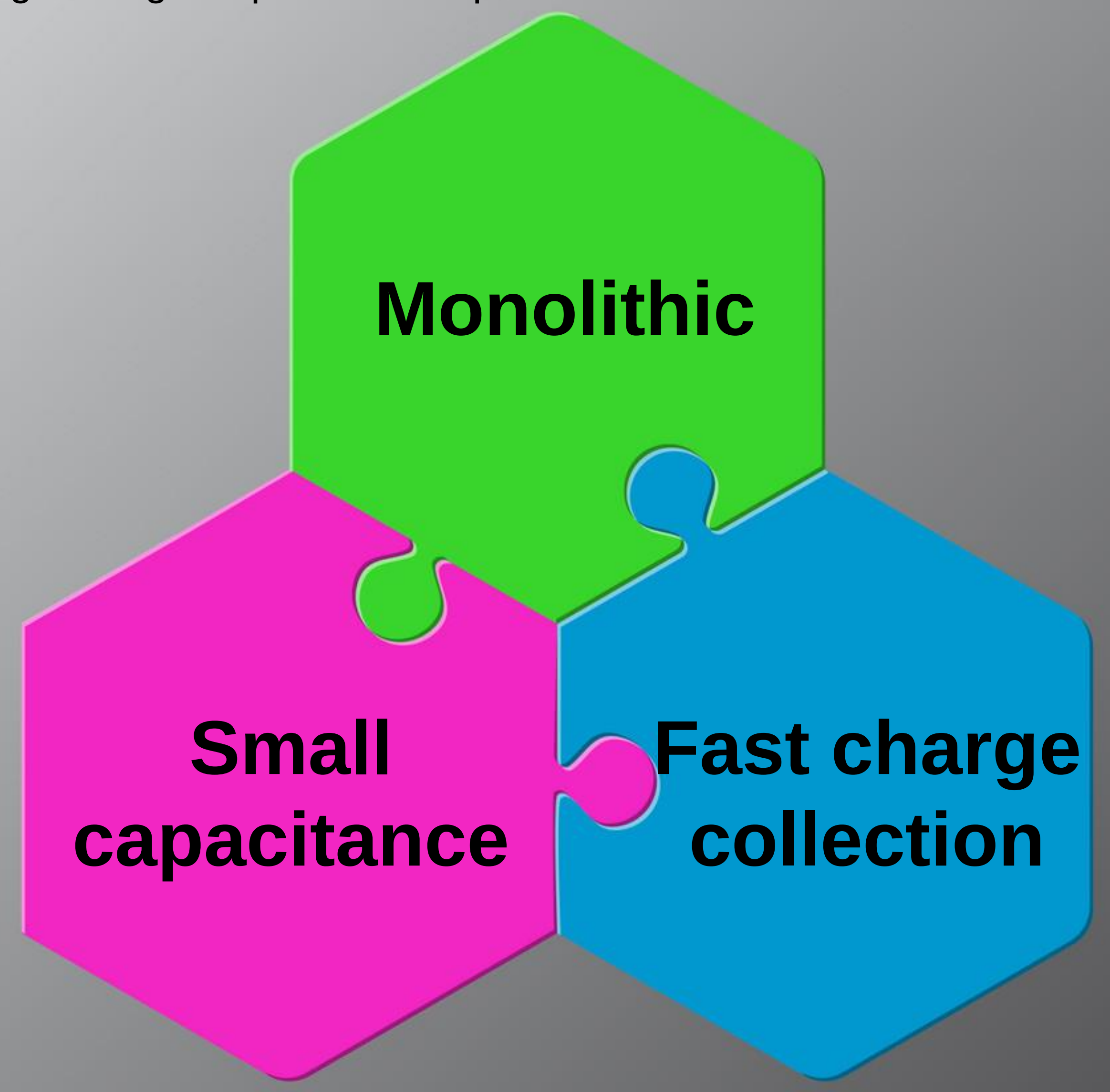
Motivation - why to further optimise?

<u>In the framework of attract FASTPIX:</u>

Combine advantages of CMOS sensors with a small collection electrode **(low cost & material, reduced production effort, small sensor capacitance)** with a fast charge collection **(ultra fast timing & radiation tolerance)** and precise spatial resolution

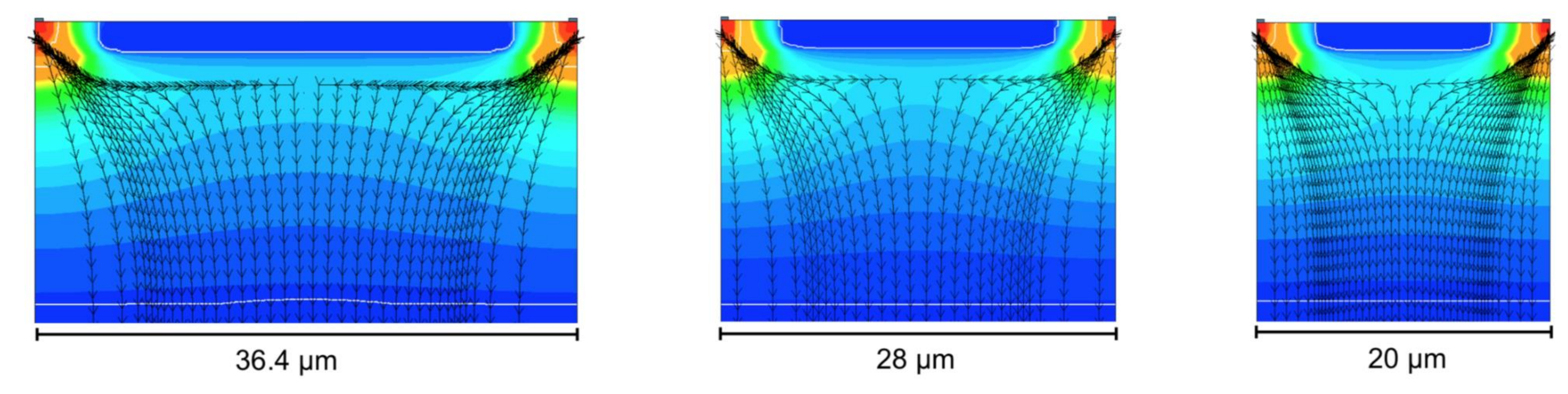
- <u>Aim for first year:</u> benchmark sensor designs (“analogue” performance)
- <u>Relevance for CLIC vertex detector:</u> precise resolution with small pixels, low material monolithic detector

https://www.vectorstock.com/royalty-free-vector/three-piece-puzzle-hexagon-diagram-puzzle-3-step-vector-21053559



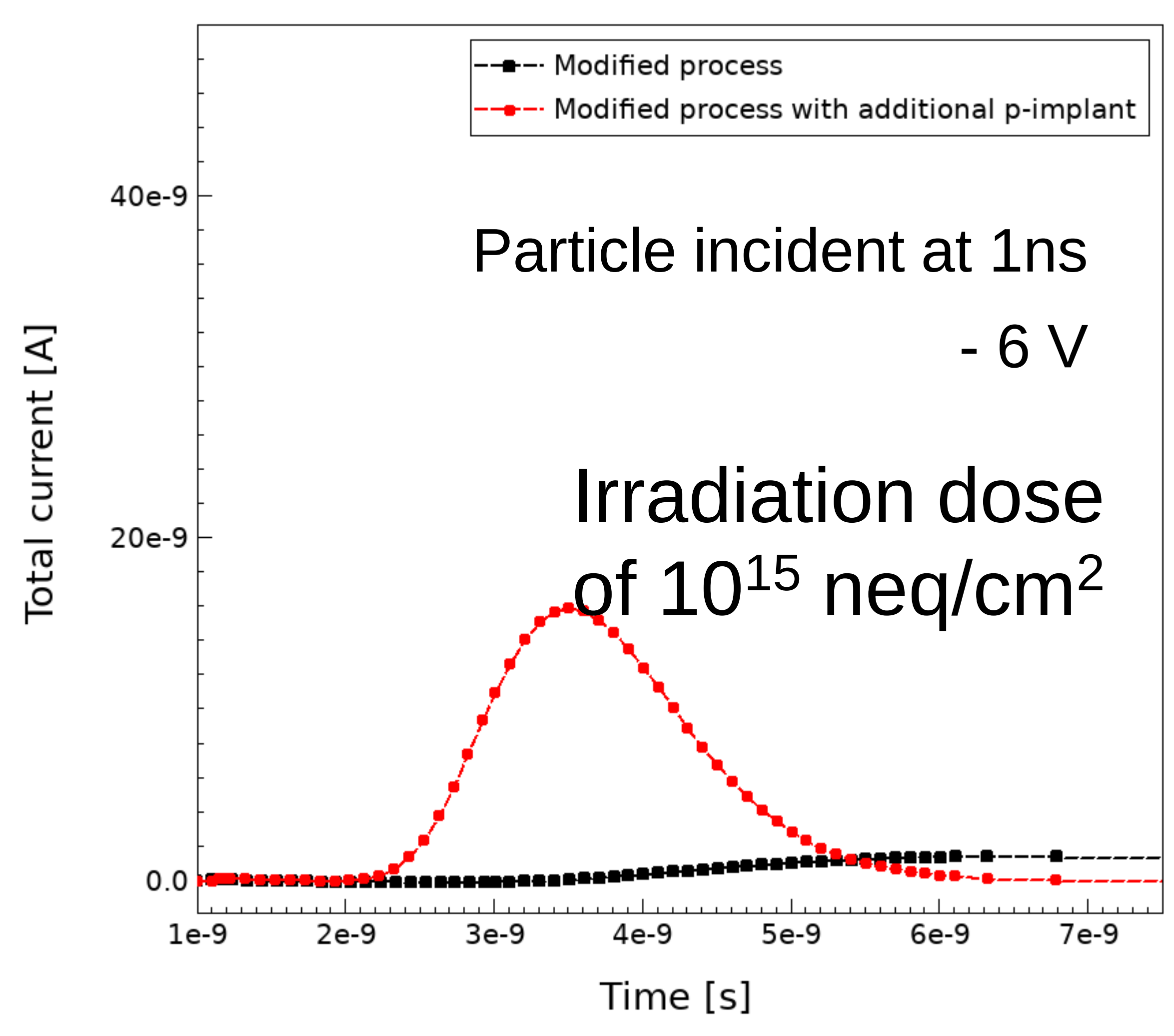
Optimising the overall pixel shape - pixel pitch

Electrostatic potential & streamlines for different pixel pitch:

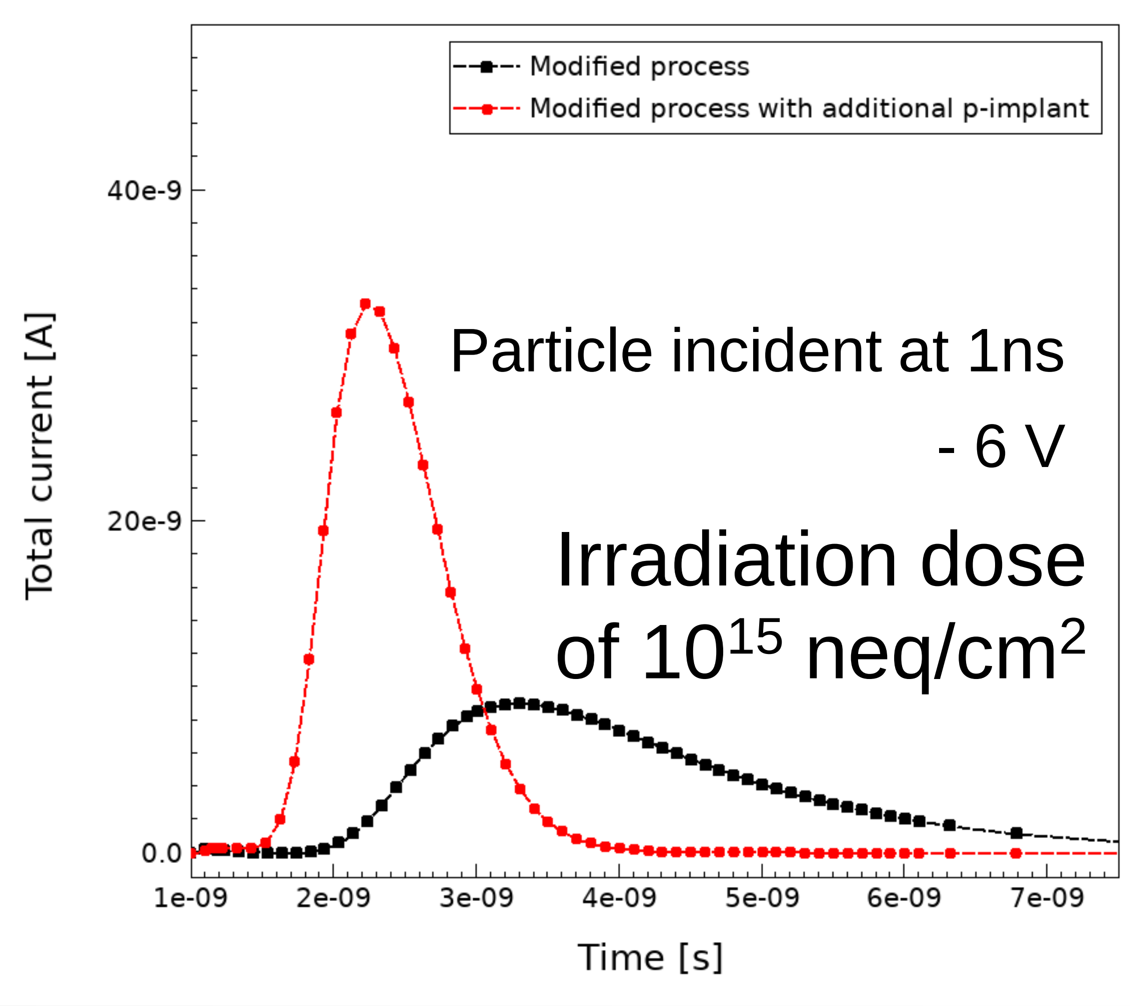


- Better opening of streamlines towards collection electrode for smaller pixels
- Strong dependancy of performance on pixel pitch: https://doi.org/10.1088/1748-0221/13/01/C01023

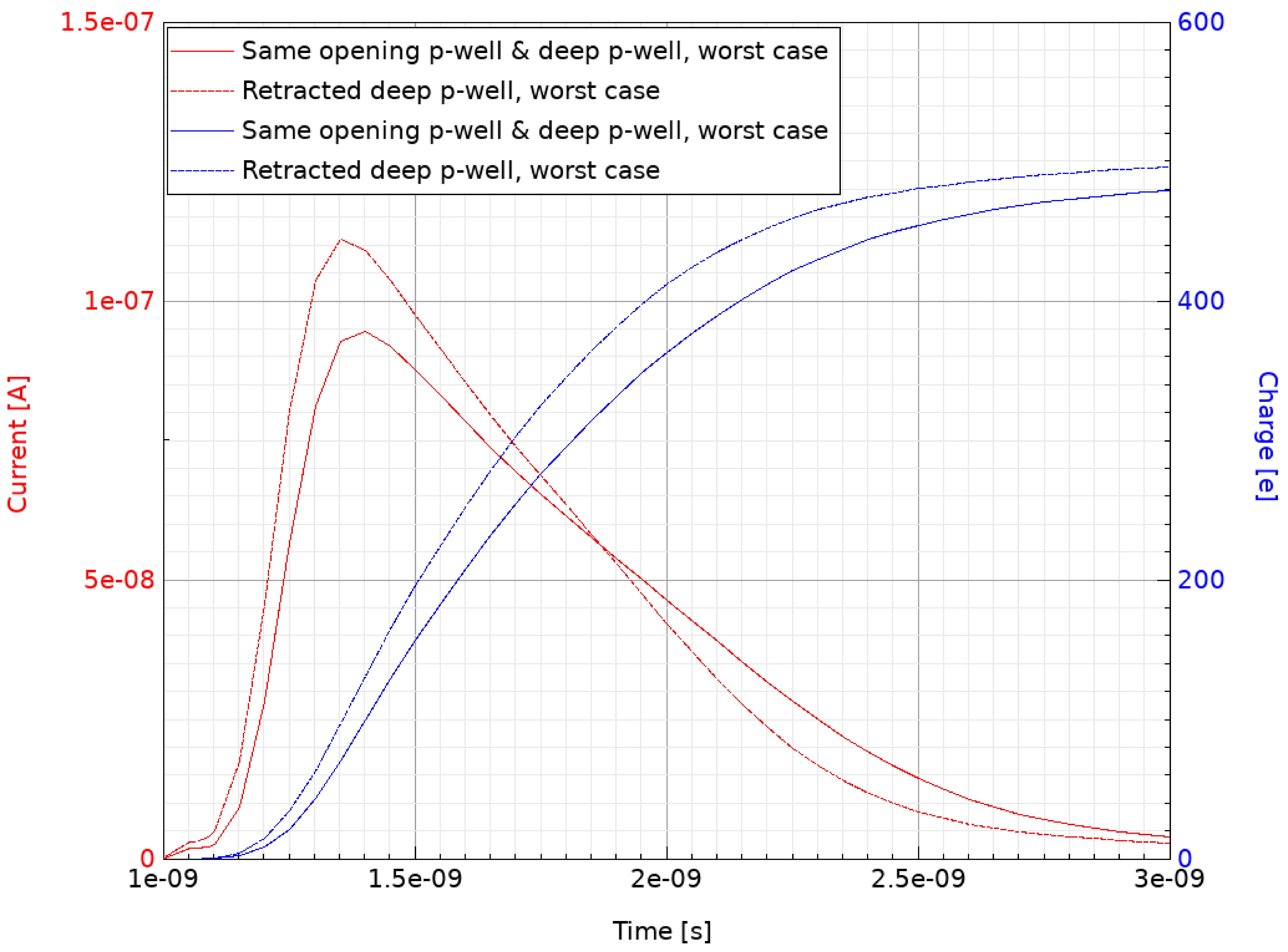
Pixel size 36.4 x 36.4 µm^2:



Pixel size 28 x 28 µm^2:

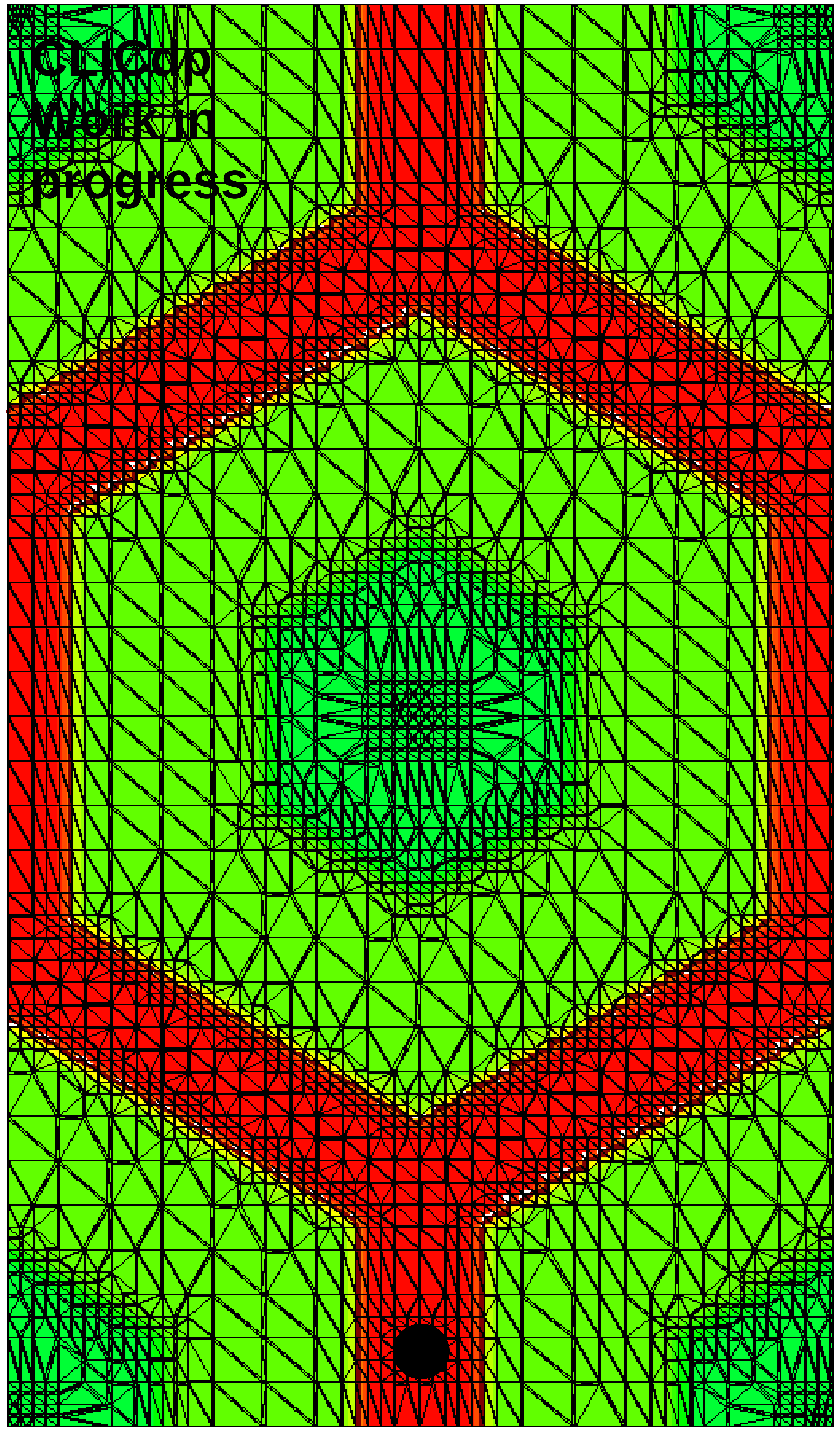


RETRACTED DEEP P-WELL

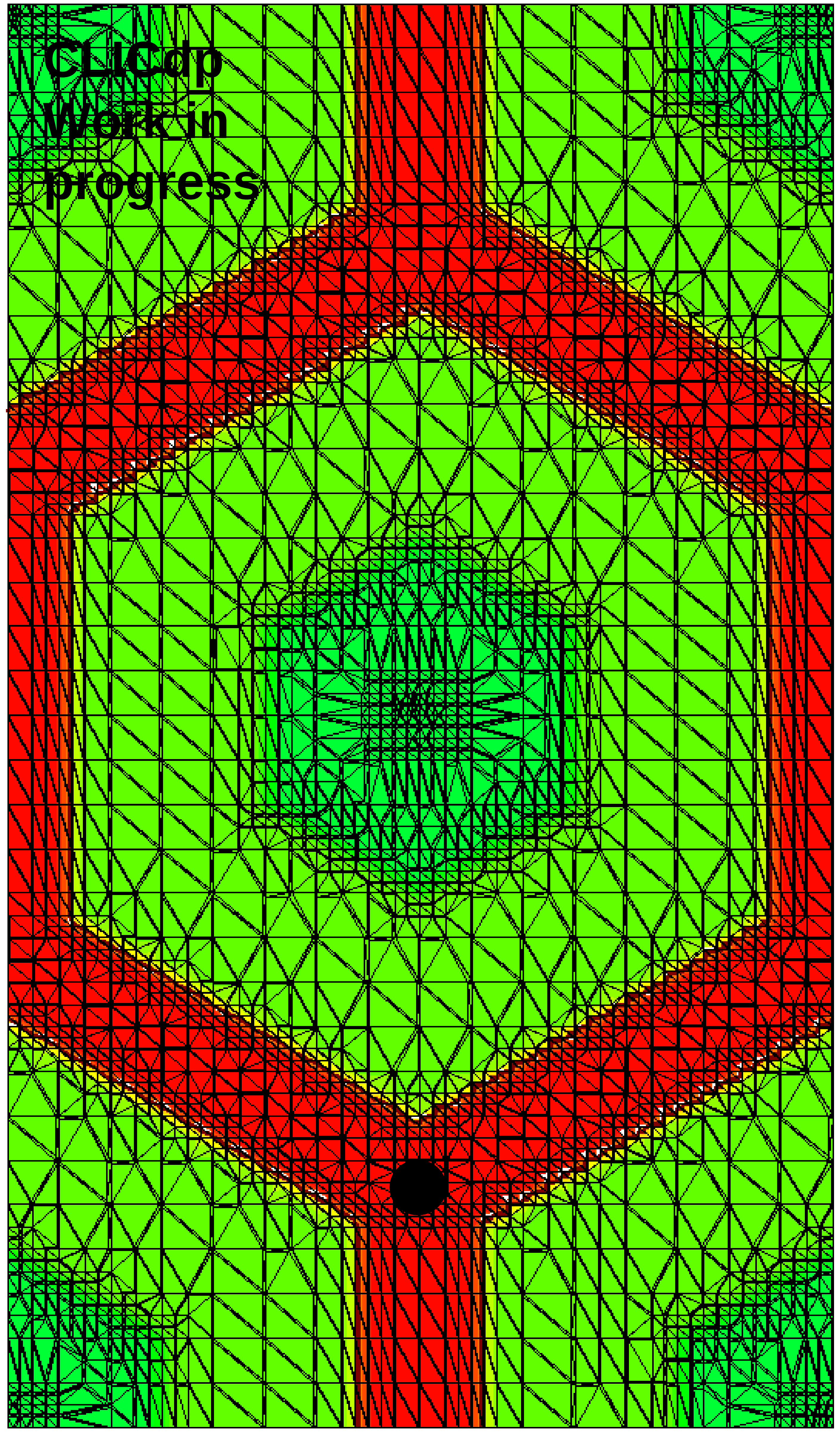


Some considerations on the 'worst case' in the hexagonal pixel design

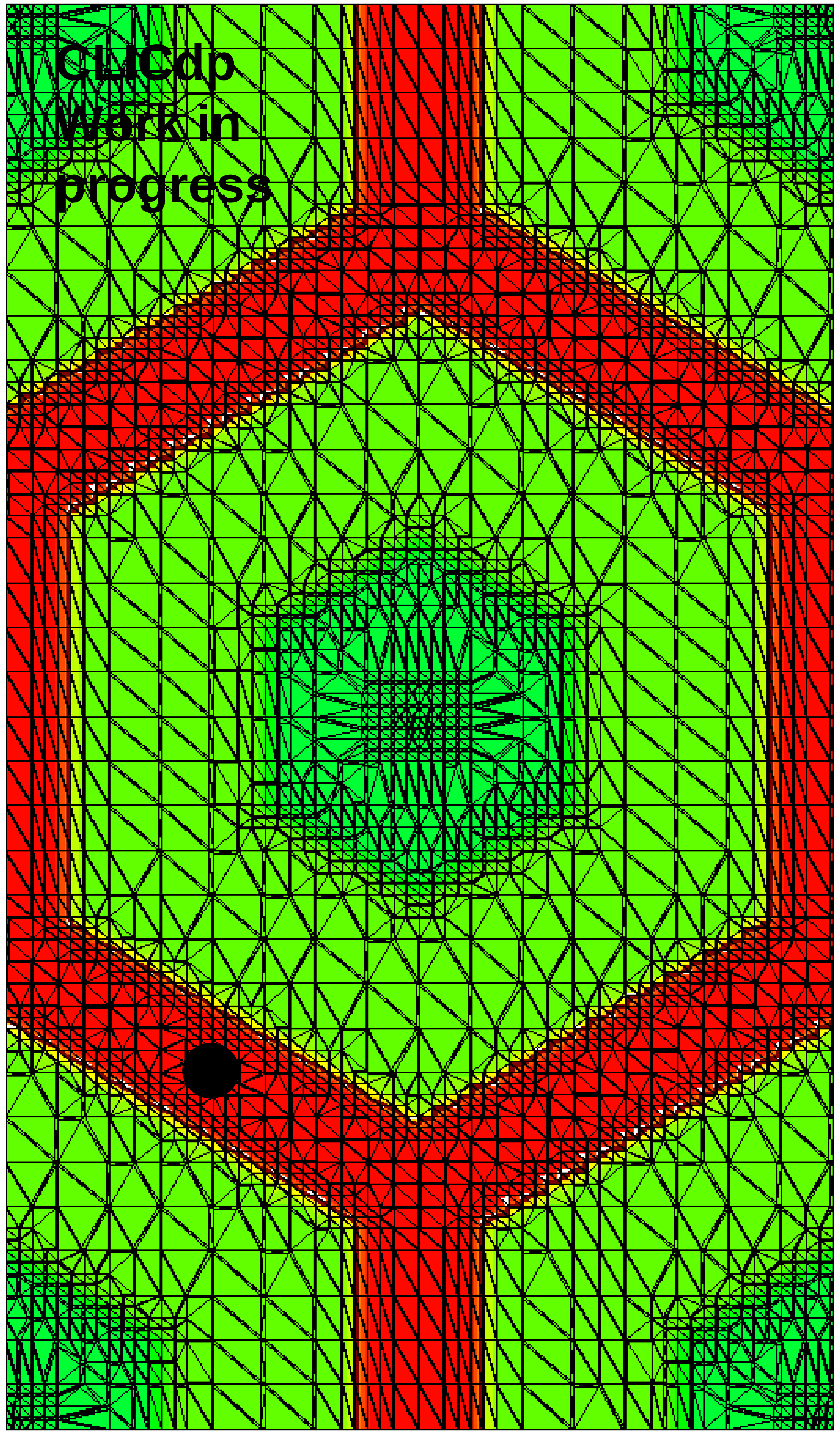
Position 0:



Position 1:

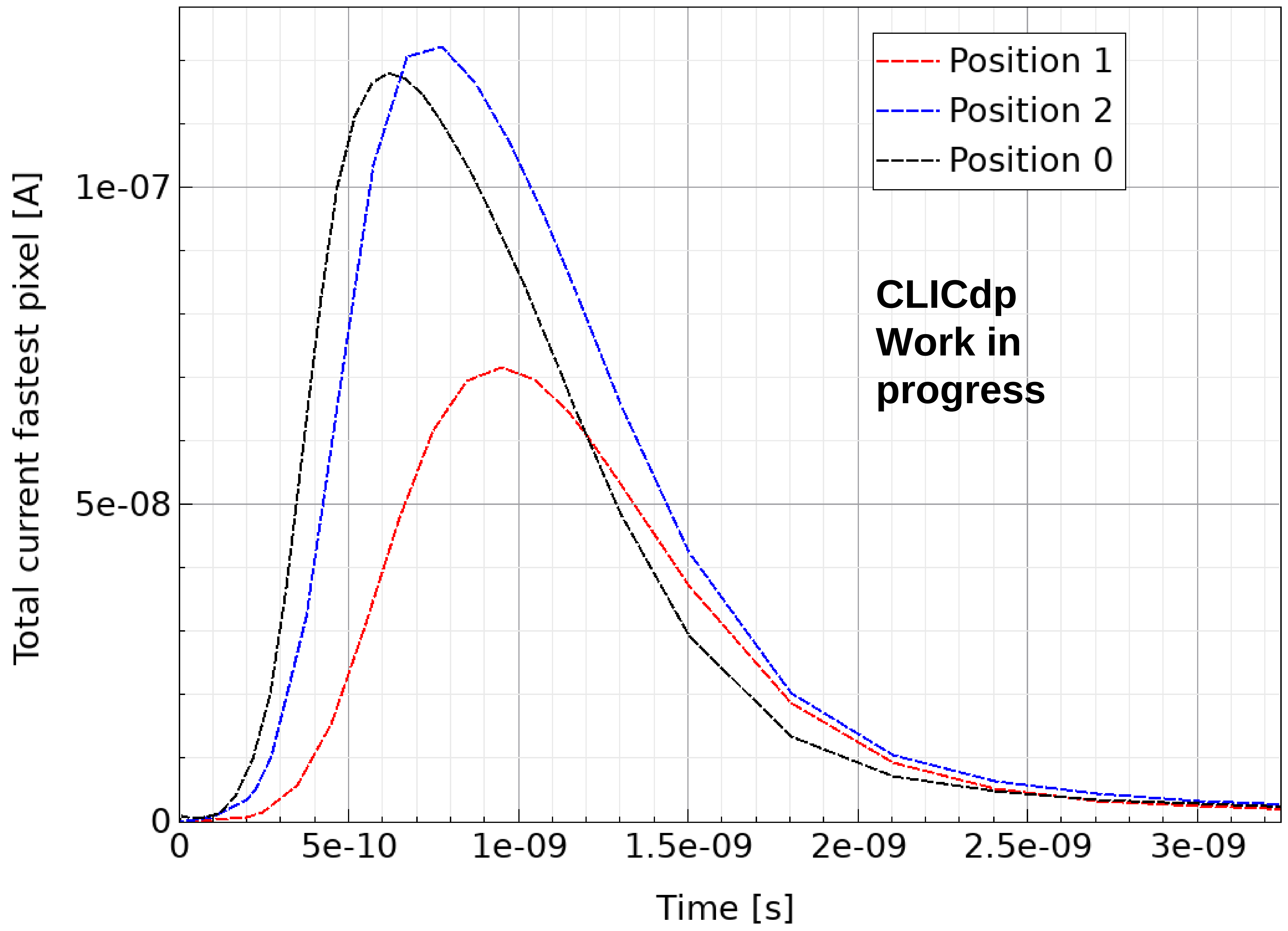


Position 2:



Some considerations on the 'worst case' in the hexagonal pixel design

Induced current of fastest pixel - c-electrode size of 0.5um:



—> Position 1 with equal distance to collection electrodes is worst case in view of timing.