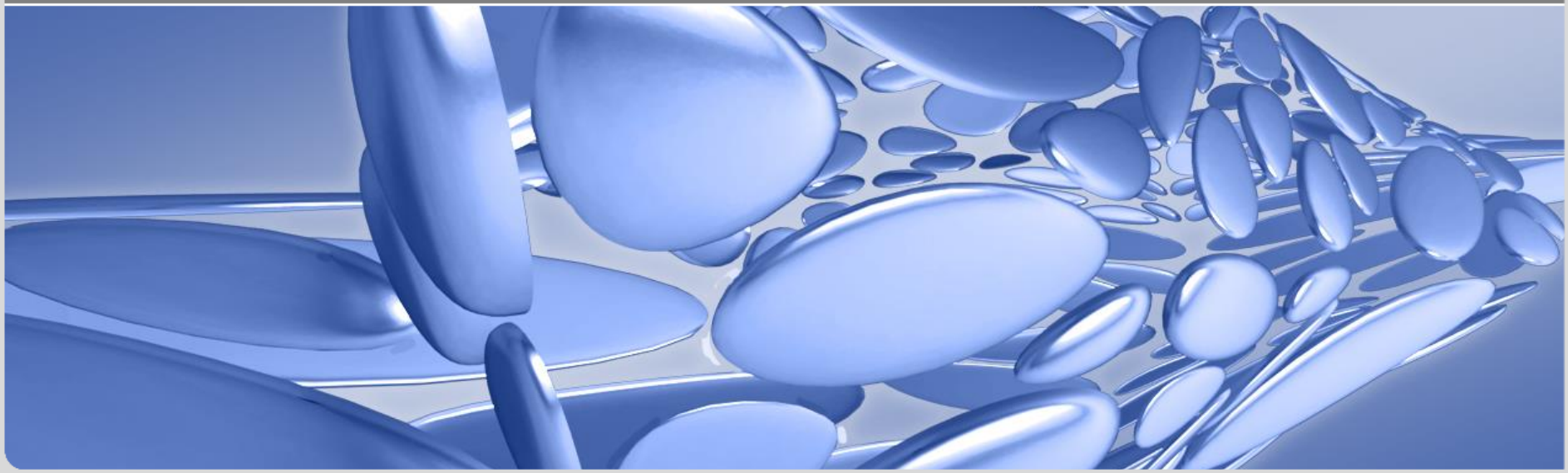
Recent Activities on HV-CMOS Detectors at KIT

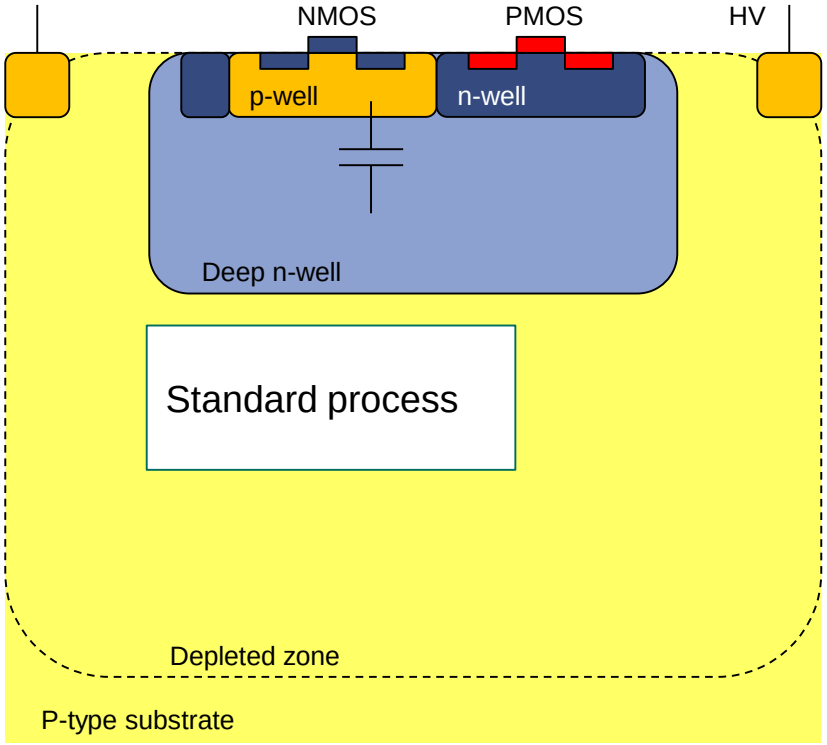
Ivan Peric

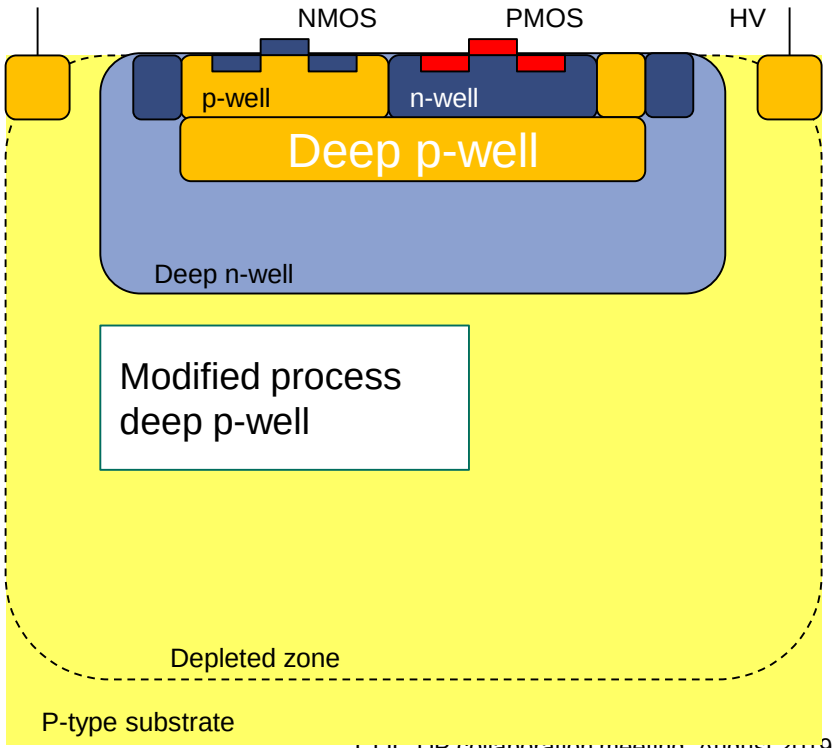


- Introduction of HVCMOS
- Engineering run in aH18 process, experimental results
- New foundry: TSI
- ATLASPIX3
- Planned new engineering run
- CLIC designs
- New ideas: small pixels and reduced detector capacitance

- HVCMOS sensors, for CLIC, Mu3e, ATLAS, COMPASS, LHCB, P2, Belle II (planned)
- Motivation
- For ATLAS HVCMOS sensors promise large cost saving (> 10M), simpler module production, better reliability, less material…
- For Mu3e HVMOS is practically the only option since a high time resolution is needed and material budget is low (0.1% of radiation length/layer - sensor must be 50µm thin)
- HVCMOS = depleted CMOS sensors with large collecting n-well electrode and pixel electronics inside

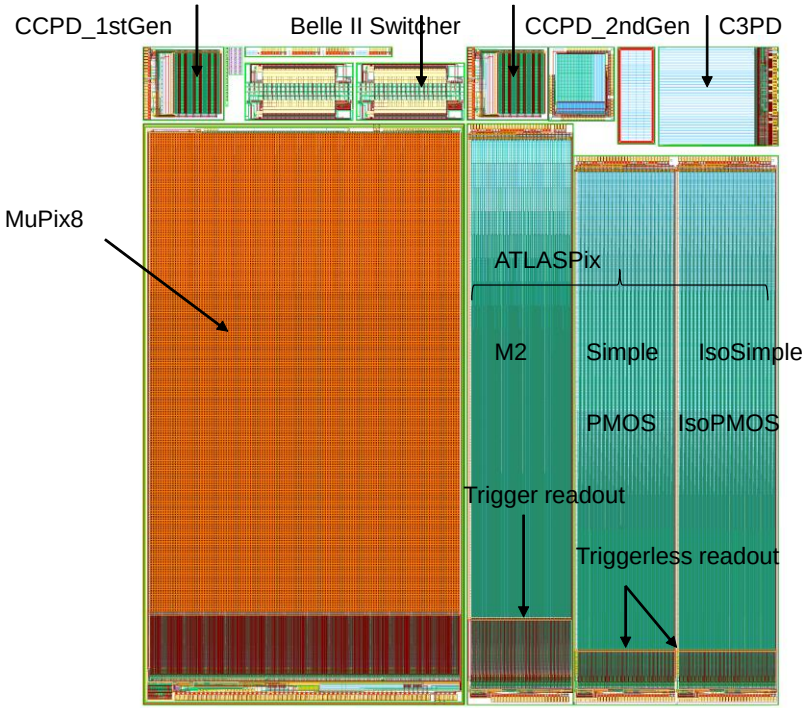
- Pixels are based on floating electronics structure – pixel electronics is placed into a deep n-well.
- Deep-n-well fulfils two tasks:
- 1. Local substrate for electronics (isolated from p-substrate)
- 2. Charge collecting electrode.
- The p-substrate region below the deep n-well is depleted by setting substrate to negative HV. Typical depletion: 30 – 50µm for 80 to 200 Ωcm resistivity. Typical MIP signals are typically >5000e for 200 Ωcm substrate
- The substrate contacts are at the chip surface (undepleted parts of it)
- Largest capacitance from p-well/n-well junction



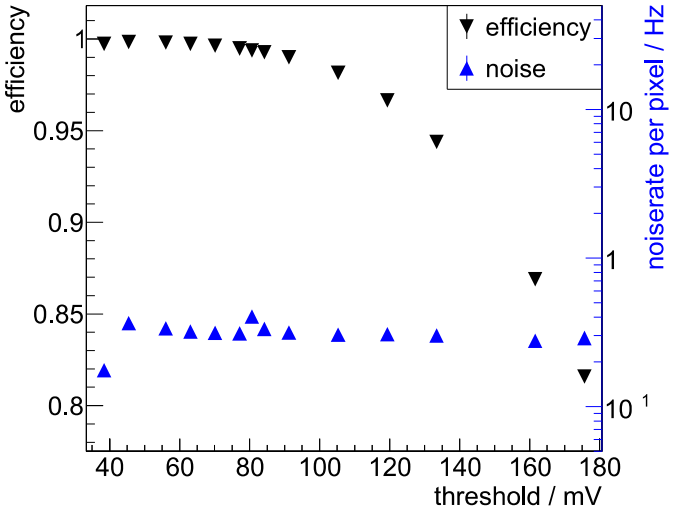


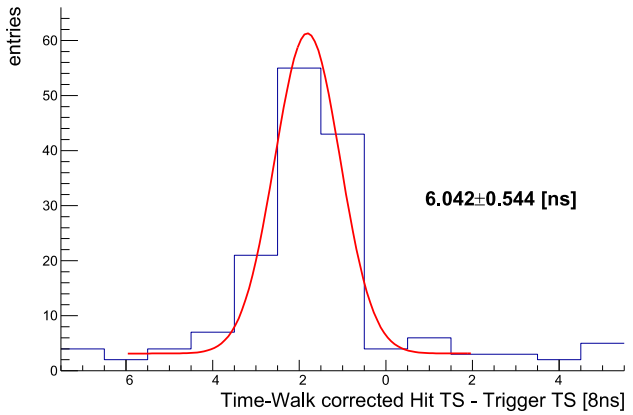
- The milestone in our development was the combined Mu3e and ATLAS run done in AMS aH18 process
- This process is compatible with the originally developed H18 (CMHV7SF) process from IBM (now Global Foundries)
- For this engineering run, AMS modified the process in two aspects – high resistivity substrates were used and the deep-well layer added to isolate the deep n-well from shallow n-well. Not all designs used this option

- We had large MU3E design MUPIX8 – 1cm x 2cm. Pixel size is 80µm x 80µm. Readout is untriggered, zero suppressed
- The chip is working well, detection efficiency is excellent, signal to noise ratio ~50, and time resolution 6ns (RMS) after some corrections

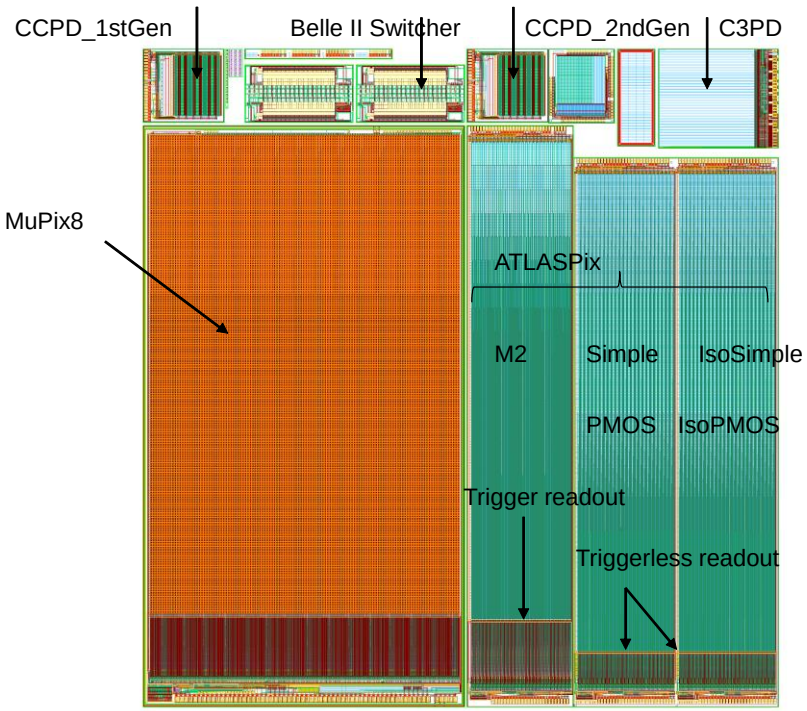


MuPix, ATLASPIX





- We had three ATLAS designs, two with untriggered and one with triggered readout. Pixel sizes are 130µm x 40µm and 60µm x 50µm. Area is about 3 mm x 20 mm
- The chips are also working well. Detection efficiency after irradiations (up to 2 x 10^{15}neq/cm^2) is very good (~99%). Time resolution is down to RMS 8ns.



MuPix, ATLASPIX

Summary of Efficiencies after Irradiation

- no tuning of pixels; ≤ 81/10000 pixel masked

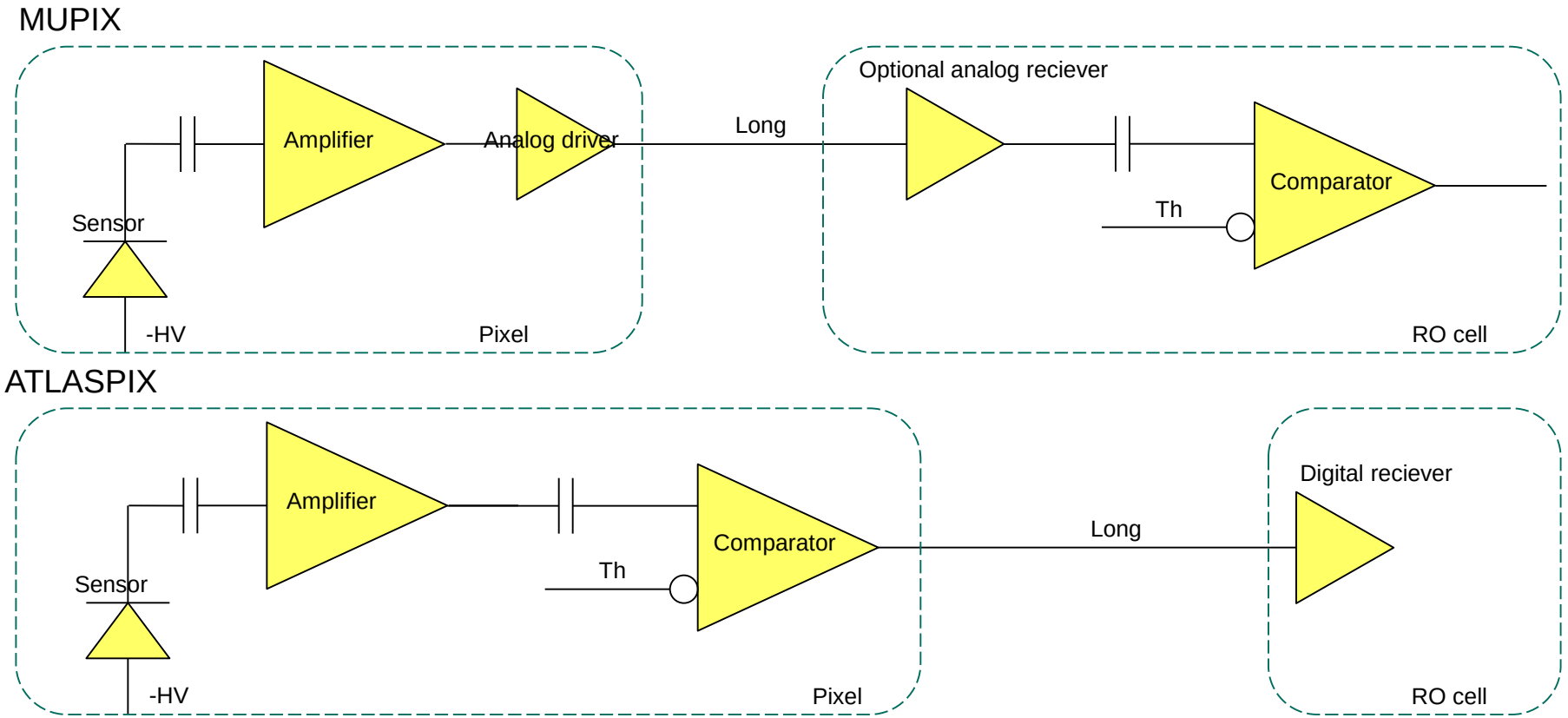
Efficiency$_{40\ Hz}$	sub-strate	thick-ness	bias voltage (#masked pixel)			
fluence (neq/cm^2)	(Ω cm)	(µm)	60 V	70/75 V	80/85 V	90/95 V
n 2e15	80	62	98.5% (81)	98.4% (81)	98.6% (81)	
n 1e15	80	62	99.3% (38)		99.5% (38)	99.5% (39)
n 5e14	80	62	99.5% (19)			
n 2e15	200	100	96.5% (55)		98.7% (60)	98.7% (55)
n 1e15	200	100/725	98.7% (18)	99.4%	99.5%	99.4%
n 5e14	200	100	99.2% (14)			
p 5e14 (50 MRad)	200	100	≥ 99.6% (9)	≥ 99.7% (9)	≥ 99.9% (9)	
p 1e14 (10 MRad biased)	200	725	≥ 99.7%			

≥ means that the 40 Hz/pixel noise limit was not reached

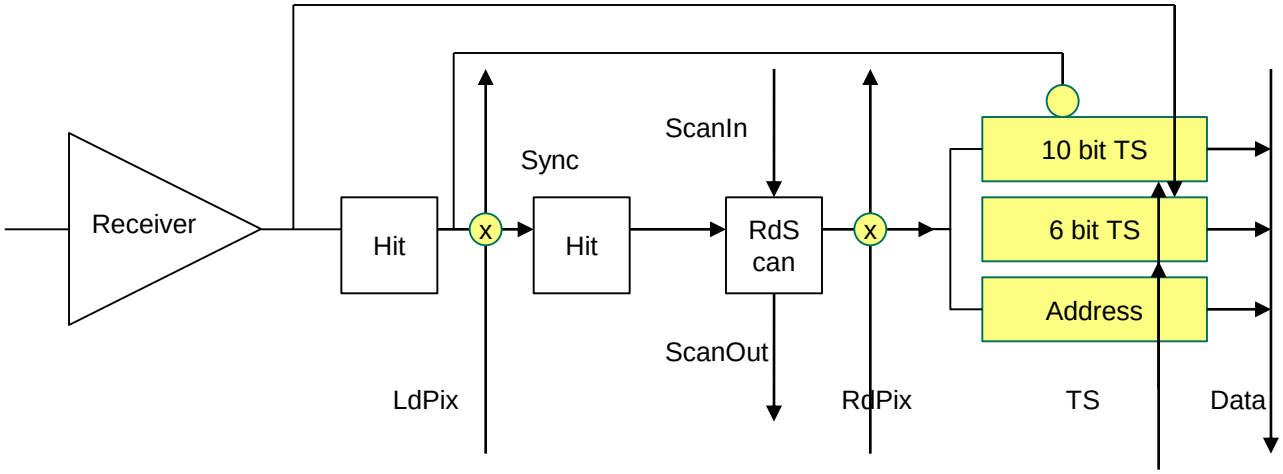
Deep p-well

- Deep p-well was used in one of the ATLASPIX simple chips to isolate CMOS comparator from sensor electrode. Another twin chips used no isolation and used NMOS-based comparator. Both versions of comparator worked good
- The use of deep p-well simplifies the comparator design and allows full swing output which makes the design more robust

- The chips have the following structure:
- Pixel matrix contains pixels. The contain collection electrodes – n-wells – filled with electronics.
- The electronics has CSA, feedback. The comparator with tune circuit is either placed in pixels (ATLASPIX) or on periphery (MUPIX)



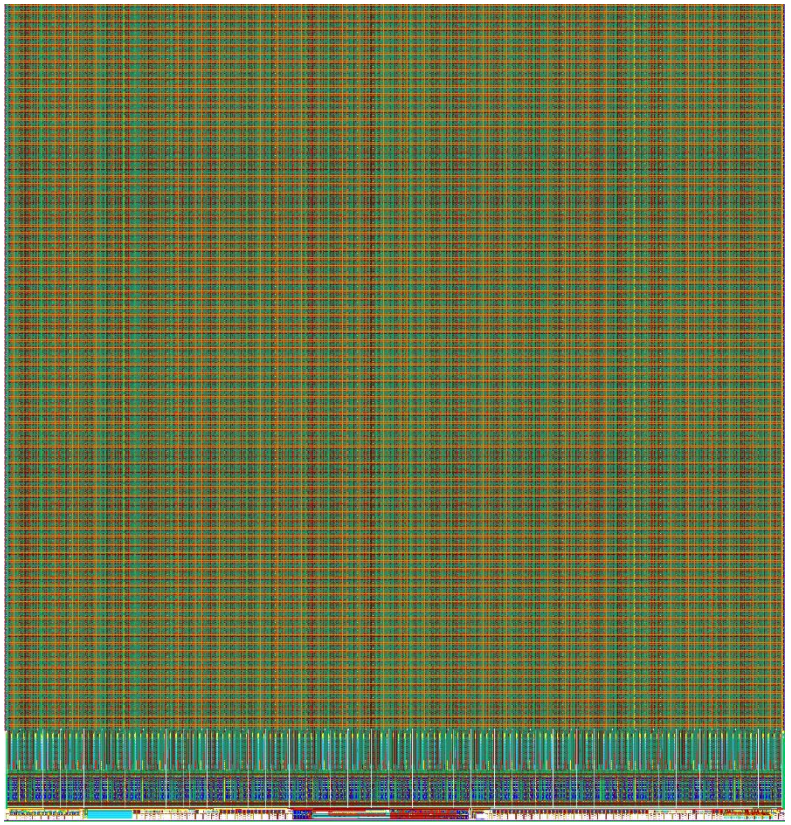
- The periphery contains hit buffers. Every pixel has dedicated hit buffer. They receive time stamps and store them when hit arrives
- A priority logic organizes readout. The hit information is generated in the buffers: address, leading edge and tot time stamp. This information is formatted and sent serially off chip.



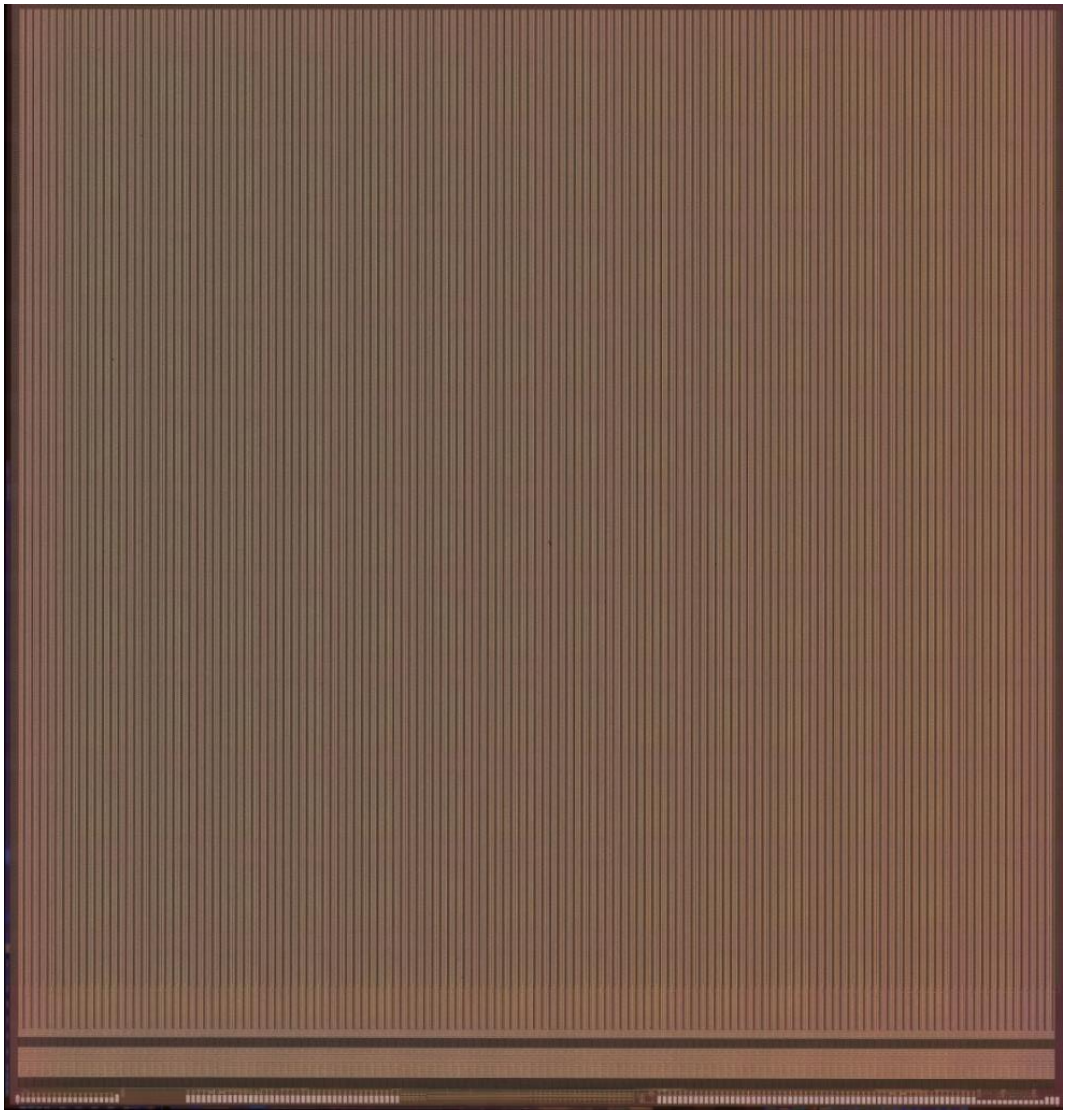
- After these nice results, we received the news from AMS that that production time will be increased
- AMS helped us to fine alternative produces – TSI semiconductors – that offers very similar process that is compatible in terms of design rules and transistor parameters with the H18.
- TSI is very open for process changes, they agreed to use high resistivity wafers and they can make deep p-well for us
- The layouts developed in IBM H18 and AMS aH18 can be used in TSI.
- In contrast to aH18, TSI offers 7 metal layer option which is very useful
- TSI is based in Sacramento, USA
- Engineering run cost about 100k€

- ATLASPIX3 chip designed in TSI process.
- This is a large chip 2 x 2 cm chip with 50µm x 150µm pixels. It has the same signal interface as Rd53 and it can be used to build quad modules for ATLAS
- It has implemented triggered- and, as test feature, untriggered readout

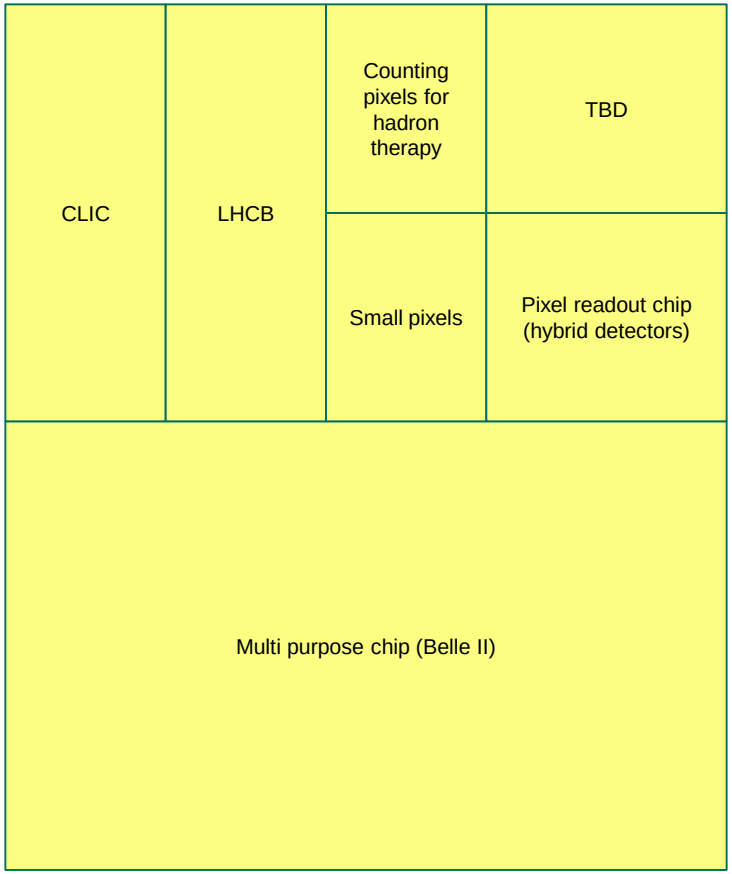
- ATALSPIX3
- HVCMOS sensor for quad module
- Implemented in TSI 180nm HVCMOS technology, licensed IBM/AMS H18 process
- Features and data interface similar as RD53
- Supports triggered readout with trigger latency up to 25µs
- Interface:
- Input CMD line (used for clock generation, L1 triggering with trigger tag, configuring and readback of configuration), like RD53
- Output: Aurora 64b66b, 1.28Gb/s, hit words 32bits, EoE words
- Supports serial powering (only one power supply)
- Size: 20.2mm x 21mm
- Submitted in April 2019



- ATLASPIX3 chip has been produced and we started with first tests this week



- We are planning two more engineering runs in TSI in 2019. A large chip for Mu3e MUPIX10 will be submitted within the first run in October.
- The second run will be shared within many projects and is planned for end of December.



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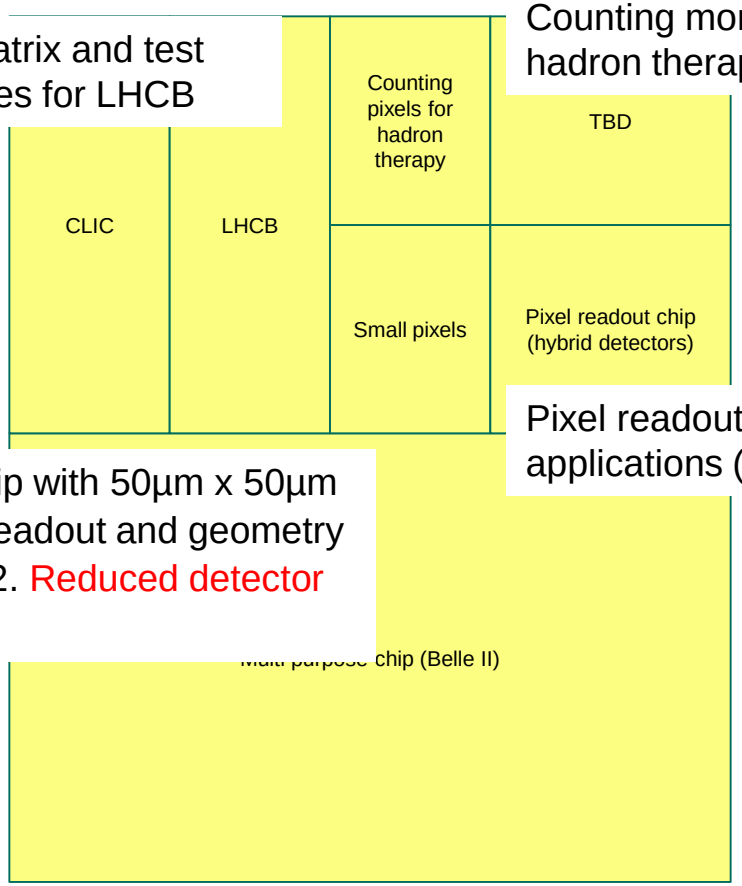
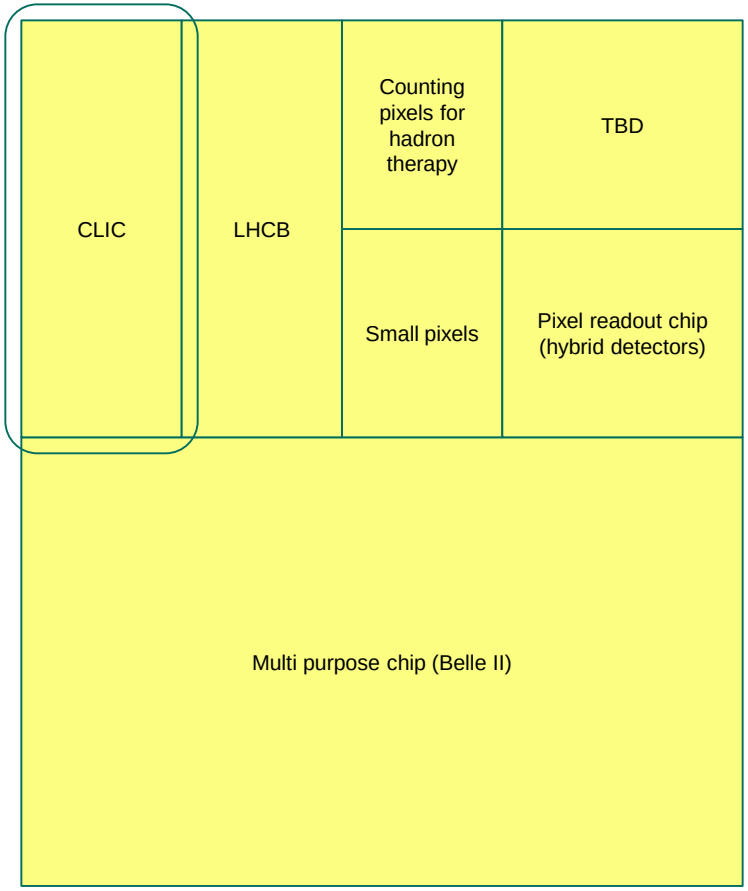
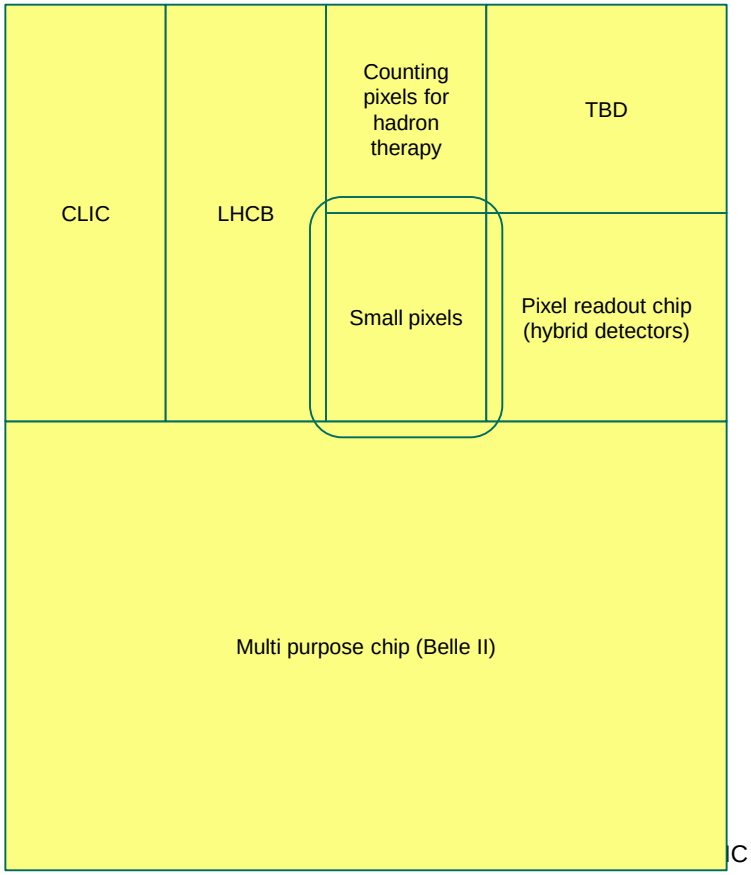


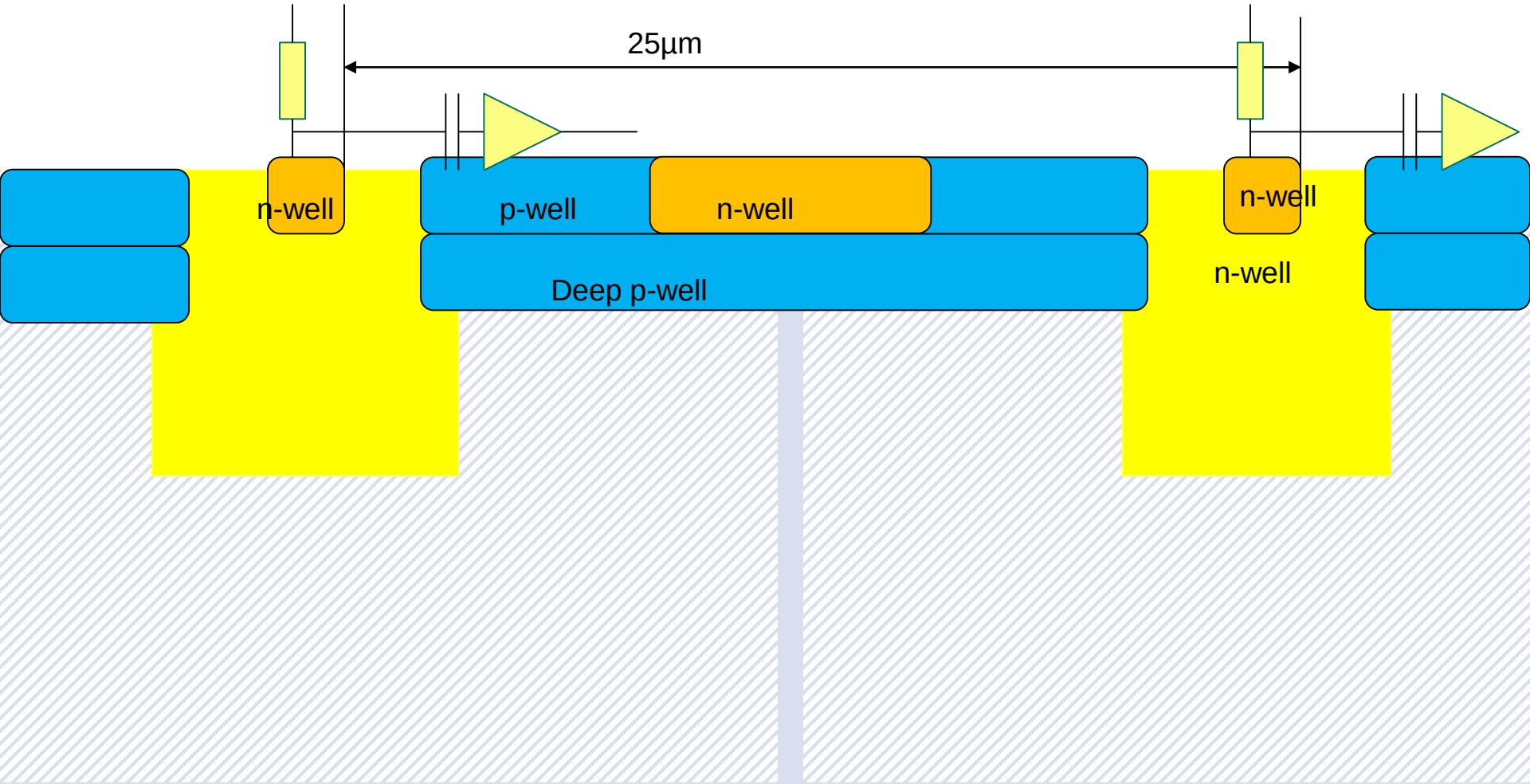
- CLIC design with elongated pixels 25 x 300 um and the readout and periphery similar to ATLASPIX simple
- 10 bit leading edge time stamp and 7 bit TOT time stamp
- The pixels would contain CSA and comparators that would be implemented as CMOS circuits and isolated by deep p-well.



- All previously mentioned sensor would be based on the pixels with large fill factor, the deep n-well filled with electronics
- Since TSI can make deep p-well we can also do low fill factor sensors. We plan following test sensor:
- The pixels would have size of 25µm x 25µm size and in-pixel electronics with CSA, comparators, time measurement and priority based readout.
- 10 bit leading edge and 6 bit TOT time stamp would be implemented per pixel

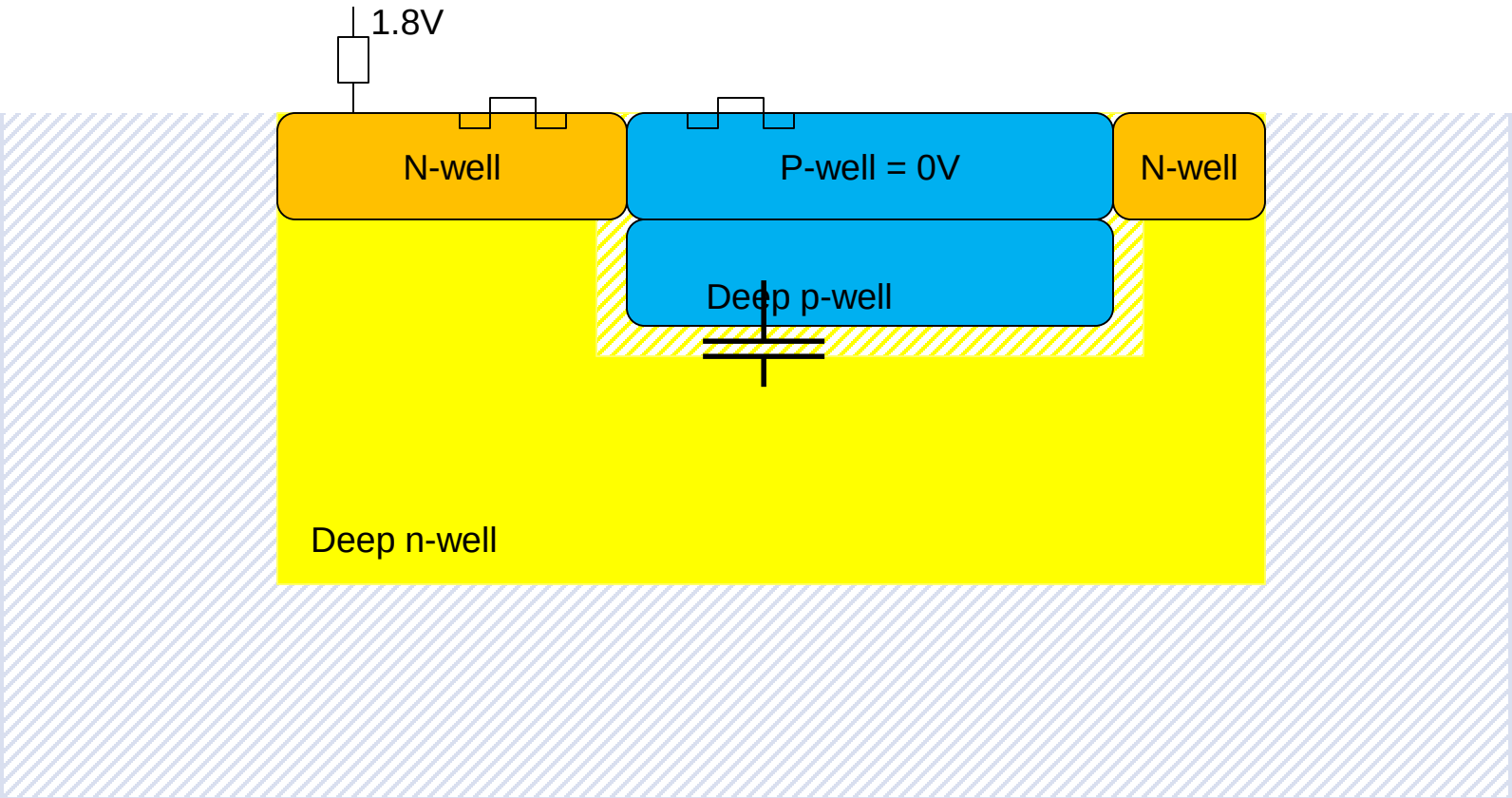


- Matrix with small pixels



P-substrate (200 Ohm cm)

- Improvements of standard HVCMOS stracture are possible
- Idea: reduce capacitance by reverse biasing of deep-pwell to n-well junction



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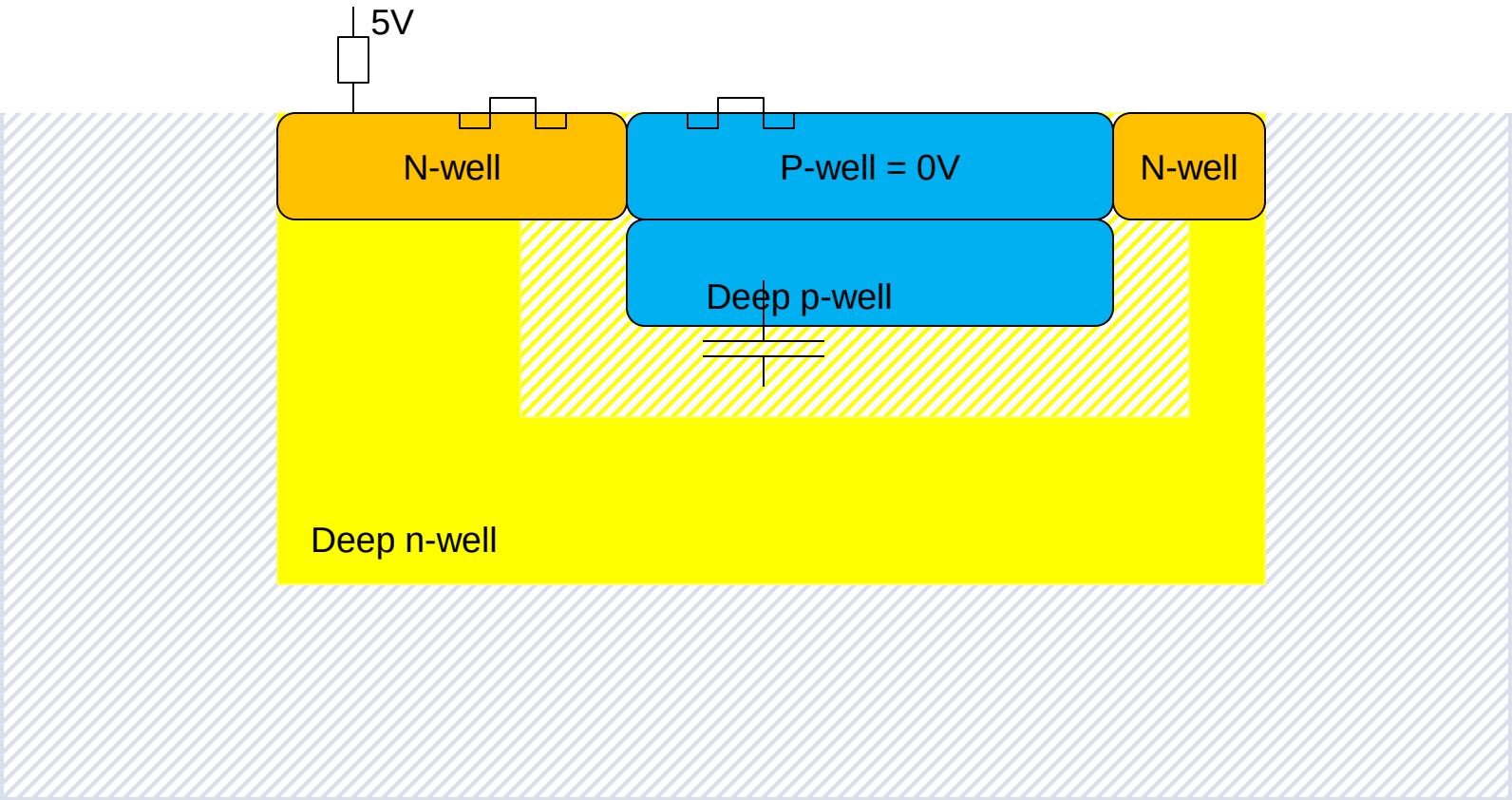

P-substrate (200 Ohm cm)

Summary

- Engineering run in aH18 process, experimental results presented
- New foundry: TSI
- ATLASPIX3 introduced
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- New ideas: small monolithic pixels and reduced detector capacitance

- Thank you