

Position Sensitive Timing Detectors



An overview of a booming field

Silicon sensors as accurate timing detectors

Up to about 10 years ago, silicon sensors were not considered mainstream MIP timing detectors

Presently, they are considered the most likely (only?) solution for 4D trackers

I will present this change in the presentation

Two inspiring early papers

IEEE Transactions on Nuclear Science, Vol. NS-29, No. 3, June 1982

L B L - 14145

FAST TIMING METHODS FOR SEMICONDUCTOR DETECTORS

Helmuth Spieler

GSI - Gesellschaft fuer Schwerionenforschung
6100 Darmstadt, West Germany

and

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University of California
Berkeley California 94720 U.S.A.

404

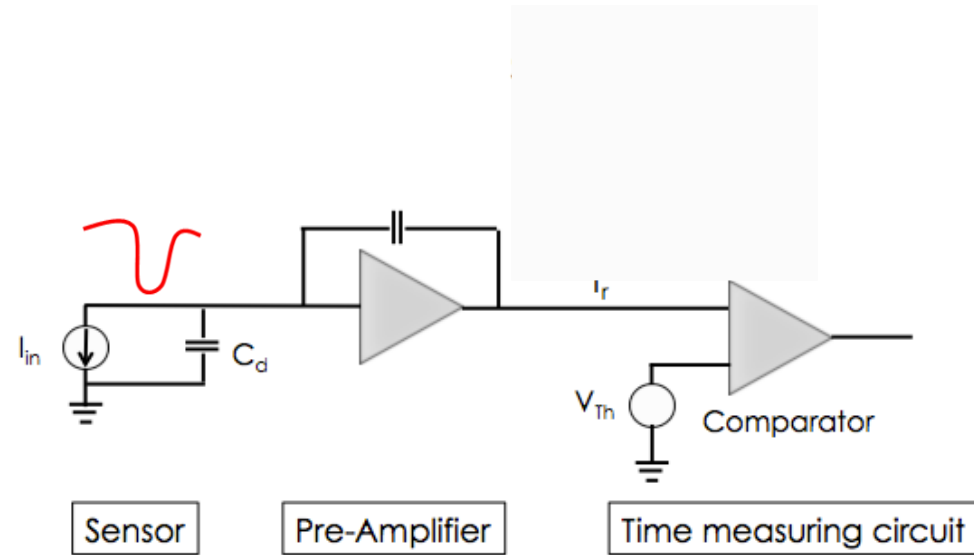
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 2, APRIL 2011

Increased Speed: 3D Silicon Sensors; Fast Current Amplifiers

Sherwood Parker, Angela Kok, Christopher Kenney, Pierre Jarron, Jasmine Hasi, Matthieu Despeisse,
Cinzia Da Via, and Giovanni Anelli

Silicon time-tagging detector

- Sensors produce a current pulse
- The read-out measure the time of arrival



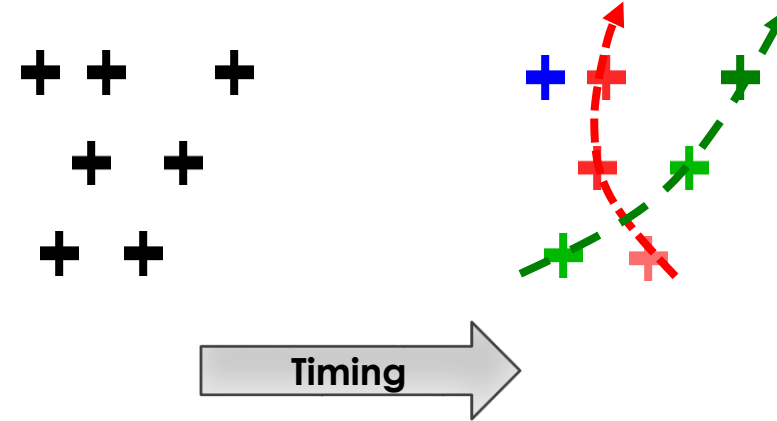
Sensors and read-out are two parts of a single object, sometimes even on the same substrate (monolithic option).

Sensors and electronics succeed (or eventually fail) together

In “timing circuits”, things can go wrong very rapidly (quote stolen from a chip designer)
=> this is not a simple evolution of what we know how to do.

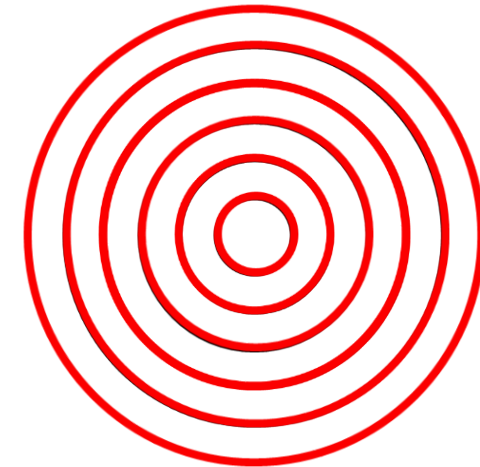
Timing layers and 4D tracking

By “**4D tracking**” we mean the process of assigning a space and a time coordinate to a hit.



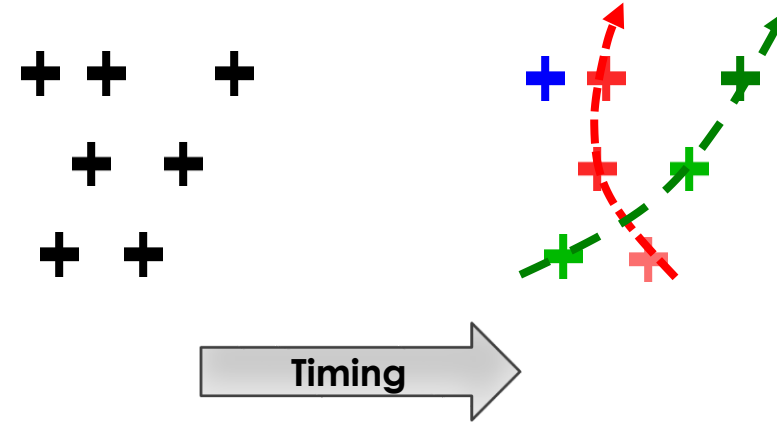
Timing can be available at different levels of the event reconstruction:

- 1) Timing in a single point (timing layer ATLAS,CMS)
- 2) Timing at some points along the track
- 3) Timing at each point along the track



Timing layers and 4D tracking

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More timing coordinates yields to more performing systems, but require a much more complex read-out system. Some projects will be perfectly fine with having a smaller set of timing points

Systems designed for accurate timing

In a large detector system, good temporal resolution has many parts:

- 1. The sensor**
- 2. The design of the ASIC:**
 - Technology (process, BW..)
 - Money
 - Power available
- 2. Detector design:**
 - Cabling, module quality, noise rejection
 - quality of power supply etc
- 3. Infrastructure:**
 - Clock distribution
 - Cooling
 - Data transfer

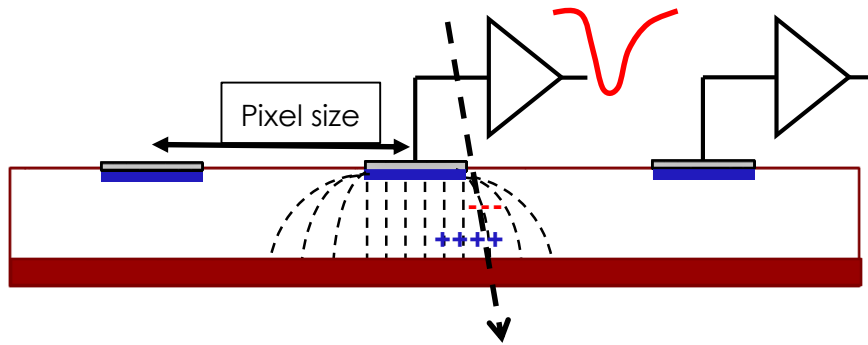
A detector for timing needs very strong R&Ds in many additional aspects

(these challenges are now faced by the ATLAS and CMS timing layers)

Position sensitive: single and multi pixels read-out

Single pixel

where the charge is collected by one pixel

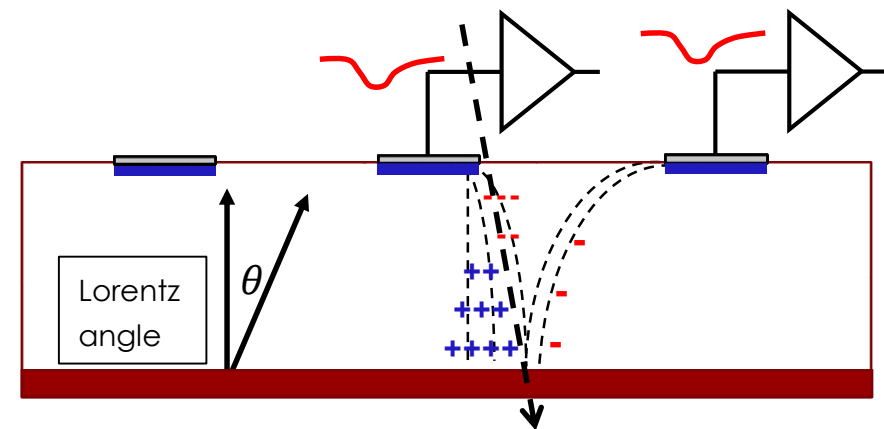


$$\sigma_x = k \frac{\text{pitch}}{\sqrt{12}}, k \sim 0.5 - 1$$

- σ_x depend on the pixel size
pixel = 100 μm \rightarrow $\sigma_x = 20 \mu\text{m}$

Multi pixels

where the charge is collected by a few pixels



$$x_i = \frac{A_i x_i}{\sum_1^2 A_l x_l}$$

- $\sigma_x \ll$ pixel size
- Sensors have to be thick to maintain efficiency
- Need B field (or floating electrodes)

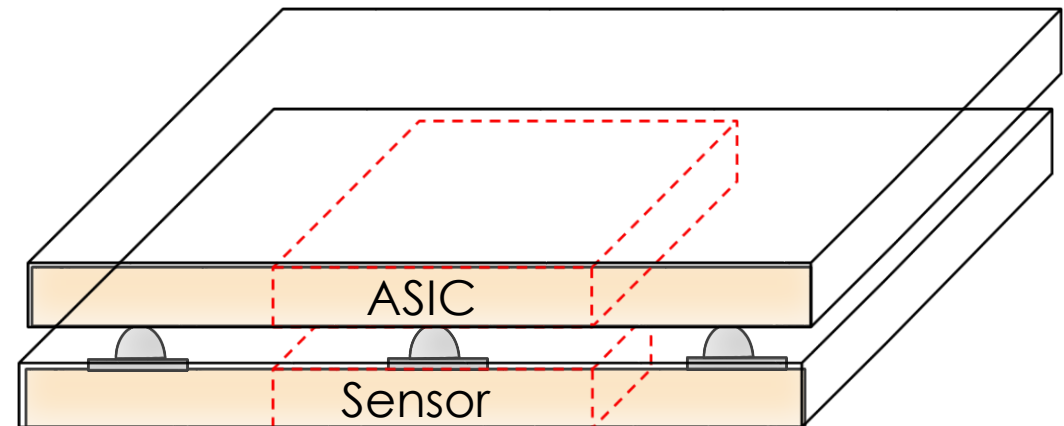
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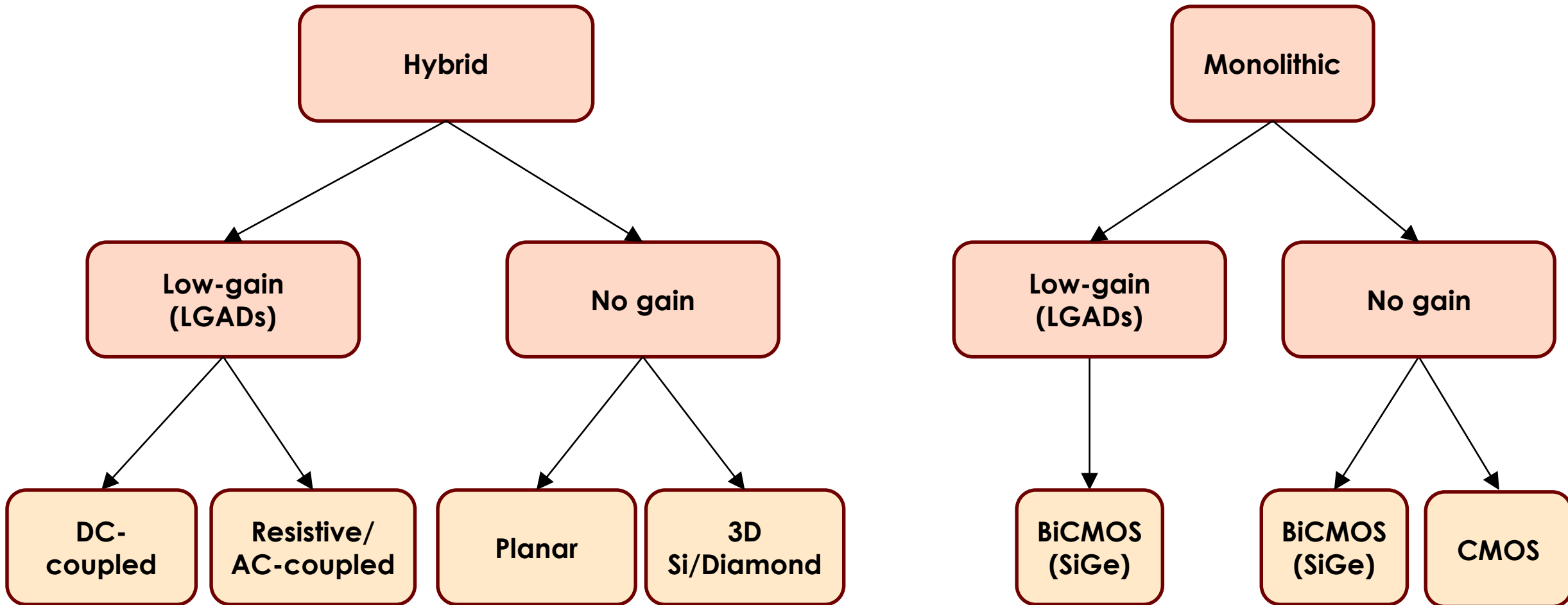
In single pixel architecture, the pixel size determines the position accuracy

This fact has tumultuous consequences on the design of the electronics and on the power consumption

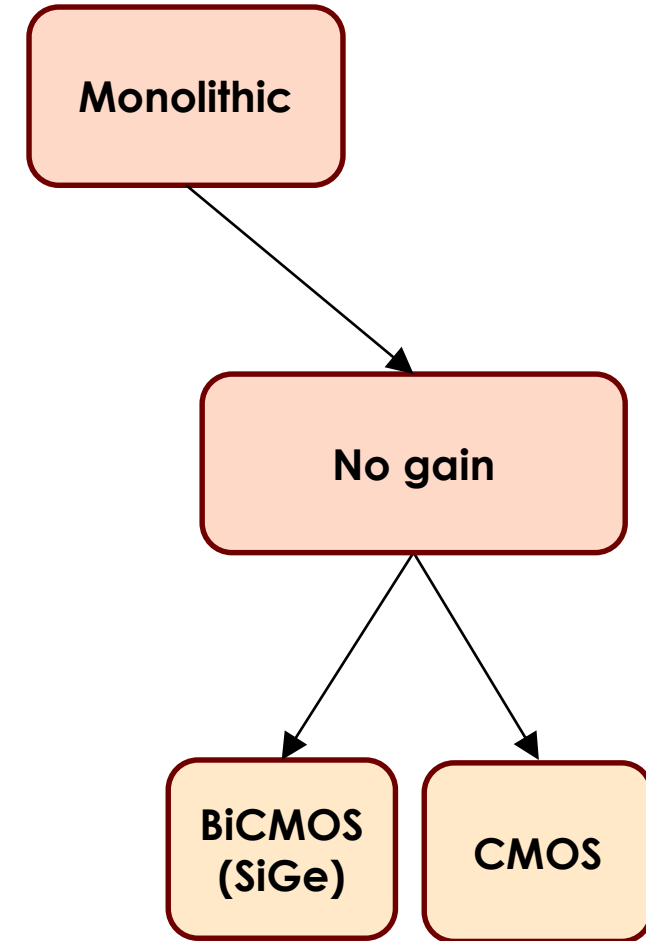
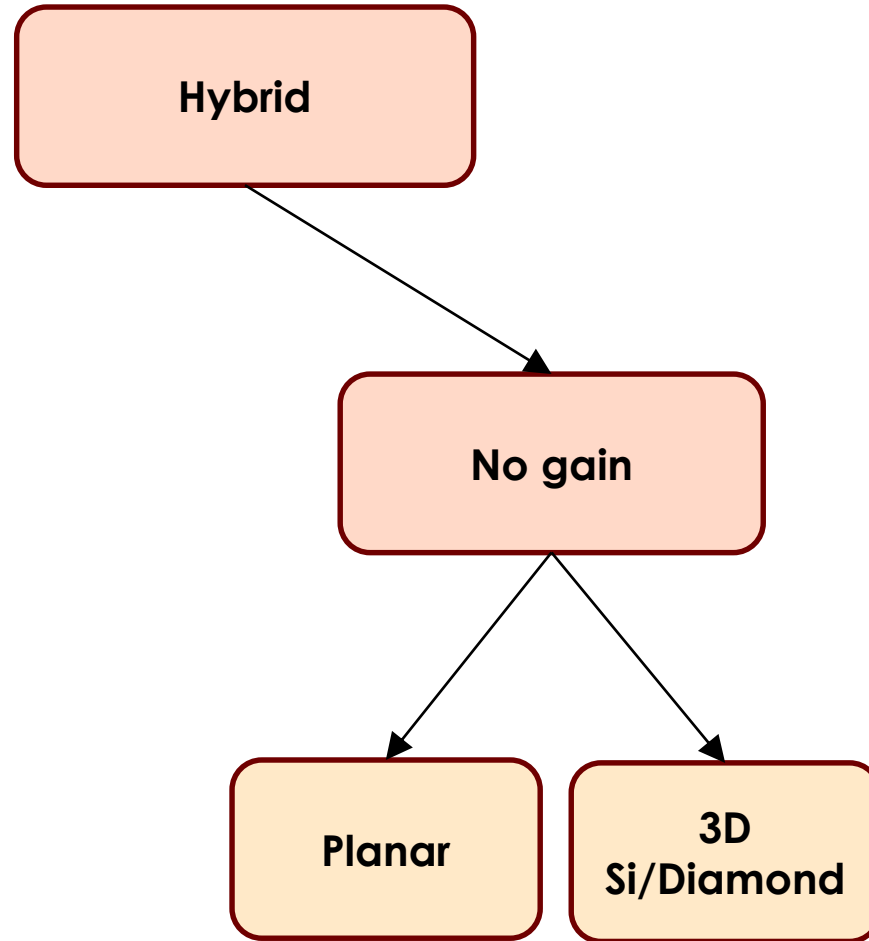


Presently explored options

The present R&D in position sensitive timing detectors shows the same variety that is present in standard silicon sensors. In the following, I will cover a few examples from this chart.



Presently explored options: without internal gain



Presently explored options: without internal gain

Hybrid

Two possible options:

- Column
- Trenches
- The amount of charge is controlled by the sensor thickness (~1-2 fC)

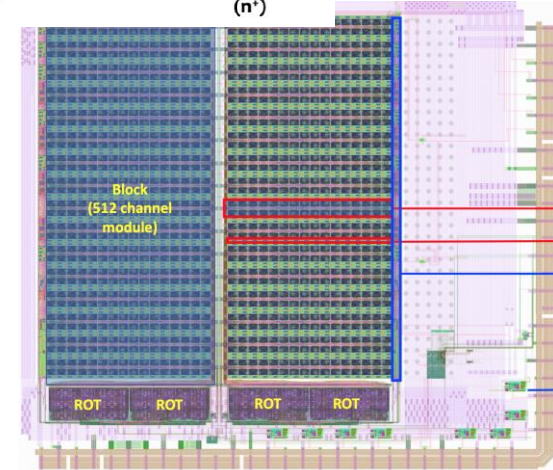
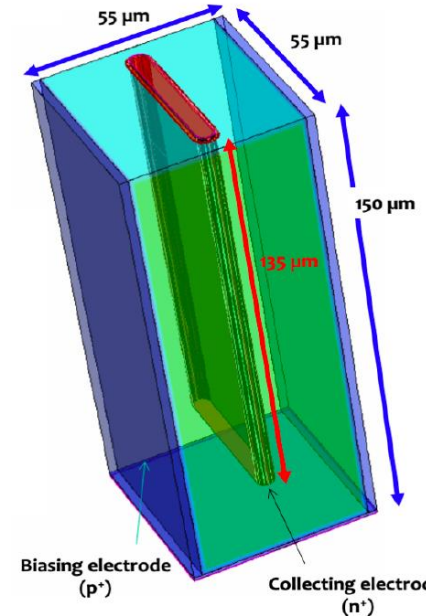
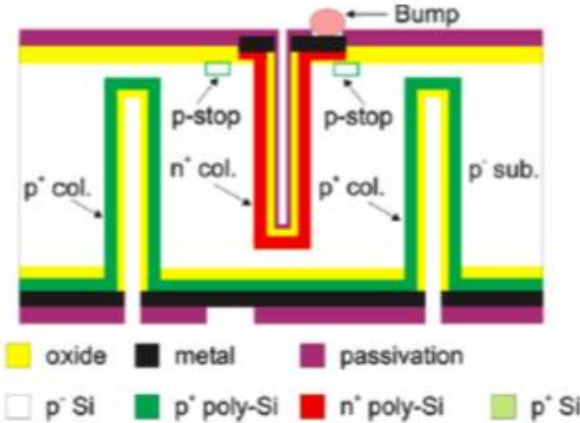
No gain

Both requires small pixels to achieve good temporal precision

==> very good position resolution

3D
Si/Diamond

Schematic Cross Section

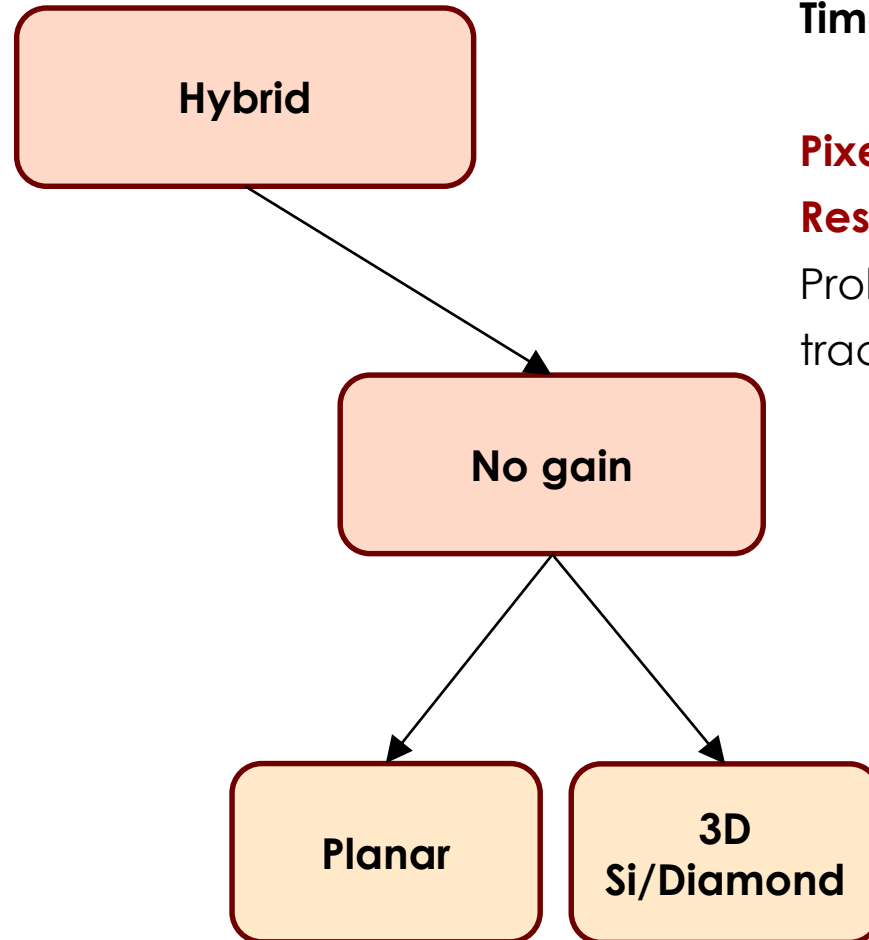


Timespot1: 28 nm ASIC

Pixels size = 55 μm

Resolution ~ 30 ps for single channel

Presently explored options: without internal gain



The ASIC Timepix family

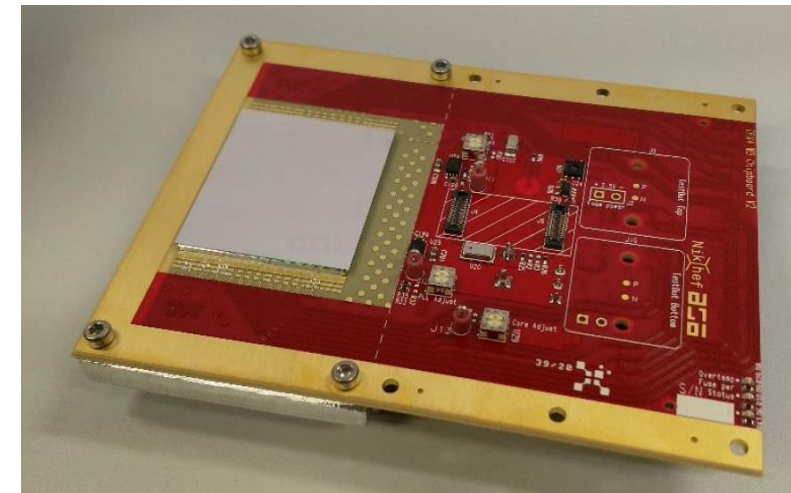
Last addition:

Timepix4: 65 nm ASIC, 512 x 448 pixels

Pixels size = 55 μm

Resolution in line with expectations ~ 150 ps RMS

Probably the best example so far of a full 4D tracking system

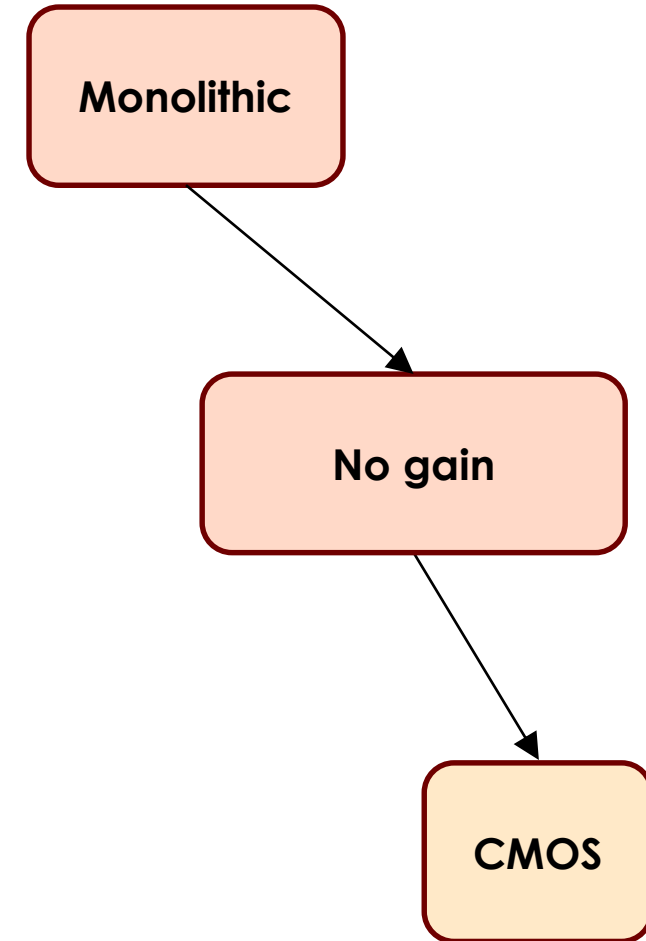
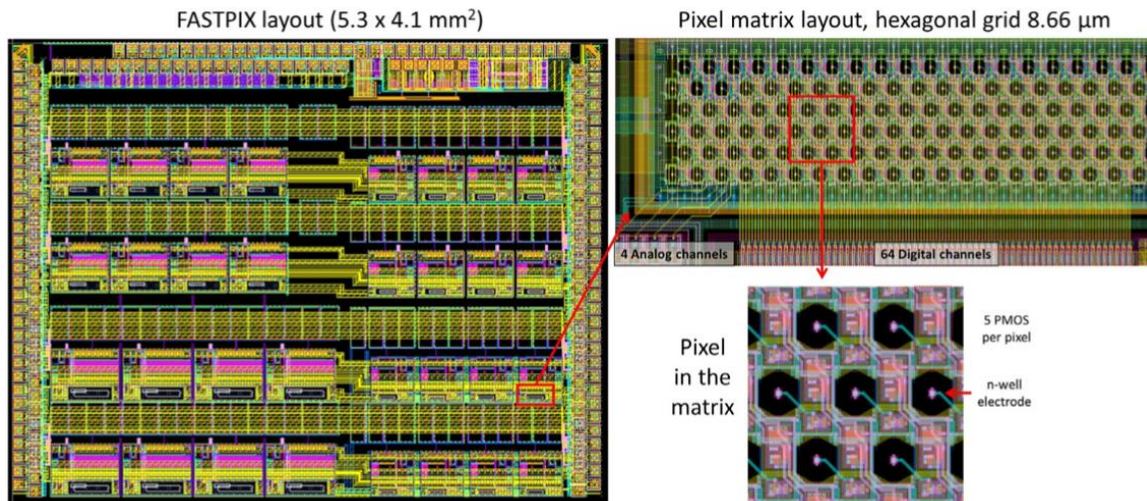


Presently explored options: without internal gain

FASTPIX is a CMOS monolith project aiming at combining temporal stamping with excellent position precision

Resolution of about ~ 100 ps,

Very small pixels



Presently explored options: without internal gain

MonPicoAD project

Exploit SiGe performances

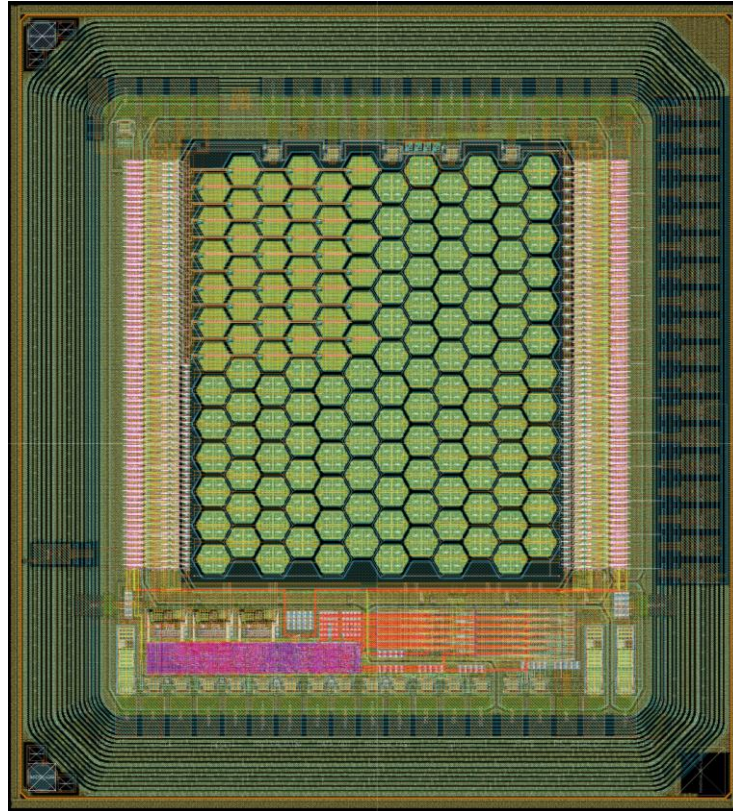
Exagonal pads, $65\ \mu\text{m}$

About $25\ \mu\text{m}$ depletion

Thinned to $60\ \mu\text{m}$

Resolution of about $\sim 38\ \text{ps}$,

Very small pixels

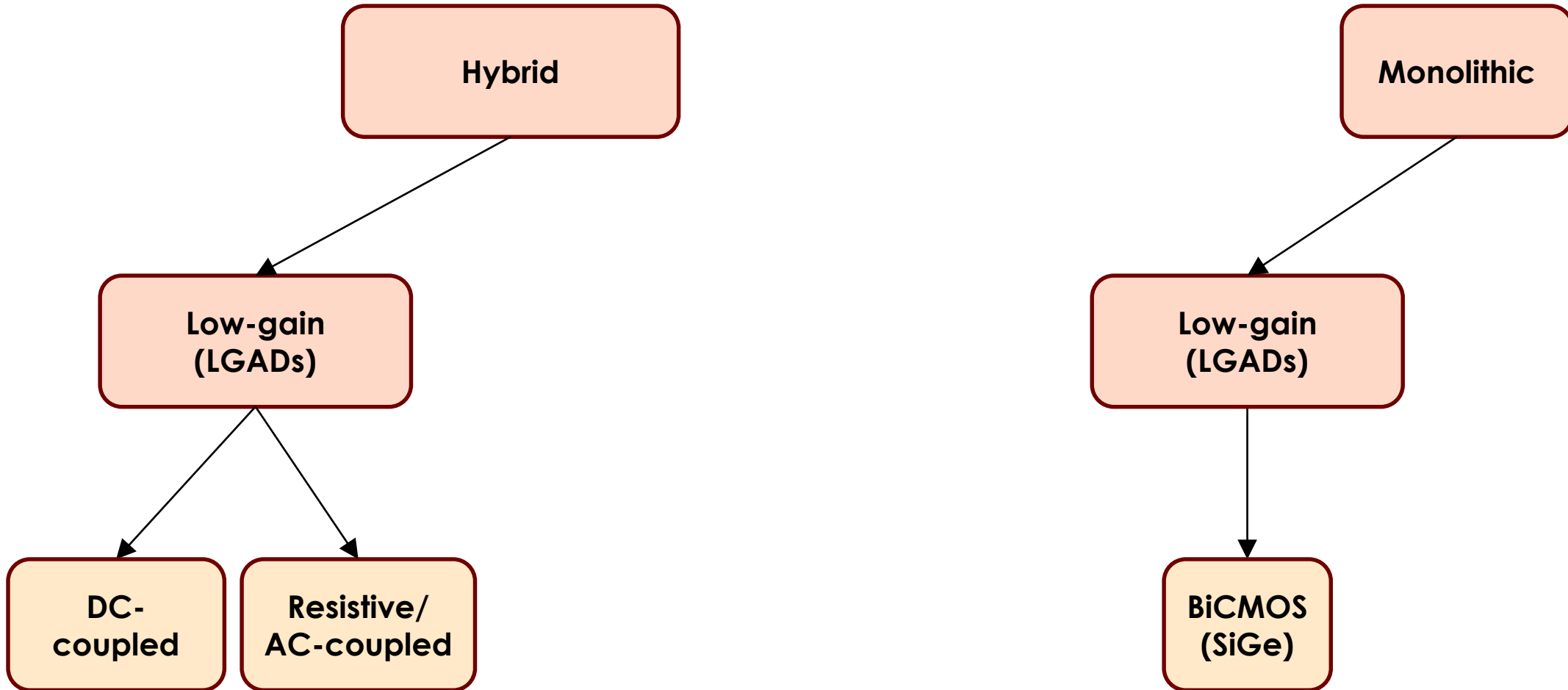


Monolithic

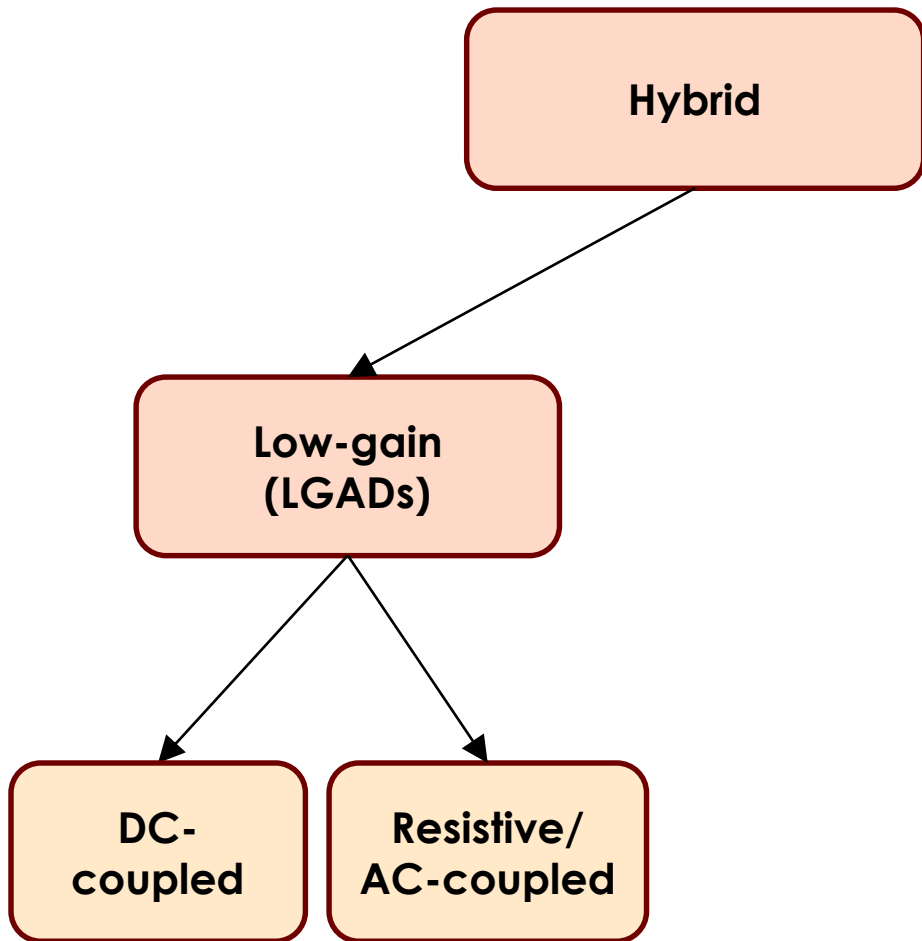
No gain

BiCMOS
(SiGe)

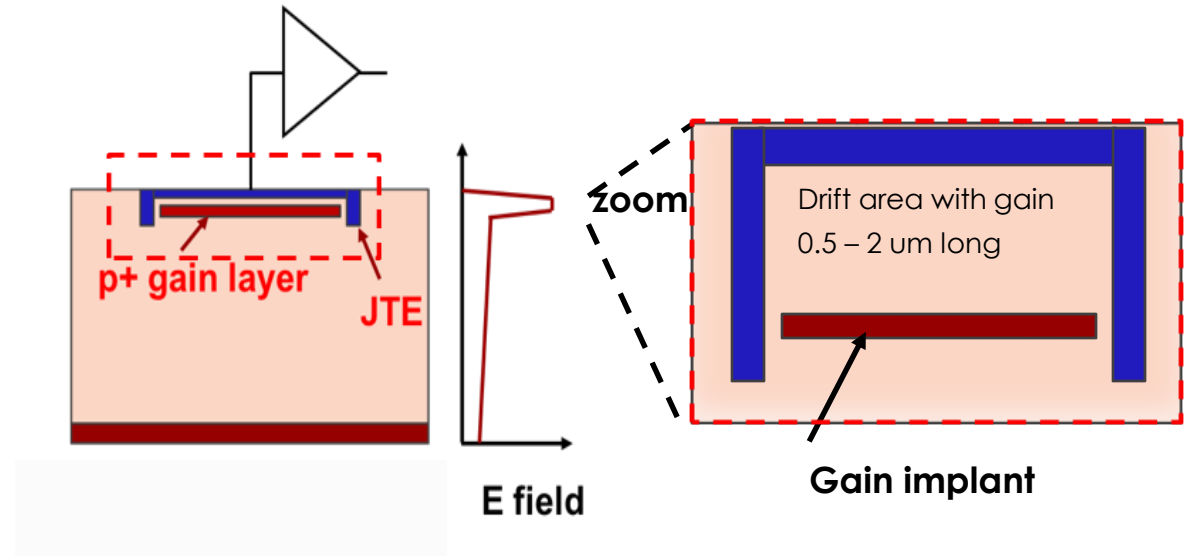
Presently explored options: with internal gain



Presently explored options: with internal gain



First design innovation: low-gain avalanche diodes



- The low-gain mechanism, obtained with a moderately doped p-implant, is the defining feature of the design.
- The low gain allows segmenting and keeping the shot noise below the electronic noise, since the leakage current is low.

Low gain minimizes jitter, it is the key ingredient to good temporal resolution

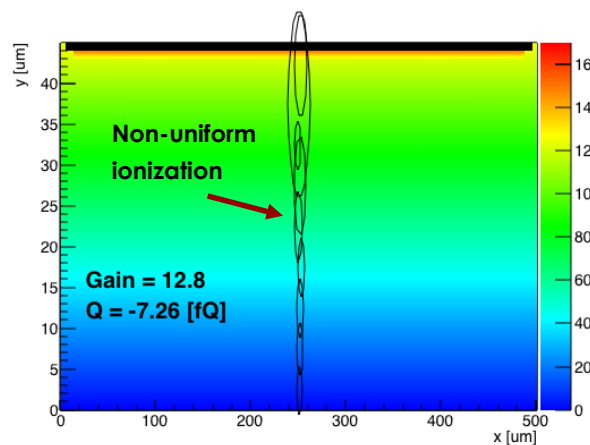
UFSD temporal resolution limit: non uniform ionization

$$\sigma_t^2 = \left(\frac{\text{Noise}}{dV/dt} \right)^2 + (\Delta \text{ionization})^2$$

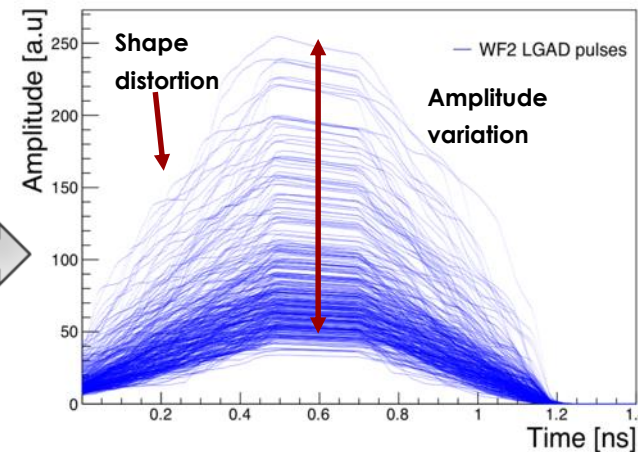
Large dV/dt ,
 → small jitter

Non uniform ionization:

Physical limit of UFSD sensors



Simulation of signals in 50-um LGAD

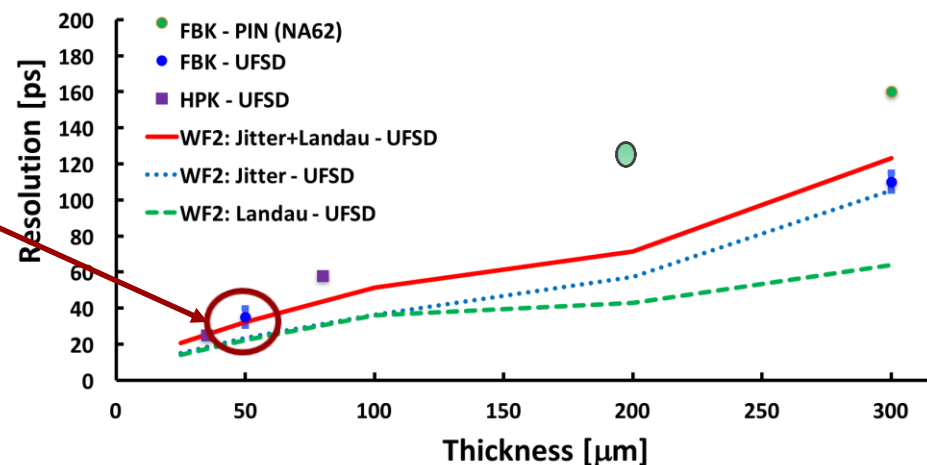


There are now hundreds of measurements
 on 45-55 μm -thick UFSDs

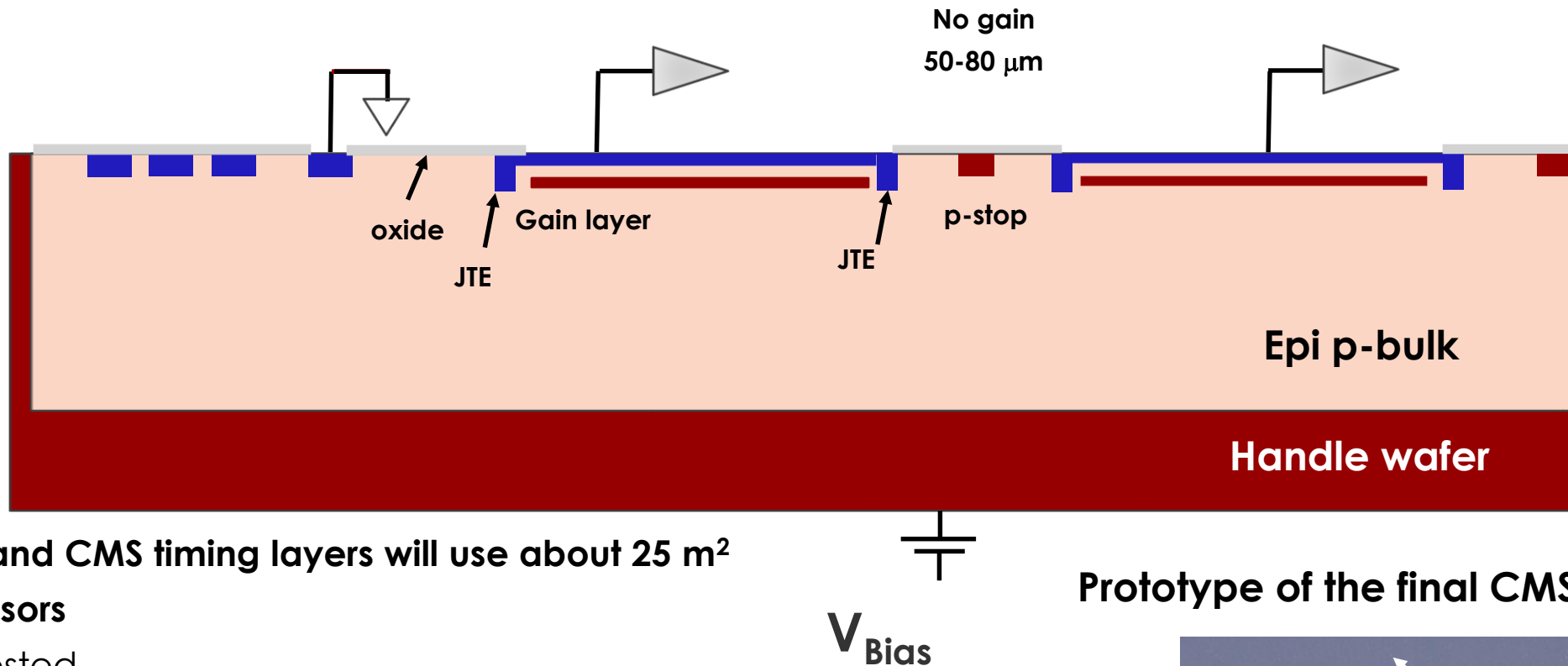
(Ultra Fast Silicon Detector: LGAD optimized for timing)

→ Current sensor choice for the ATLAS and
 CMS timing layers

Comparison WF2 Simulation - Data
 Band bars show variation with temperature ($T = -20\text{C} - 20\text{C}$), and gain ($G = 20 - 30$)



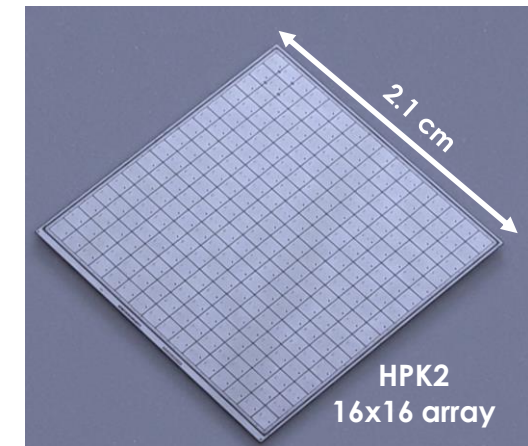
State-of-the-art: sensors for ATLAS and CMS



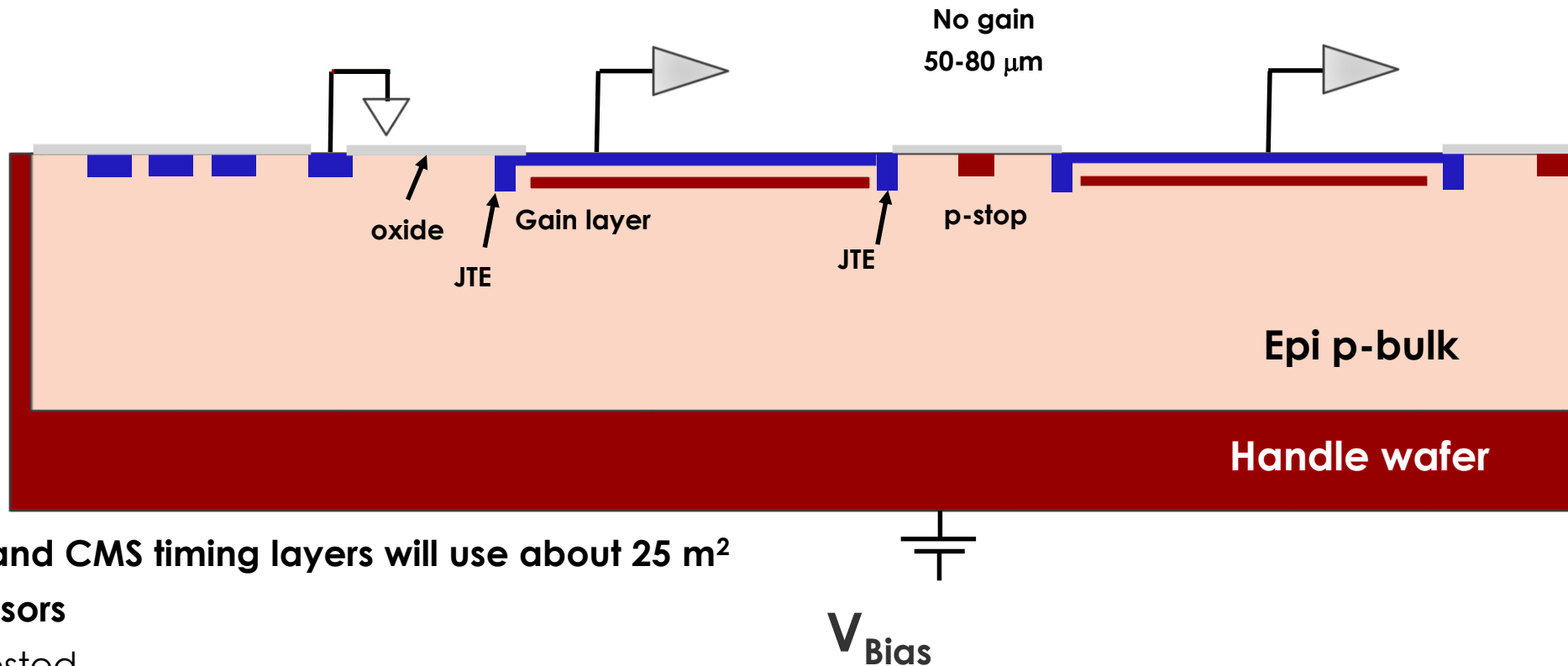
- The ATLAS and CMS timing layers will use about 25 m² of UFSD sensors

- Very well tested
- Will be used up to $\sim 2 \text{ E}15 \text{ n}_{eq}/\text{cm}^2$
- Gain \sim up to 40 when new \implies up to 20 fC
- Signal duration $\sim 1 \text{ ns}$
- Low noise
- Rate $\sim 50\text{-}100 \text{ MHz}$
- Excellent production uniformity

Prototype of the final CMS sensor



State-of-the-art: sensors for ATLAS and CMS



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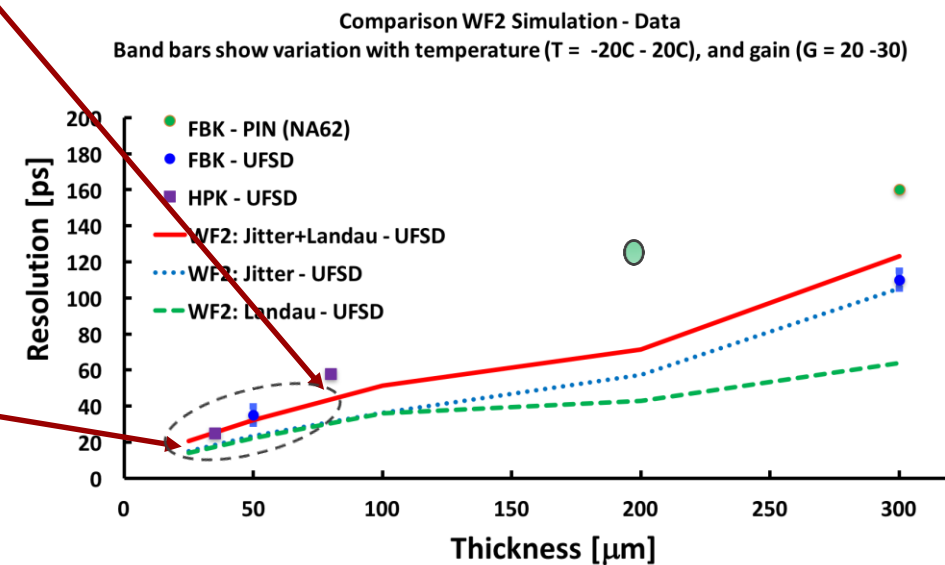
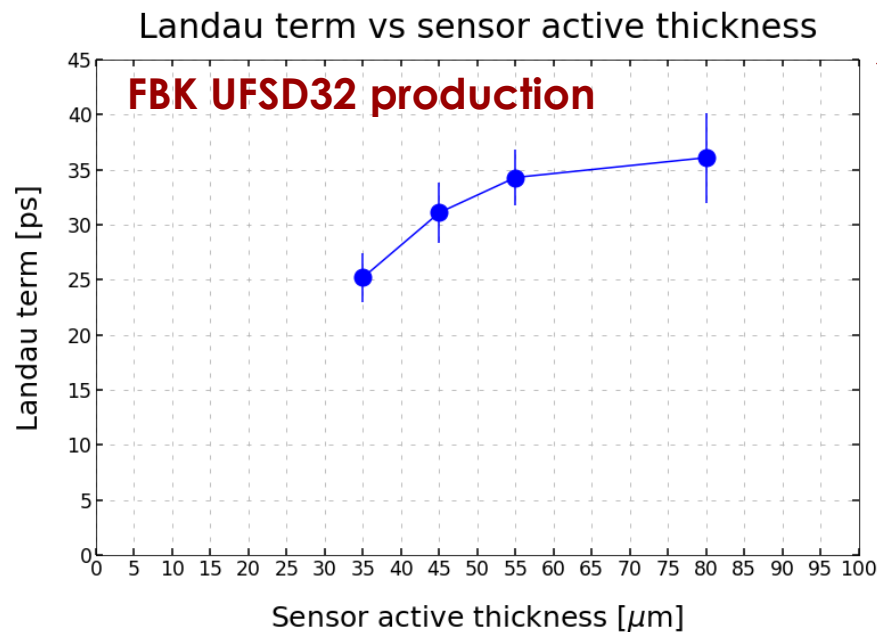
Shortcomings:

- **Large no-gain area between pads \implies not suitable for 4D tracking**
- **Intrinsic temporal resolution $\sim 25\text{-}30 \text{ ps}$ due to Landau noise**
- **Poor spatial resolution**

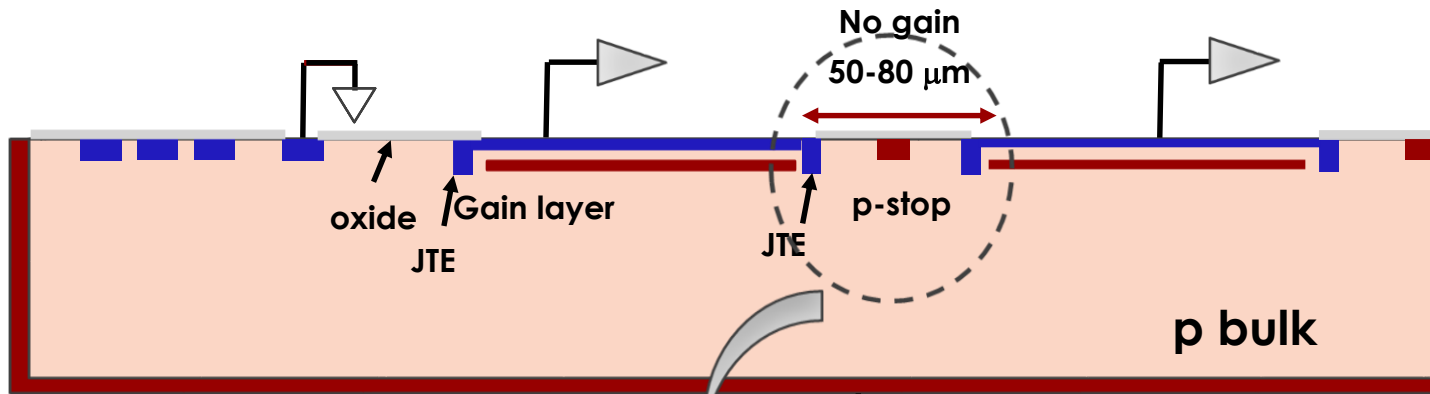
UFSD temporal resolution in thinner sensors

UFSD minimum temporal resolution improves in thinner sensors: reasonable to expect 10-20 ps for 10-20 μm thick sensors.

Be aware: very difficult to do timing with small signals...



LGAD Trench Isolated: enabling small UFSD pixels

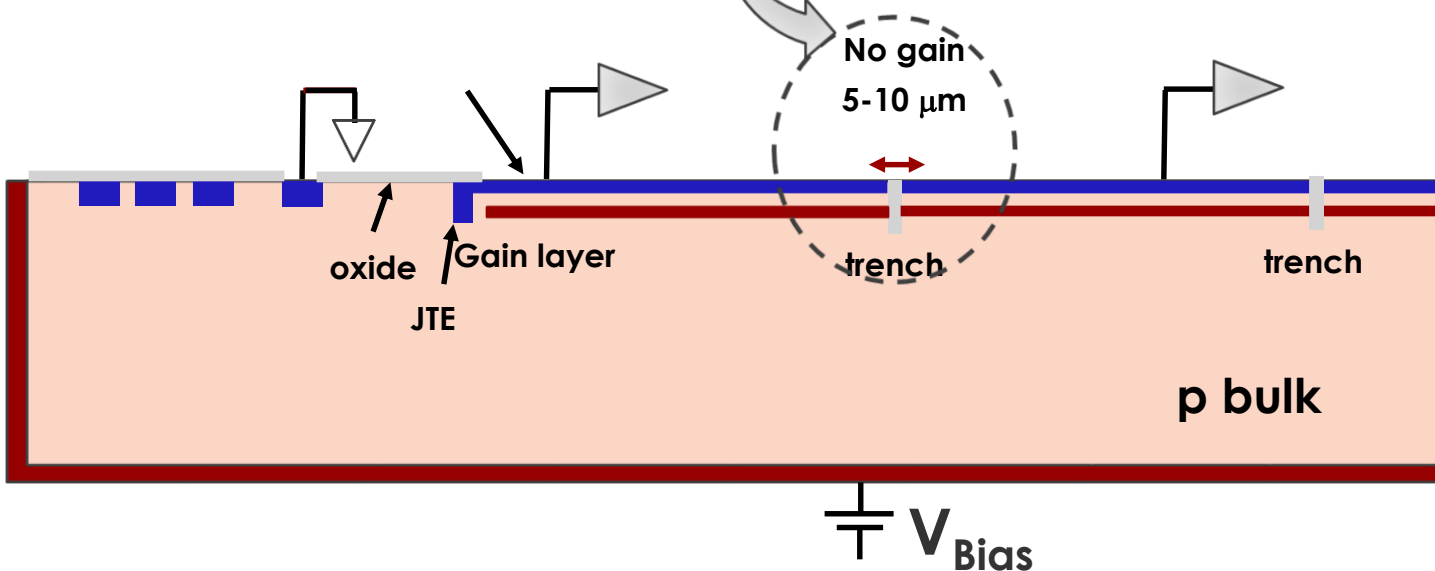


No-gain region $\sim 50\text{-}80 \mu\text{m}$
 → cannot use for small pixels

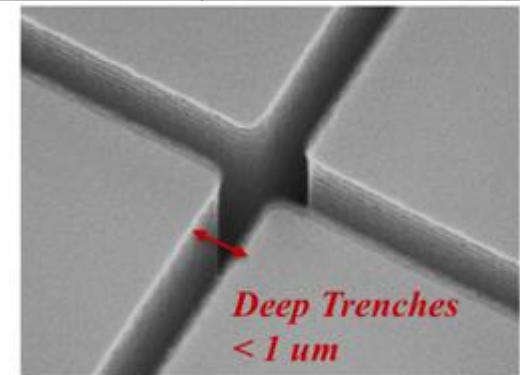
Solution: use trenches for pad isolation
 → No-gain region $\sim 0 - 10 \mu\text{m}$

RD50-TI production

Interpad design	Interpad distance [μm]
V1_1TR	2.7 ± 0.2
V2_1TR	6.5 ± 0.2
V3_1TR	7.9 ± 0.1
V4_1TR	10.6 ± 0.2
V2_2TR	8.9 ± 0.2
V3_2TR	10.3 ± 0.1



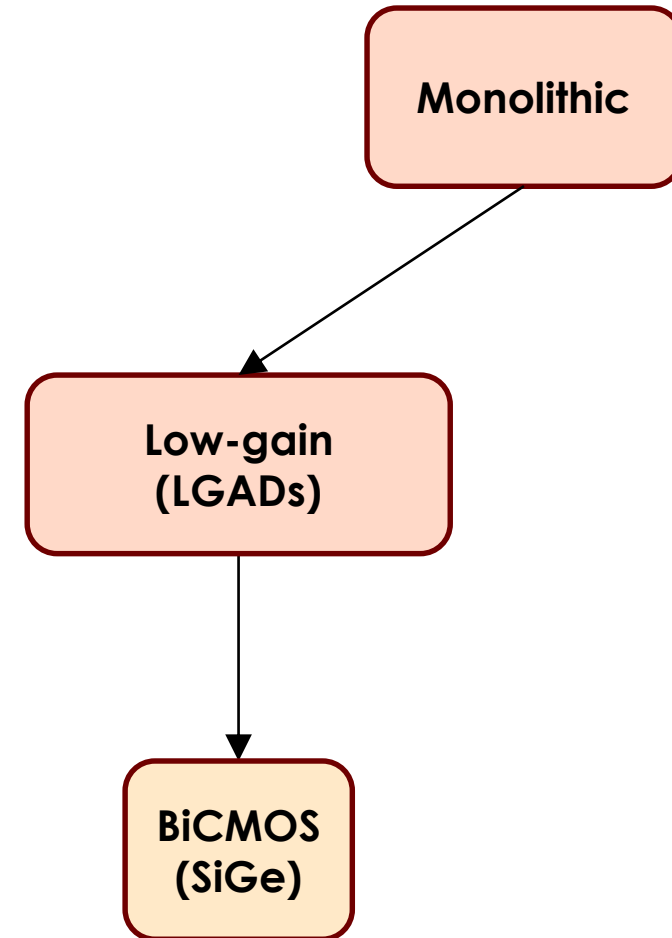
→ The R&D to achieve small pixels is clear



Presently explored options: with internal gain

This is a very powerful research path pursued by the **“Monolith” project**.

Looking forward to the first results
See talk by M. Munker on Monday



Position Sensitive Timing detectors

- **"Position sensitive"** is a much more difficult task than simply **"silicon timing detectors"**
- Good position resolution requires small pixels
- A lot of small pixels consume too much power

- **Consider the ATLAS-CMS timing layer:**
 - Pixel size: 1.3 x 1.3 mm²
 - ~ 40 ps precision
 - **Power: 0.3 W/cm²**

- **TimeSpot1 ASIC (28 nm):**
 - Pixel size: 55 x 55 μm²
 - ~ 30 ps precision
 - **Power: 5-10 W/cm²**



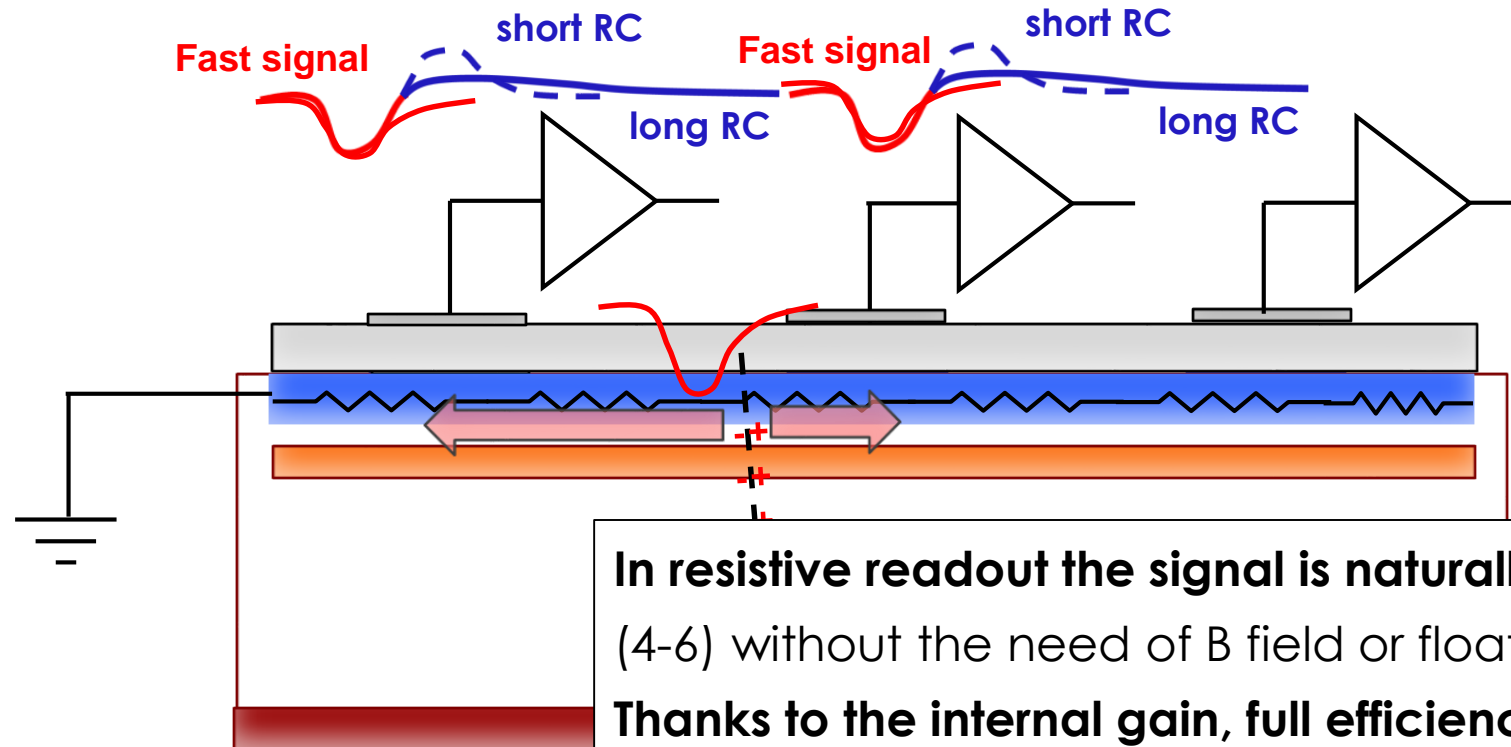
Even with a much smaller technological node, precision timing with small pixels requires a lot of power

Bonus: internal gain decreases the need of power

Second design innovation: resistive read-out

Innovative design: resistive silicon detectors (RSD or AC-LGAD), as in RPC et al.

- The signal is formed on the n+ electrode
- The AC pads offer the smallest impedance to ground for the fast signal
- The signal discharges to ground

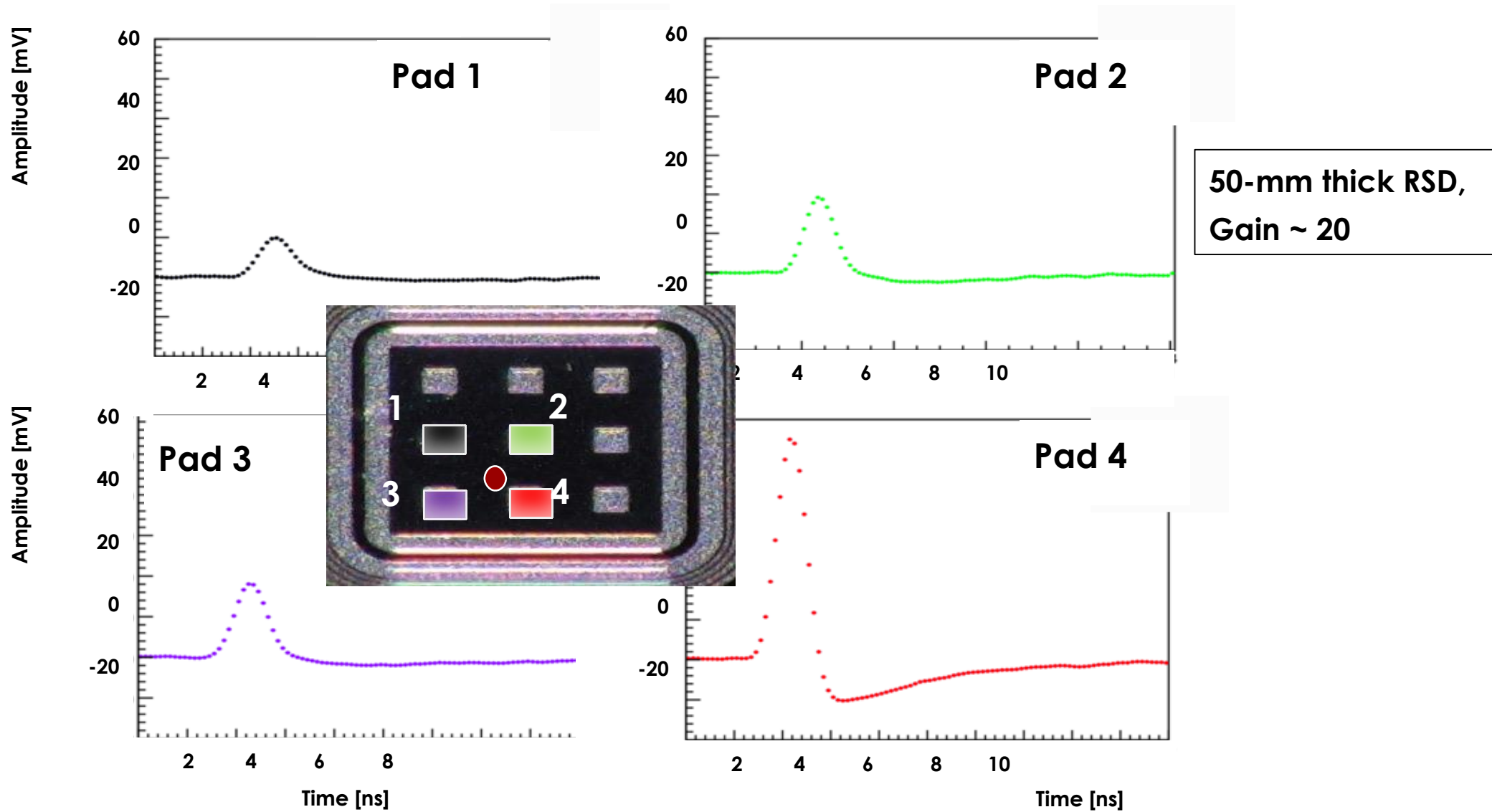


In resistive readout the signal is naturally shared among pads (4-6) without the need of B field or floating pads

Thanks to the internal gain, full efficiency even with sharing

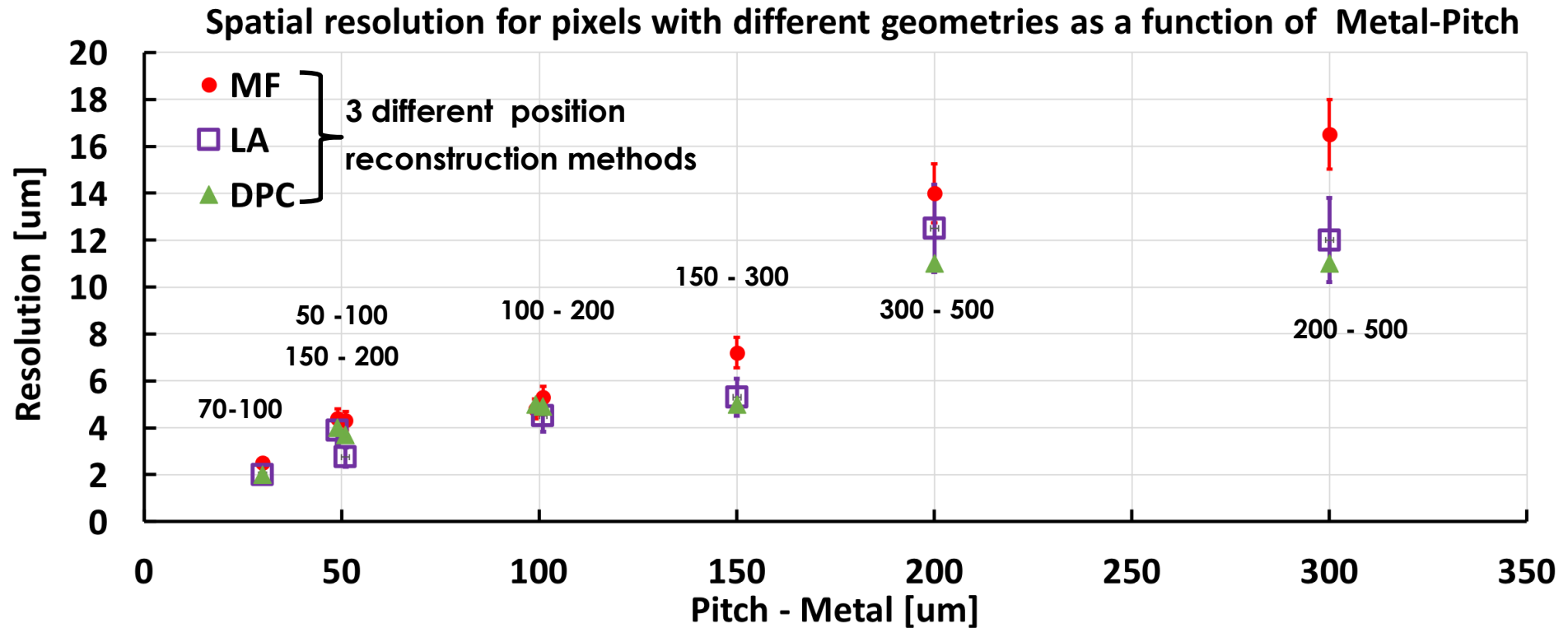
Results presented here are from the FBK RSD1 production

Resistive Silicon detector: example of signal sharing



The laser is shot at the position of the red dot: the signal is seen in 4 pads

Laser study: position resolution vs pixel geometry



RSDs reach a spatial resolution that is about 5% of the inter-pad distance

→ ~ 5 μm resolution with 150 μm pitch

RSDs have the “usual” UFSD temporal resolution of 30-40 ps

Present and future

Under construction:

The two large timing layers (25 m²) of the ATLAS-CMS collaboration

1.3 x 1.3 mm² pads UFSD, ALTIROC & ETIROC ASICs, 200-300 mW/cm², resolution ~ 45 ps/hit

Advanced prototypes:

Timepix4 soon to be coupled with TI-LGAD

55 x 55 μm² pixels, ~ 0.6 mW/cm², target resolution <100 ps/hit

TIMESPOT1 with trenched detectors

55 x 55 μm² pixels, ~ 5-10 W/cm², resolution ~ 30 ps/hit

Demonstrators:

FASTPIX (CMOS), MonPicoAD (SiGe), Resistive readout (large pixels, excellent spatial and temporal resolution)

New kids on the block:

Monolith (SiGe+LGAD)

Wrap-up

4D tracking is a very young booming field, hybrid and monolithic approaches are yielding very good results

The pace of innovation is very fast (especially considering that silicon sensors is a very mature field)

Several demonstrators with temporal precision of about 30 ps are available. Not unreasonable to expect 10-15 ps in the next few years.

In my view, the most difficult part is in the design of the electronics.

Temporal resolution degrades very quickly if the whole system is not “perfect”

It is very difficult to combine very good position precision, $<5 \mu\text{m}$, with good temporal resolution using the “single pixel” design. Charge sharing might be the key to solve this problem.

It takes a village

The path to 4D tracking is complex, with many different communities working on various aspects. Their contributions are of fundamental importance to reach the end goal.

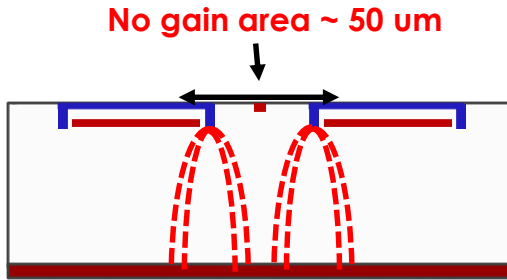
Acknowledgement

We kindly acknowledge the following funding agencies, collaborations:

- RD50 collaboration
- INFN - Gruppo V, UFSD and RSD projects
- INFN – FBK agreement on sensor production (convenzione INFN-FBK)
- Horizon 2020, grant UFSD669529
- U.S. Department of Energy grant number DE-SC0010107
- Dipartimenti di Eccellenza, Univ. of Torino (ex L. 232/2016, art. 1, cc. 314, 337)
- Ministero della Ricerca, Italia , PRIN 2017, progetto 2017L2XKTJ – 4DinSiDe
- Ministero della Ricerca, Italia, FARE, R165xr8frt_fare

Collection of extra sides

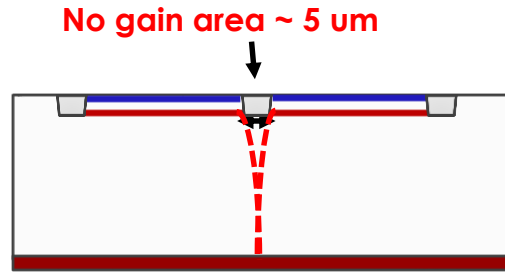
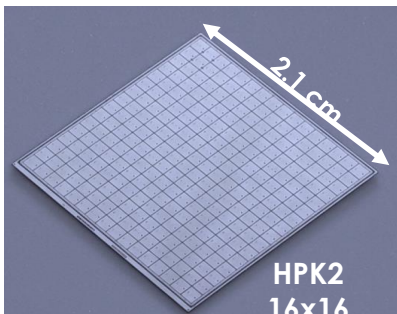
UFSD Summary: more gaining and more sharing



JTE + p-stop design

JTE/p-stop UFSD

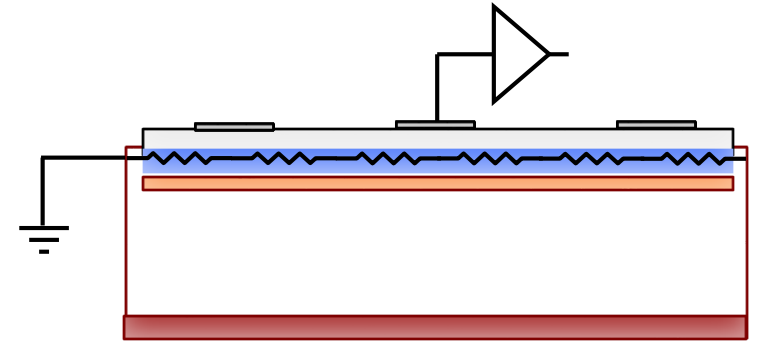
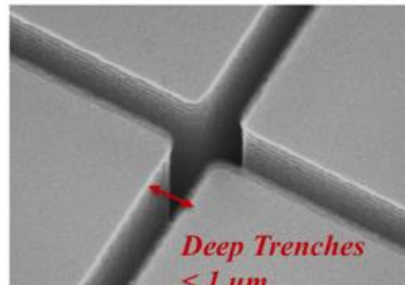
- CMS & ATLAS choice
- Signal in a single pixel
- Not 100% fill factor
- Very well tested
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness ~ 2-3E15 n/cm2



Trench-isolated design

UFSD evolution: use trenches

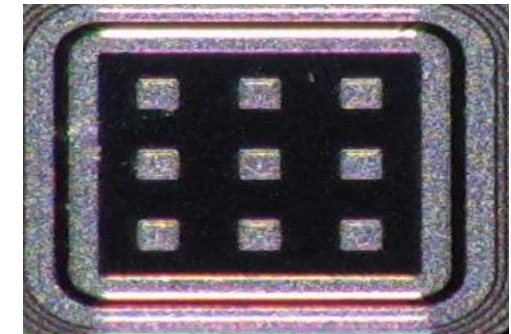
- Signal in a single pixel
- Almost 100% fill factor
- Temporal resolution (50 μm) : 35-40 ps
- High Occupancy OK
- Rate ~ 50-100 MHz
- Rad hardness: to be studied



RSD -- AC-LGAD

RSD evolution: resistive readout

- Signal in many pixels
- 100% fill factor
- Excellent position resolution: ~ 5 μm with large pixels
- Temporal resolution (50 μm) : 35-40 ps
- Rate ~ 10-50 MHz
- Rad hardness: to be studied



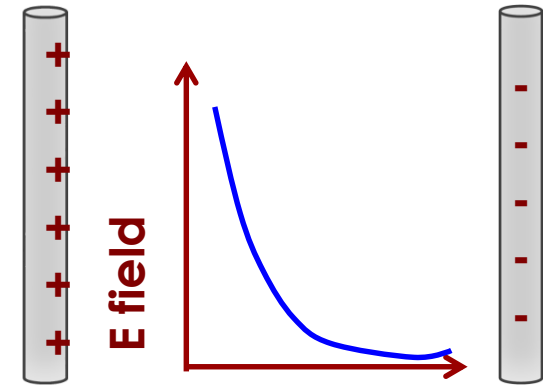
3D sensors for timing applications

3D sensors for timing have the same underlying features of standard 3D detectors: very good radiation resistance

The design is insensitive to non-uniform charge deposition

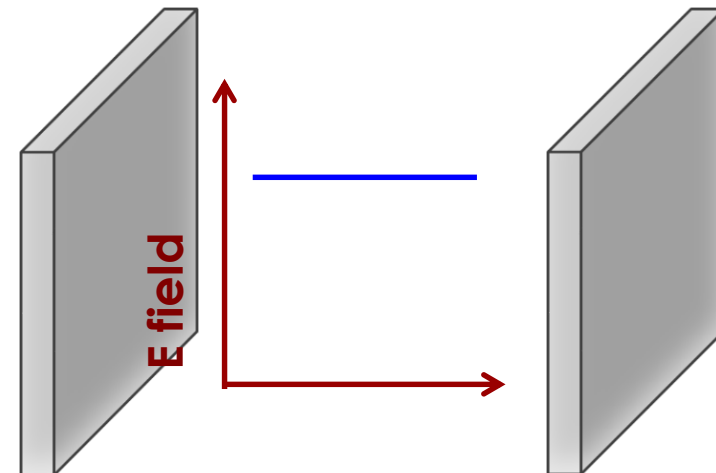
CNM-Ljubliana studies: use column geometry

In their “column” geometry, they cannot, the E field is not uniform enough



Timespot approach

using trenches gives a parallel plate geometry, and a weighting field $\sim 1/d$

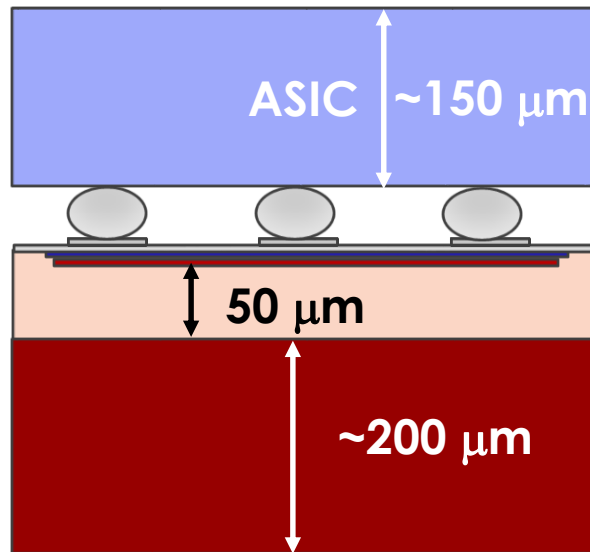


Reduced material budget

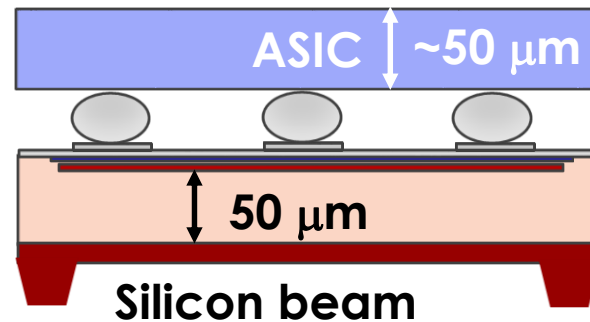
The active thickness of UFSD sensor is rather small $\sim 50 \mu\text{m}$.

In the present prototypes, the active part is attached to a thick “handle wafer”

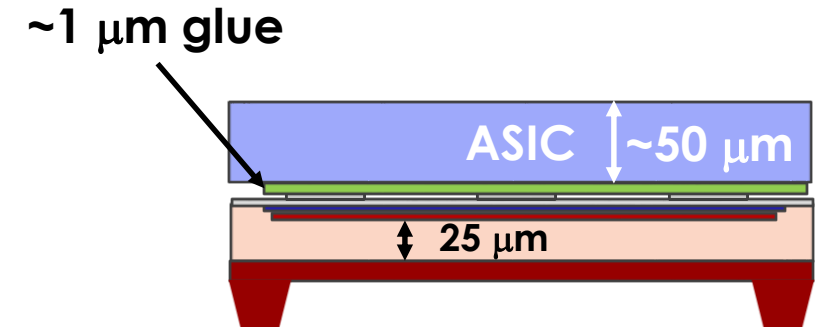
There is a clear path leading to $< 100 \mu\text{m}$ material:



Present design: no material budget optimization



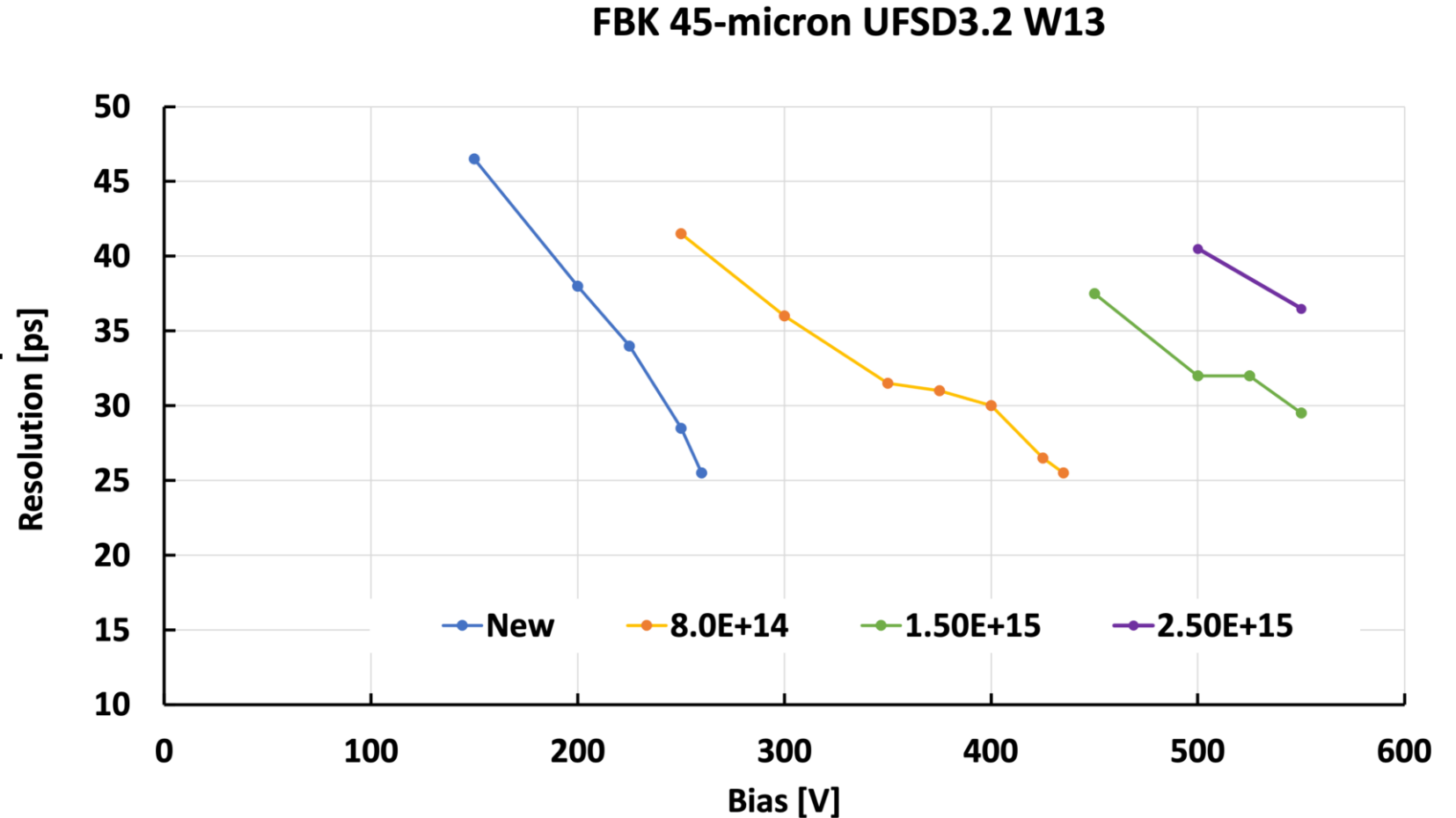
- Thinned handle wafer:
 $500 \mu\text{m} \rightarrow 10\text{-}20 \mu\text{m}$



- Thinned handle wafer:
 $500 \mu\text{m} \rightarrow 10\text{-}20 \mu\text{m}$
- Thinned active area:
 $50 \mu\text{m} \rightarrow 25 \mu\text{m}$
 $50 \text{ps} \rightarrow 25 \text{ps}$

UFSD radiation hardness

Evolution with radiation of the biasing working point for a 45-micron thick LGAD with a carbonated gain layer

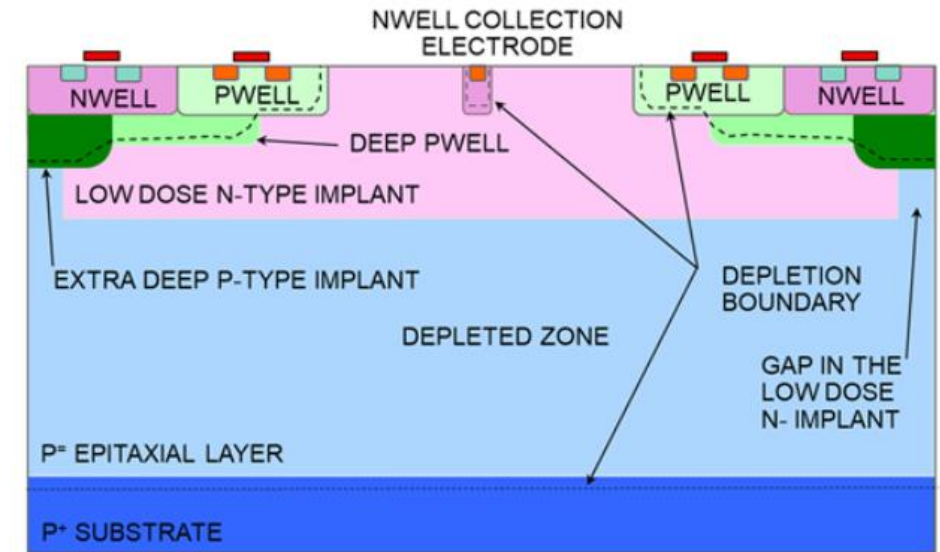


Present LGAD design assures better than 40 ps up to $2.5E15 n_{eq}/cm^2$

FASTPIX approach

“In the ATTRACT project FASTPIX we investigate monolithic pixel sensors with small collection electrodes in CMOS technologies for fast signal collection and precise timing in the sub-nanosecond range.”

- Evolution of the process used for MALTA: speeding up the electron lateral drift
- Small pixel pitches ($\sim 10 \mu\text{m}$)
- Very low electrode capacitance ($< 1\text{fF}$)
- Expected jitter (electronics): 20ps @ $Q_{\text{in}} = 1000 e^-$
- Estimated resolution: sub-ns (a few hundred ps)



T. Kugathasan et al., Nucl. Inst. Meth. A
Vol. 979, Nov. 2020

Present status of ATLAS-CMS timing layer

UFSD are available from many vendors: HPK, FBK, CNM, BNL

and several more are coming on line: Micron, NDL (China), IHEP (China)

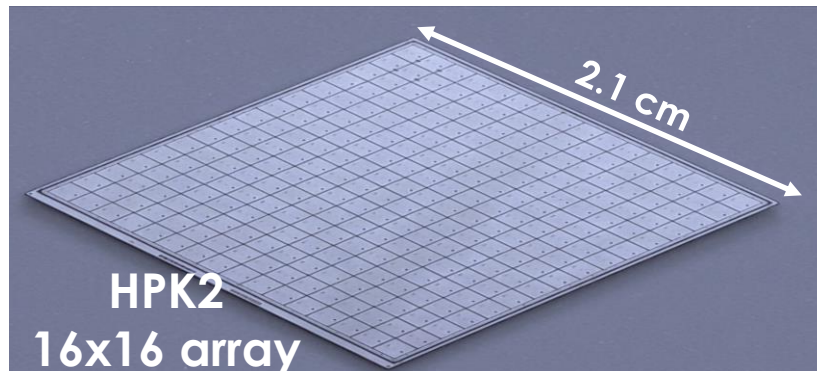
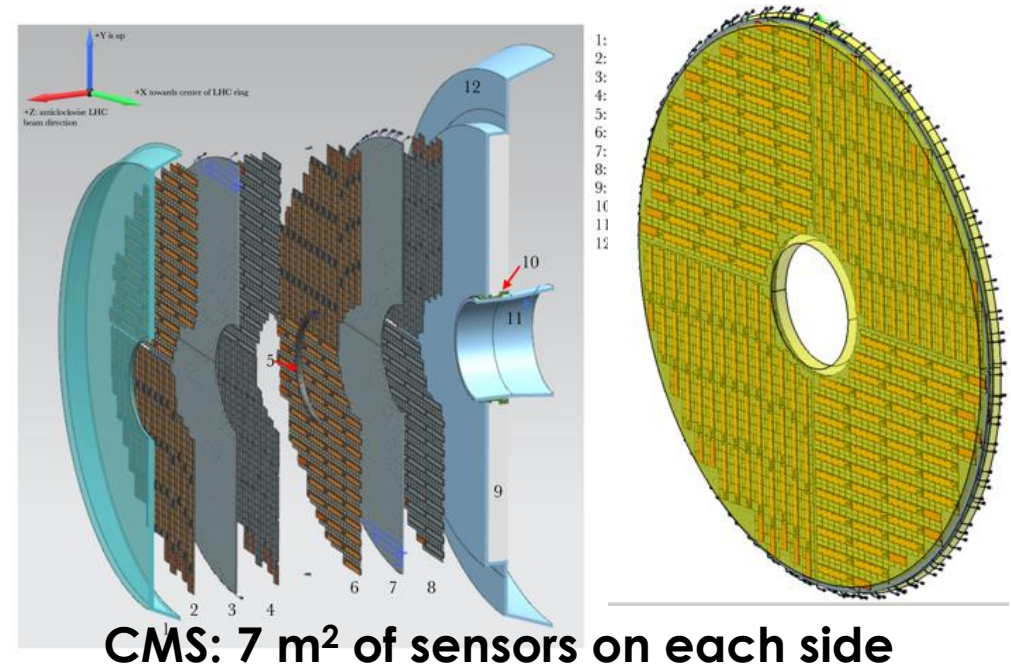
ATLAS and CMS are planning to use ~ 20-30 m²

→ Mature technology

Installation: 2023-2025

CMS: 2 layers, covering the full endcap $1.6 < \eta < 3$

ATLAS: 2 ½ - 3 layers, covering high rapidity $2.5 < \eta < 4$



Read-out chips for UFSDs

In the past 3-4 years, the ATLAS and CMS collaborations poured a considerable amount of resources into designing the read-out chips for their respective timing layers.

ATLAS: ALTIROC, TSMC 130 nm, 15x15 pads,

CMS: ETROC, CMOS 65 nm, 16x16 pads

For both: input load about 4 pF, jitter ~ 20ps at 10fC of input charge

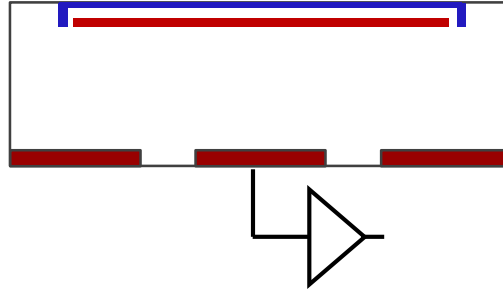
Power:

ALTIROC ~ 3.5 mW/ch, }
ETROC ~ 3 mW/ch } 2-300 mW/cm²

As a comparison, the **RD53 readout chip for pixel detectors** for tracking (i.e. no timing) at the HL-LHC with 50 x 50 μm^2 and 25 x 100 μm^2 feature sizes is estimated to have a power density of **about 1 W / cm²**

A timing layer with large pixels needs less power than a layer of small traditional pixels

I-LGAD: a new design for 100% fill factor



i-LGAD

- **p-side segmentation**
 - **Signal in a single pixel**
 - **100% fill factor**
 - **Thin i-LGAD with single side processing under development (using trenches)**
- => done with TCAD simulation, run starting in spring 2021 @ CNM**
- **High Occupancy OK**
 - **Rate ~ 50-100 MHz**
 - **Rad hardness ~ 2-3E15 n/cm²**

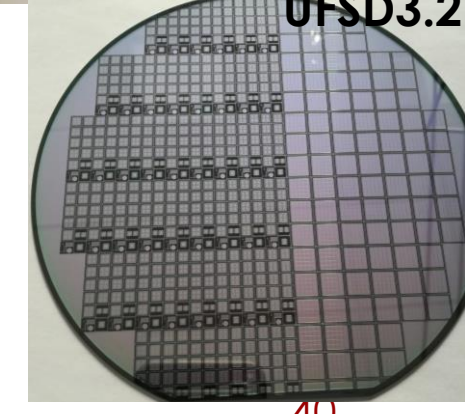
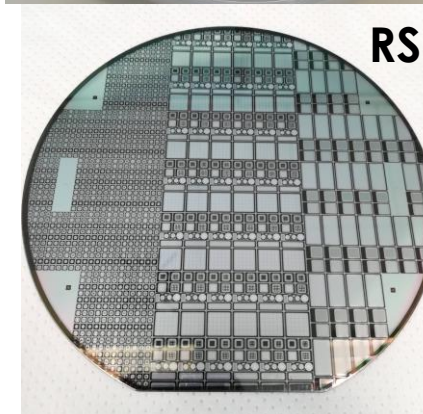
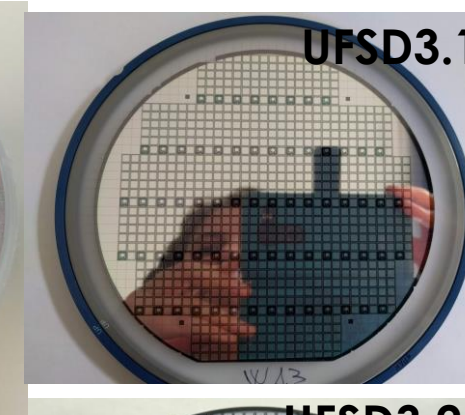
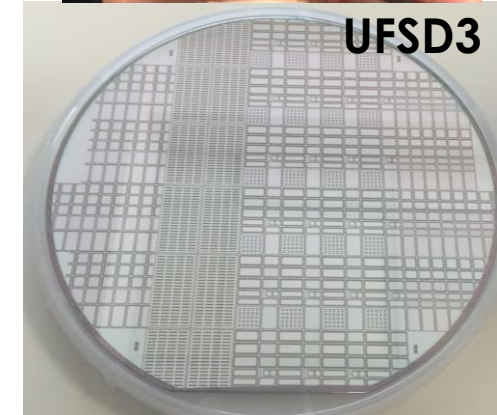
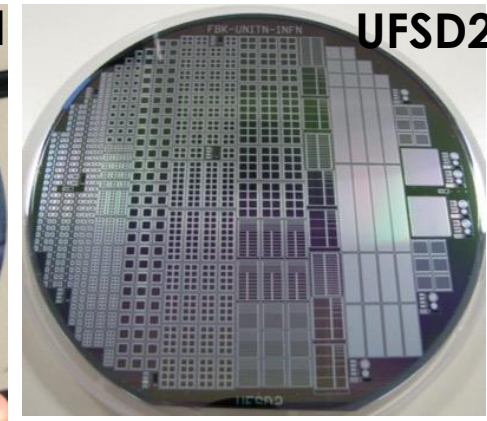
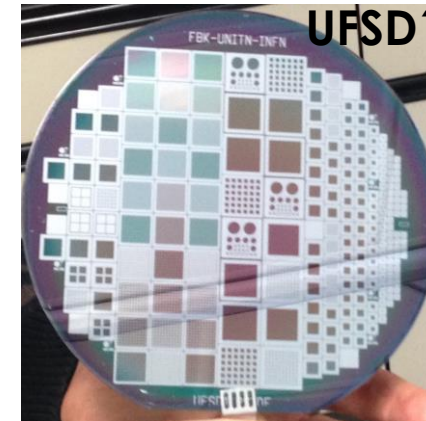
The UFSD project: brief history

Aim: develop sensors with excellent temporal and spatial resolutions via a series of productions and design refinements

Long term R&D, Not for a specific experiments

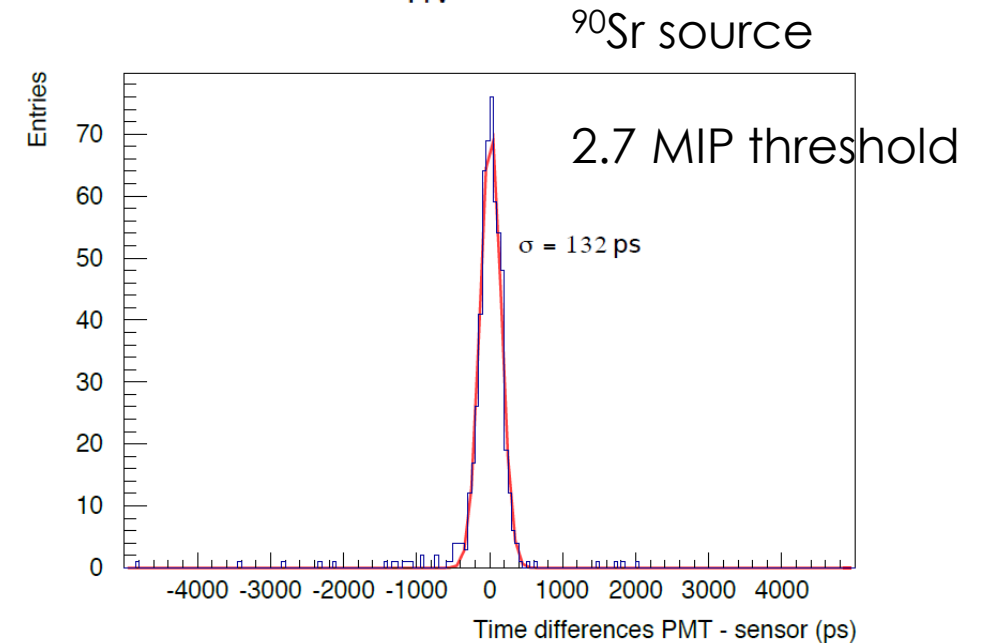
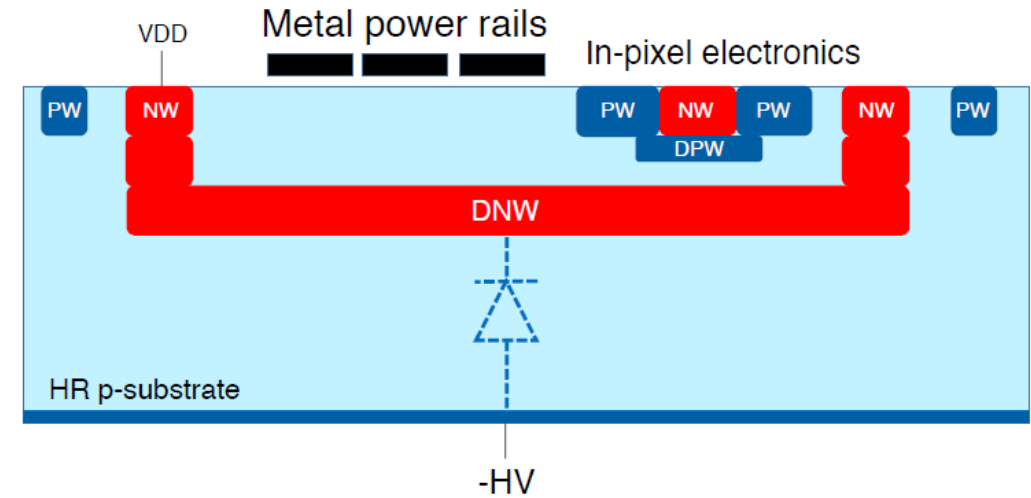
1. **2016:** UFSD1 First 300 μm thick LGAD (FBK 6" wafer)
2. **2017:** UFSD2 First 50 μm thick LGAD (FBK 6" wafer)
Gain layer doping: Boron, Gallium, Boron + Carbon,
3. **Fall 2018:** UFSD3 50 μm LGAD (FBK 6" wafer), produced with the stepper (many Carbon levels, studies of interpad design)
4. **June 2019:** UFSD3.1 50 μm LGAD (internal FBK) interpad design.
5. **June 2019** RSD1 Resistive AC-LGAD (FBK 6" wafer)
6. **June 2020:** UFSD3.2 25, 35, 45, and 55 μm LGAD, carbon studies, deep, shallow gain implant (FBK 6" wafer)
7. **Q1/2021:** UFSD3.3 (FBK 6" wafer)
8. **Q1/2021:** Trench-Isolated (FBK 6" wafer)
9. **Q2/2021:** RSD2 (FBK 6" wafer)
10. **Q2/2021:** ExFlux -> optimized for extreme fluence

Project fully funded for 3 more years



HV-CMOS approach: CACTUS

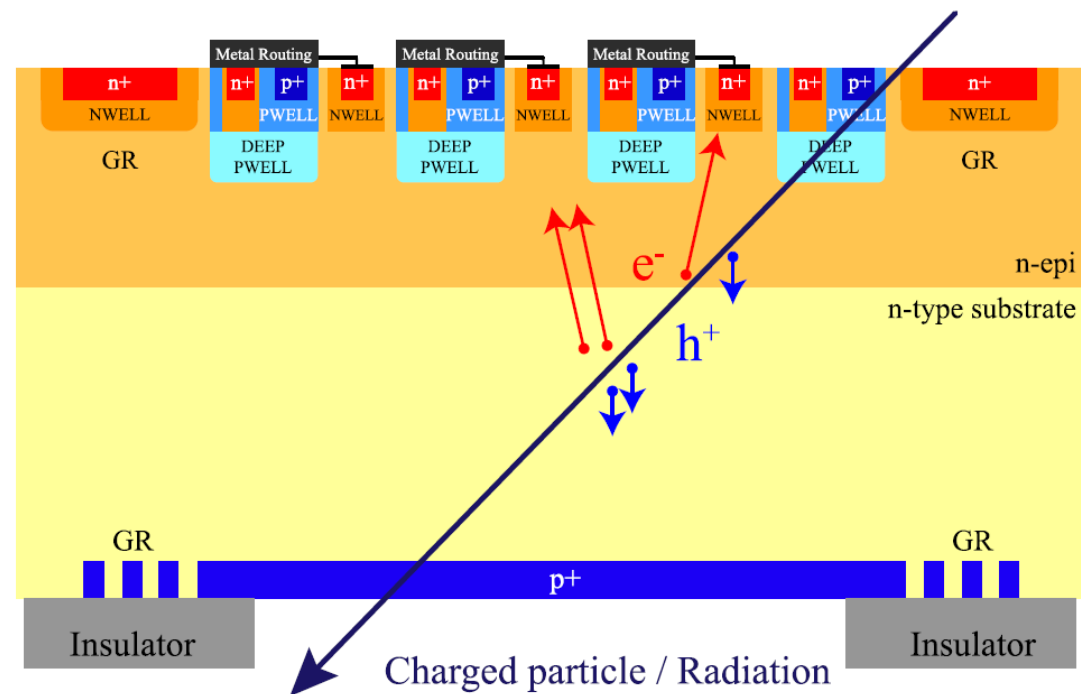
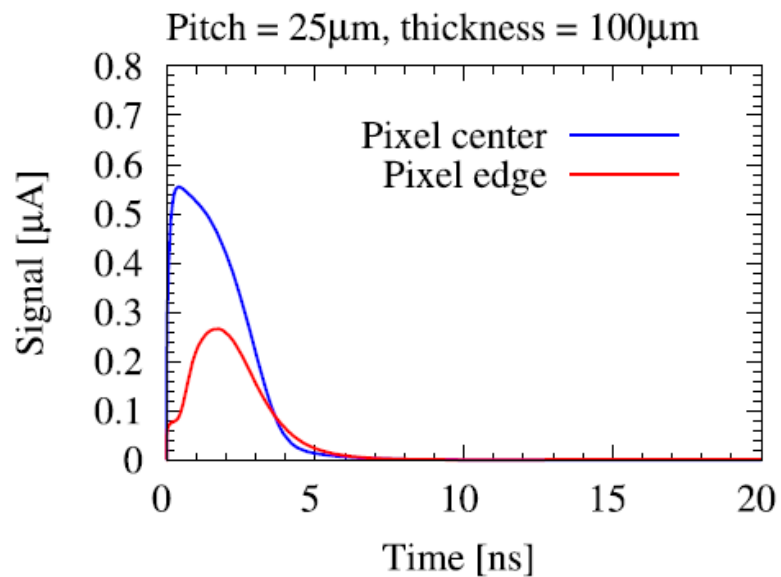
- CMOS LFoundry 150 nm
- Deep nwell collection diode, fully depleted
- FE electronics inside the pixel
- Fast and uniform charge collection
- Substrate thickness: 200 μ m
- Pixel size: 0.5 – 1 mm²
- Pixel capacitance: 1 – 1.5 pF
- Res: 278 ps at 1.7 MIPS, 303 ps at 1 MIP
- Noise can be reduced by moving the readout electronics outside the pixels: capacitance reduction



Y. Degerli et al., 2020 JINST 15 P06011

ARCADIA

- MAPS 110-nm CMOS
- Fully depleted substrate: charge collection by drift
- Process validated on 100 – 300 μm thick substrates, 25 and 50 μm pitch
- New test structures with 10 μm pitch on 50 μm substrate being designed: $\sim 1\text{ns}$ charge collection time



L. Pancheri et al., IEEE Tran. Electron Dev., Vol. 67, No. 6, June 2020

R&D in progress at the University of Geneva

MONOLITH Project:

- ERC advanced for the development of monolithic silicon pixel sensors in SiGe BiCMOS with picosecond time resolution. Sensor design based on PicoAD concept of the University of Geneva.

FASER :

- SNSF project to build of a new pre-shower module for FASER experiment at LHC based on monolithic pixels in SiGe BiCMOS with very large dynamic range, 100 μm pixel size and 100ps time resolution.

100 μPET :

- SNSF project to build a small animal PET scanner with 100 μm resolution based on monolithic silicon pixel sensors in SiGe BiCMOS.