

# HEPS-BPIX4: A Prototype Pixel Readout Chip Working in Single Photon Counting Mode with a Novel Charge Sharing Suppression Scheme

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HEPS-BPIX4 is a hybrid pixel detector readout chip for X-ray applications for the High Energy Photon Source (HEPS) in China. The prototype readout chip contains an array of  $20 \times 32$  pixels with a pixel size of  $55 \mu\text{m} \times 55 \mu\text{m}$ , working in single photon counting mode. Each pixel handles with both positive and negative input charge signals and has a counting depth of 11 bits. The chip could work at a 160 Mbps output data rate with zero dead time.

Besides the chip design description, this paper also proposes a novel architecture aiming at eliminating the spectral distortion caused by the charge sharing effect due to the fine pixel pitch. It is based on charge summing and centroid arbitration among adjacent pixels. In every cluster grouped by  $3 \times 3$  pixels in the chip, charge deposited in four pixels by a single photon is concentrated into the center pixel and added together. Then it is compared with the energy threshold for discrimination. In the meantime, the center pixel is also judged by a secondary comparator with a minimum threshold. Then the arbitrator decides if the charge of the center pixel is the maximum. Only those two matched conditions give a photon counting pulse to the digital part.

Compared with reported schemes that transmitted more than ten signals, the proposed scheme reduced the complexity of communicated pixels interconnection in the layout. There are only seven signals including three analog signals and four digital signals received by the center pixel from the adjacent four pixels. Besides, it improved the charge sharing decision precision to be as high as 99% and has been verified by python modelization simulation. The chip has been manufactured and tested. Detailed results, especially the charge sharing cancellation test in the pixel array, is given in this paper.

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