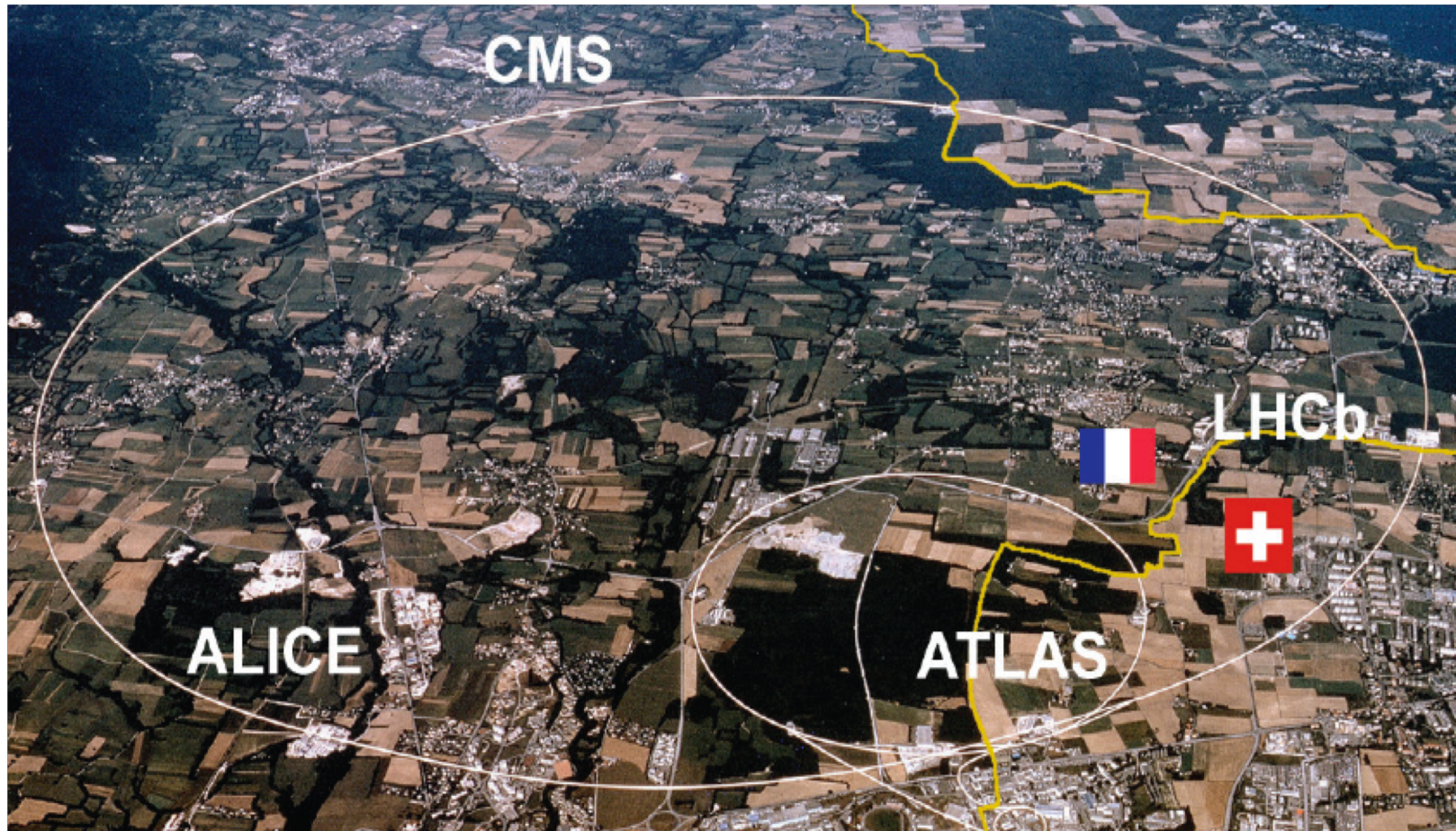


# ATLAS Japan ITk

Univ of Tsukuba

Daigo Harada

# LHC



- The largest (27km) pp hadron collider in the world.
- 13 TeV Center of Mass energy
- 4 collision position (ATLAS, CMS, ALICE, LHCb)

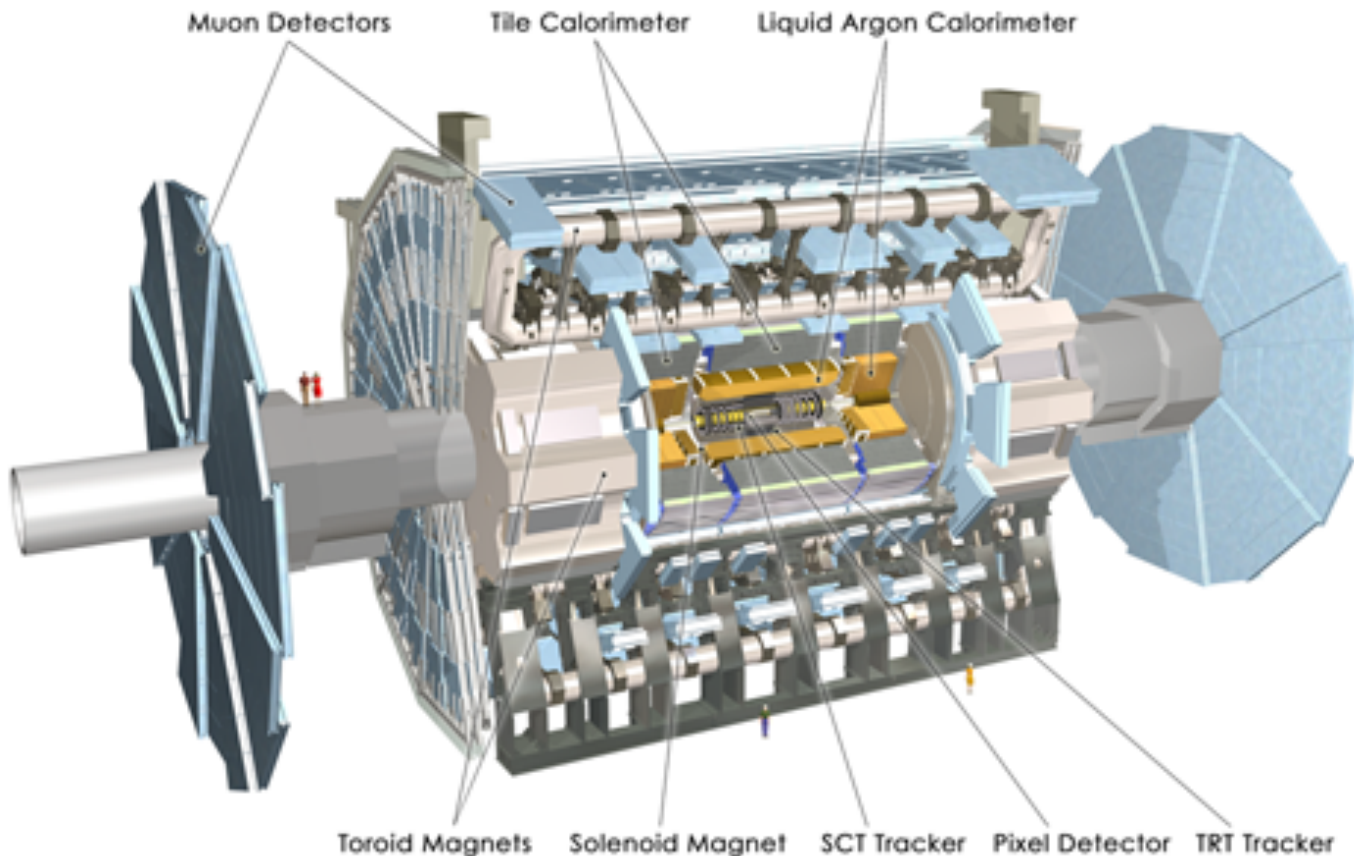


# ATLAS

height 25m, length 44m weight 7000t

three type sensors

- Inner detector <- our group  
first part of ATLAS to see the decay products of the collisions  
very compact and highly sensitive
- Calorimeters  
measure the energy a particle loses as it passes through the detector
- Muon detectors  
detect muon using muon chambers



# HL-LHC

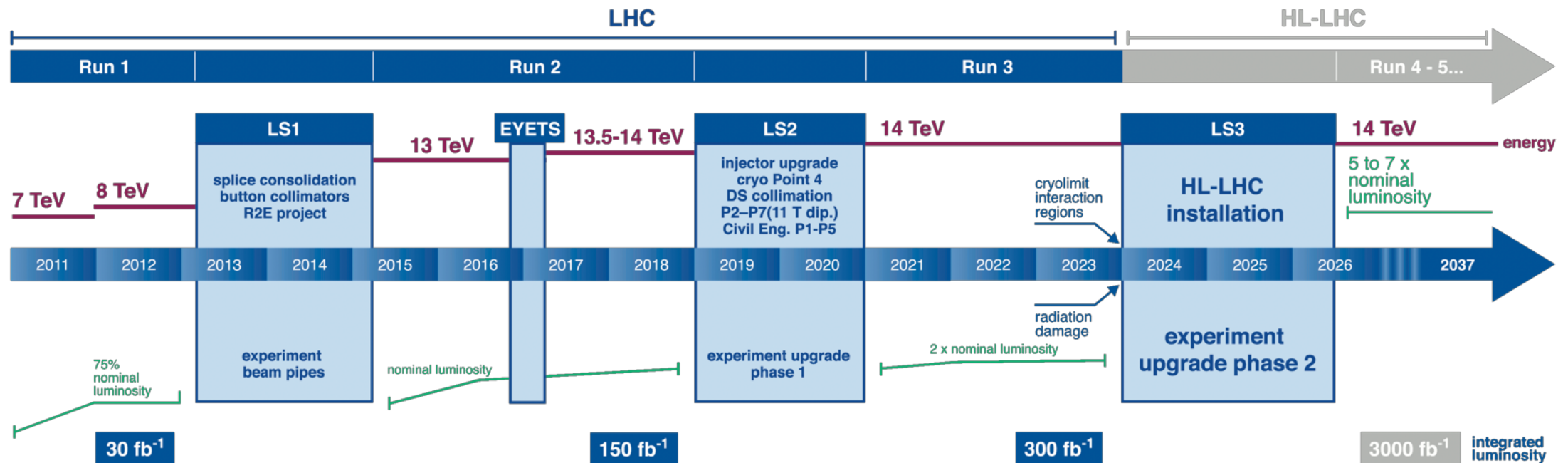
The LHC will become High-Luminosity-LHC(HL-LHC) at 2026.

The benefits are measurements and studies of rare processes.

Peak luminosity:  $5-7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \sim \times 5-7$

Average pile-up: up to  $\sim 200 \sim \times 5$

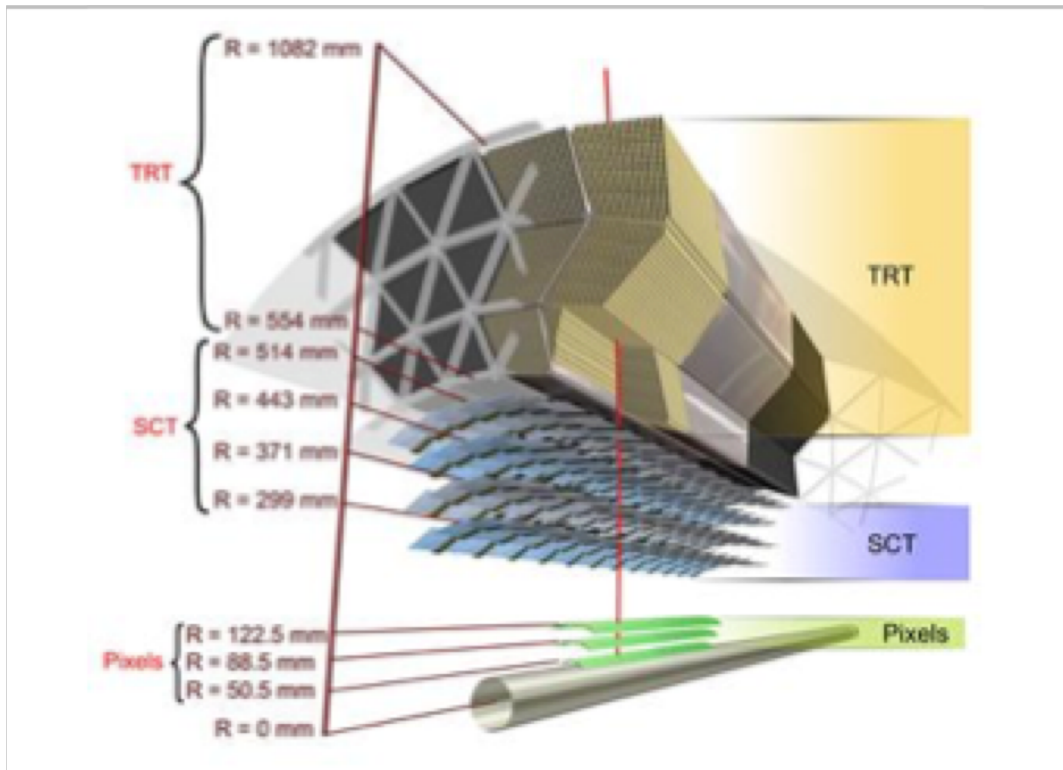
Integrated luminosity:  $3000 \text{ fb}^{-1} \sim \times 10$



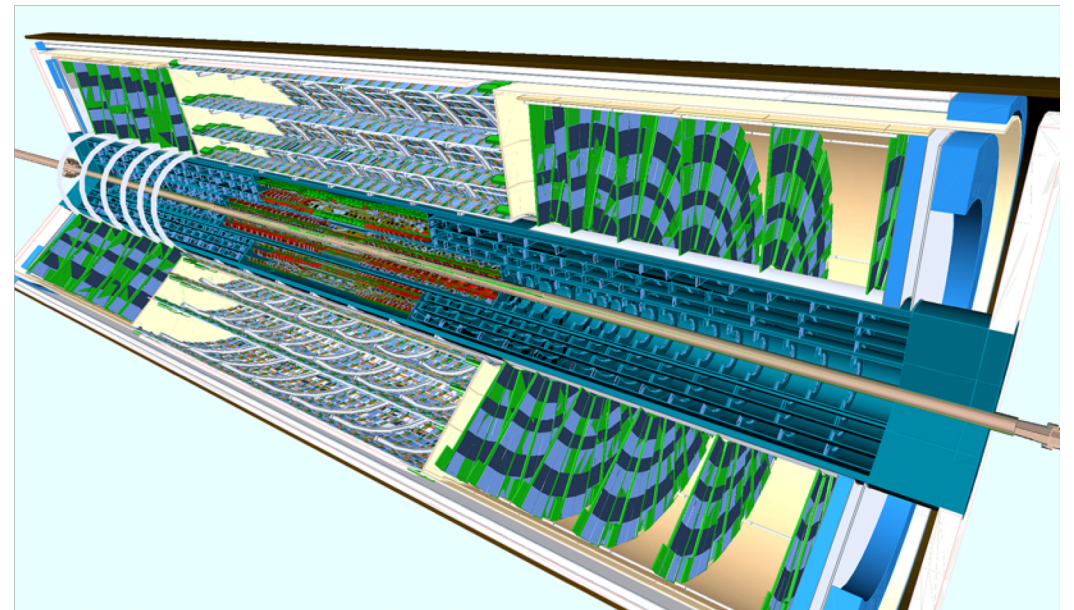
# ITk

for HL-LHC ATLAS detector will upgrade.

- replace all silicon sensor strip/pixel detector
- cover large area ( $\eta = 4.0$ )
- to reduce hit occupancy small pixel/strip size
- high radiation resistivity



present Inner detector

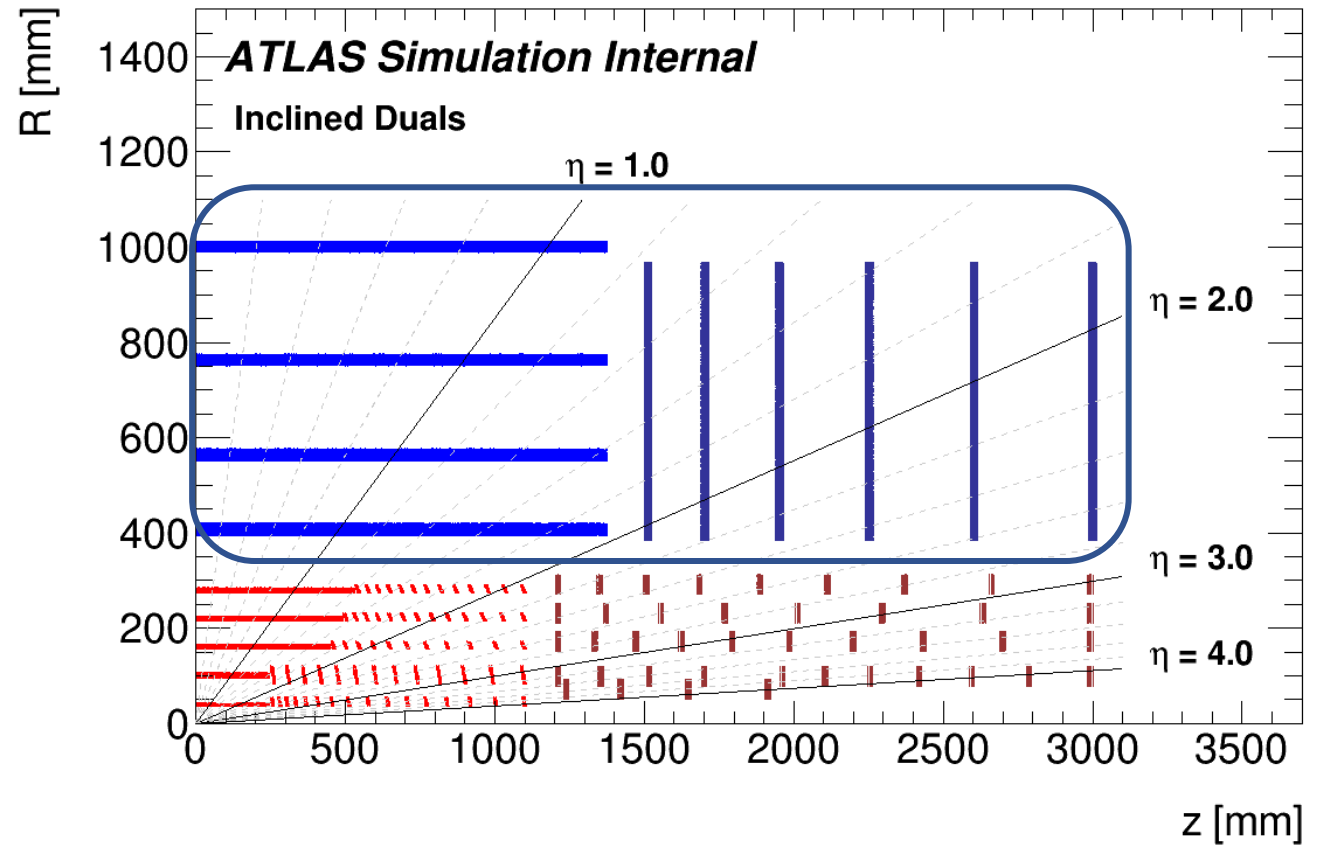
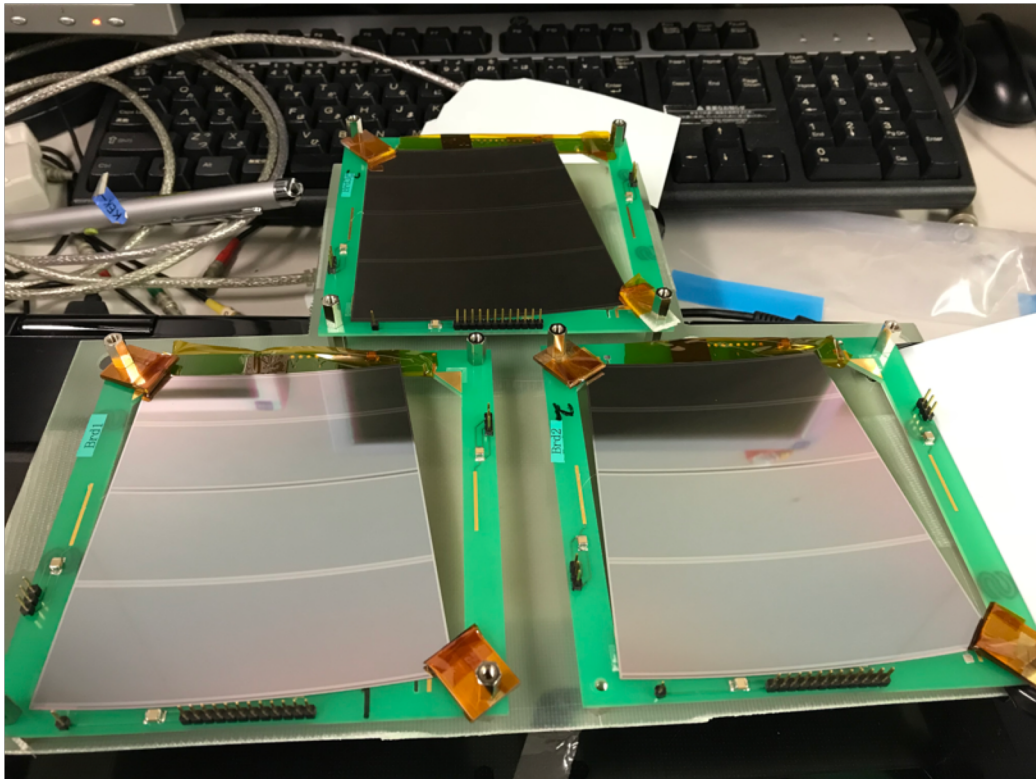


HL-LHC Inner detector (ITk)



# strip detector

large area of ITk are strip detector.  
strip sensors have already been under  
pre-production  
Japan group QC/QA



# Japanese QA/QC overview

Japan takes responsibility on ½ barrel sensor (~6,000) production and associated QC/QA

QC: everything at HPK

❖ IV+CV ... as HPK provides

❖ AC probing

3 half moon's per batch (~50)

❖ DC probing

~10 batches/month

Image capture/warp meas.

~~24h stability~~

QA: Tsukuba

mini CCE/IV/CV

MD8 IV/CV

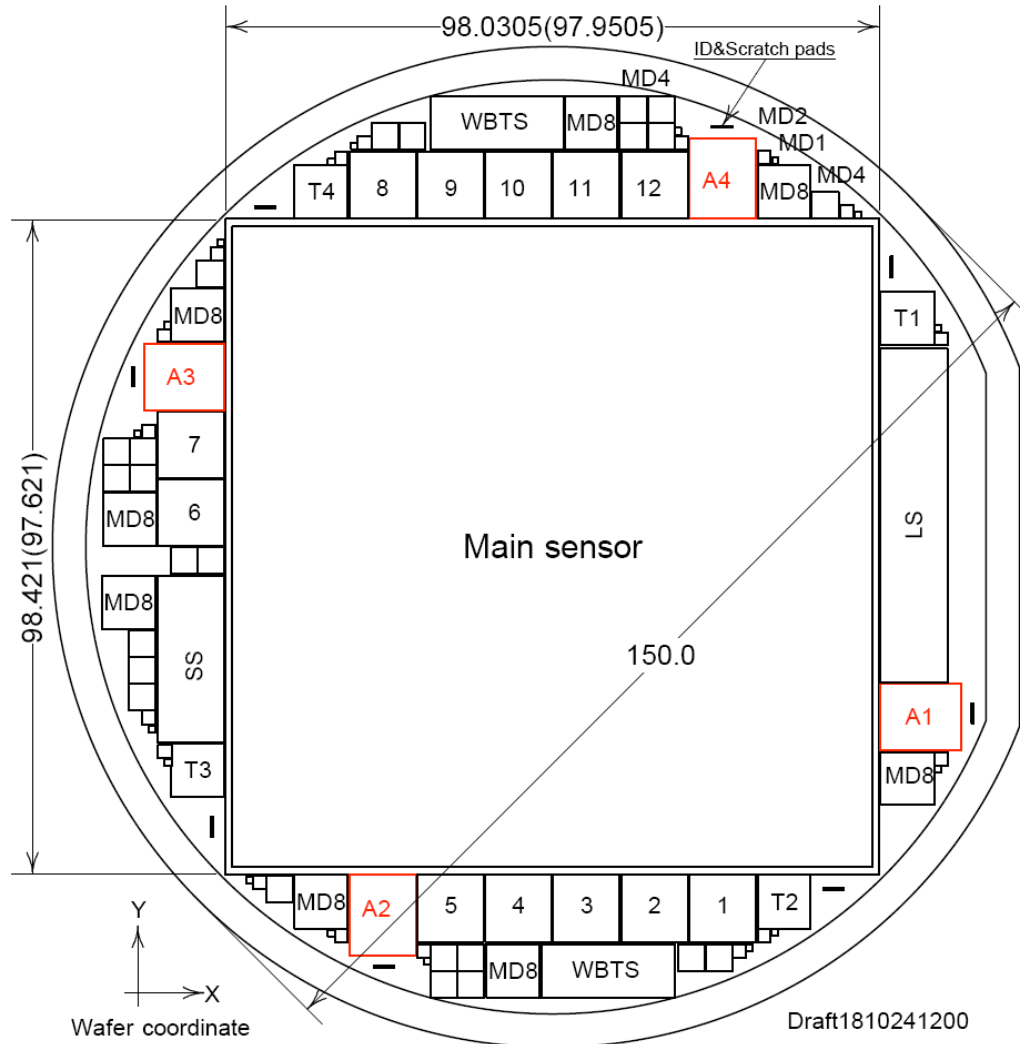
~~TS surface properties~~

CYRIC irradiation (twice/year) as cross-check of

monthly Birmingham irradiation

mini/MD8/~~TS~~

# production

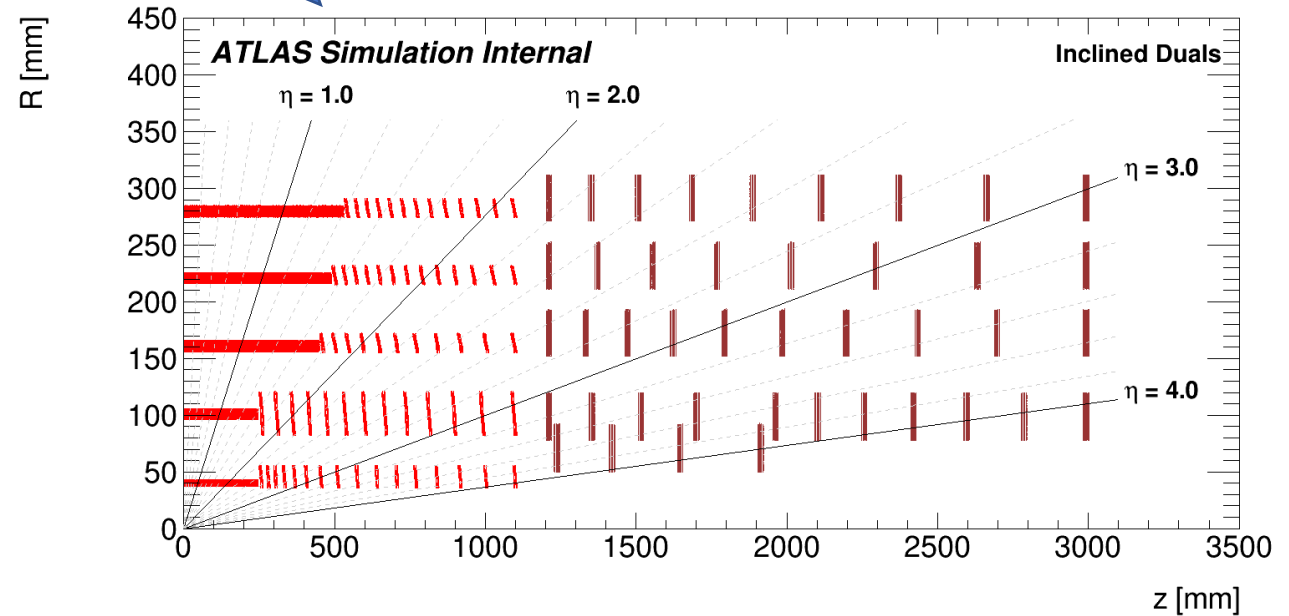
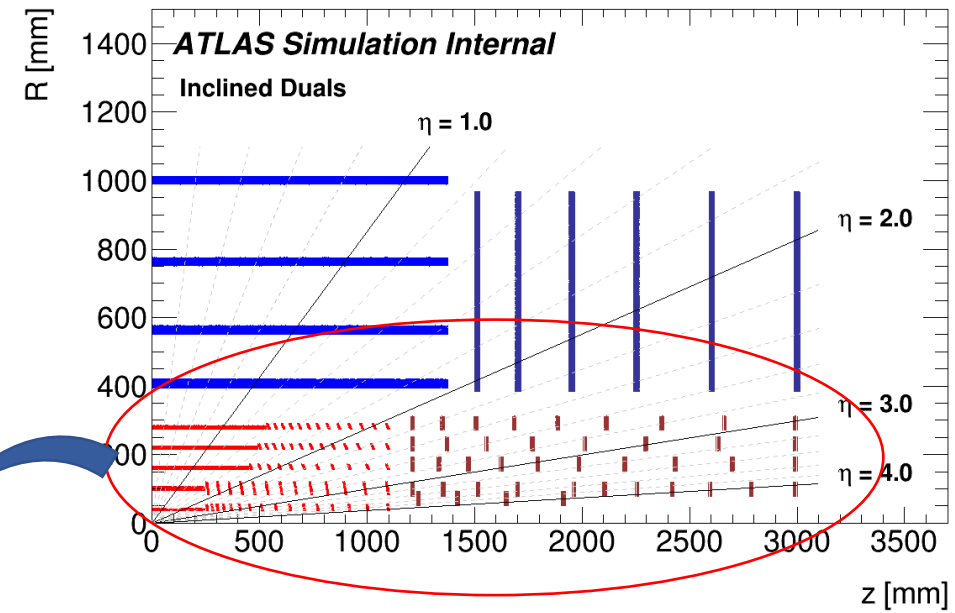
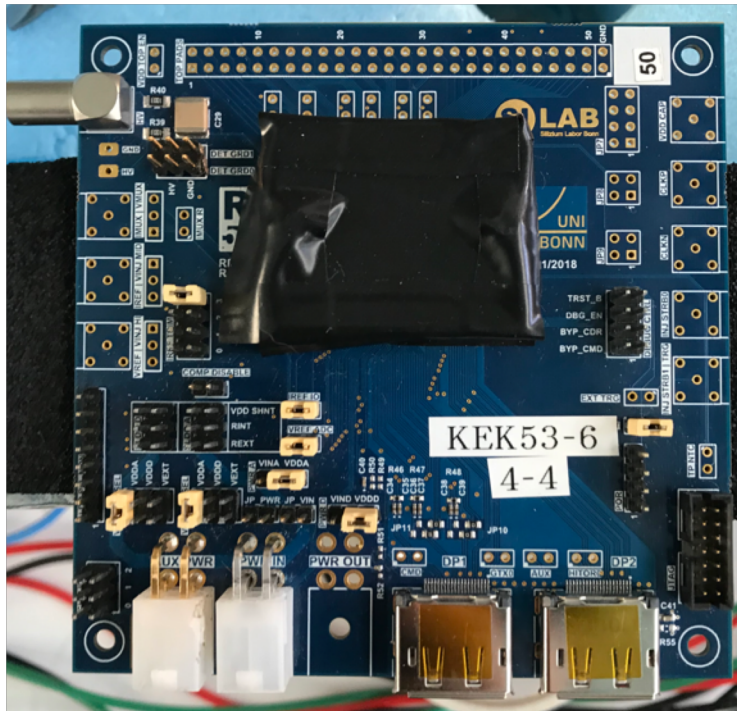


- All the Monitor test structures (except 8x8 and 4x4 diodes) can be inserted in one single test chip.
  - Monitor diodes and minis placed close to test chip to form a “test Si piece”
  - Four instances across the wafer
  - In discussions with HPK it was agreed that in production they could cut:
    - Piece 1: 1 test chip + diodes
    - Piece 2: 1 mini sensor
- In 2-3 wafers per batch (40-50)



# pixel detector

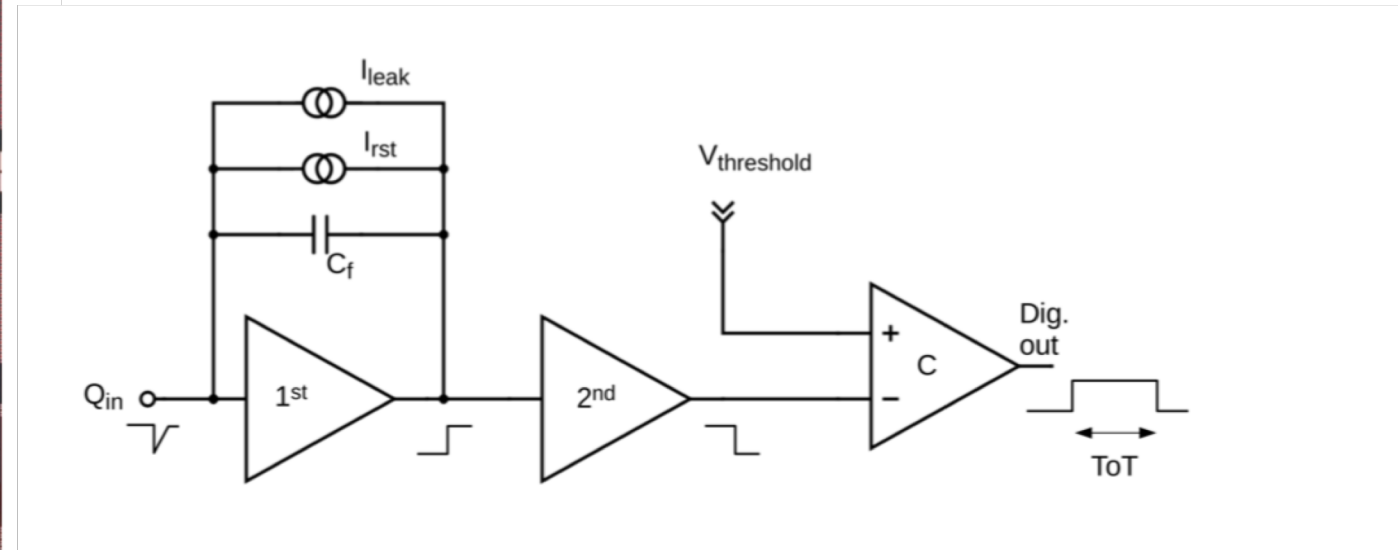
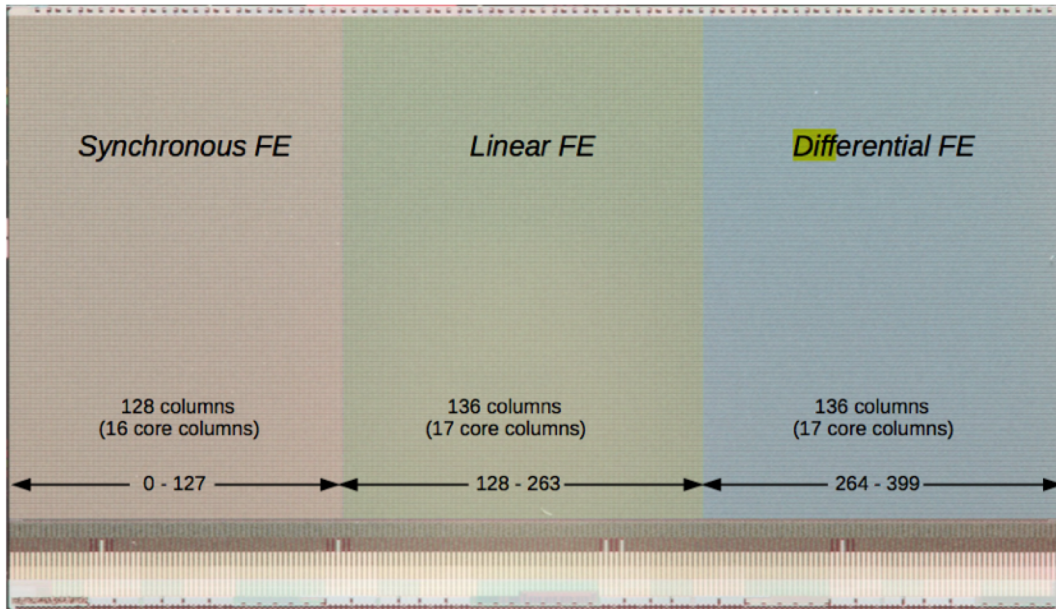
pixel detector is innermost sensor in ITk.  
1<sup>st</sup> layer is 3D sensor and 2<sup>nd</sup> to 5<sup>th</sup> layers are n+ in p  
50 × 50μm or 25 × 100μm (1/5 size of present sensor)  
Japan group develop 3<sup>rd</sup> to 5<sup>th</sup> sensor  
these area fluence is  $3.0 \times 10^{15}$



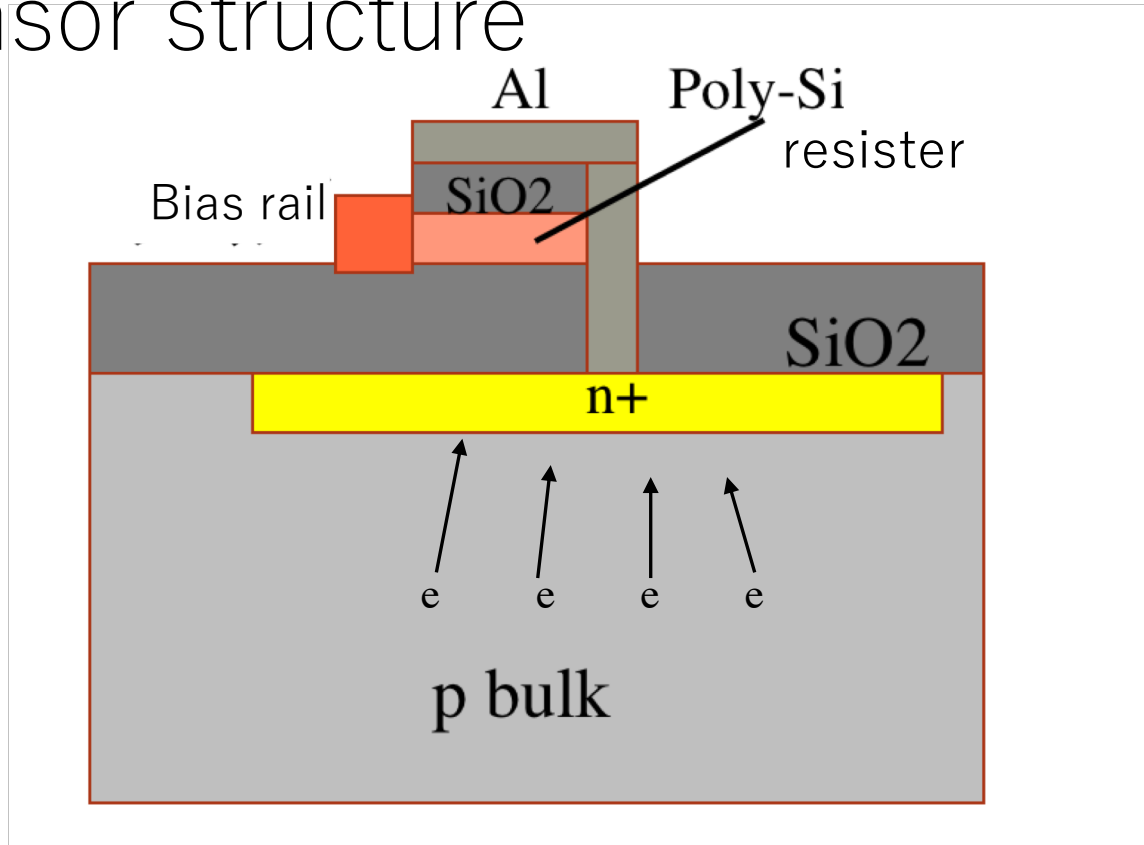
# RD53A readout ASIC

RD53A is new readout ASIC for test  
 bump pitch is 50x50  $\mu\text{m}$   
 to improve radiation resistivity,  
 65 $\mu\text{m}$  process  
 3 front end type by region

Feature	RD53A	Prod. spec.	Comment
Input pitch	50 $\mu\text{m}$ $\times$ 50 $\mu\text{m}$	50 $\mu\text{m}$ $\times$ 50 $\mu\text{m}$	aspect ratio defined by sensor
Bump columns $\times$ rows	400 $\times$ 192	400 $\times$ 384	
Input polarity	Negative	Negative	
Min. stable threshold	600 $e^-$	600 $e^-$	with 50 fF load, 4 $\mu\text{A}$ /pixel analog.
In-time threshold	< (thresh.+600 $e^-$ )	< (thresh.+600 $e^-$ )	varies w/ front end
Hit loss to in-pixel pileup	$\leq 1\%$	$\leq 1\%$	at 75 kHz avg. hit rate
Single pixel noise (ENC)	<100 $e^-$	<100 $e^-$	with 50 fF load; varies w/front end
Trigger latency	<12.8 $\mu\text{s}$	<35 $\mu\text{s}$	
Trigger mode	single level	two level	
Current/pixel, analog	3-4 $\mu\text{A}$	<4 $\mu\text{A}$	varies w/ front end
Current/pixel, digital	4 $\mu\text{A}$	4 $\mu\text{A}$	@ 75 kHz/pixel and 1 MHz trigger
Current, periphery	<150 mA	<200 mA	4 enabled output drivers
Command & control	serial 160 Mbps	serial 160 Mbps	DC-balanced, no separate clock
Output	4 $\times$ 1.28 Gbps	4 $\times$ 1.28 Gbps	
Output protocol	Aurora 64b/66b	Aurora 64b/66b	can use 1 to 4 lanes
Data aggregator output	none	bf 5.12 Gbps	



# sensor structure



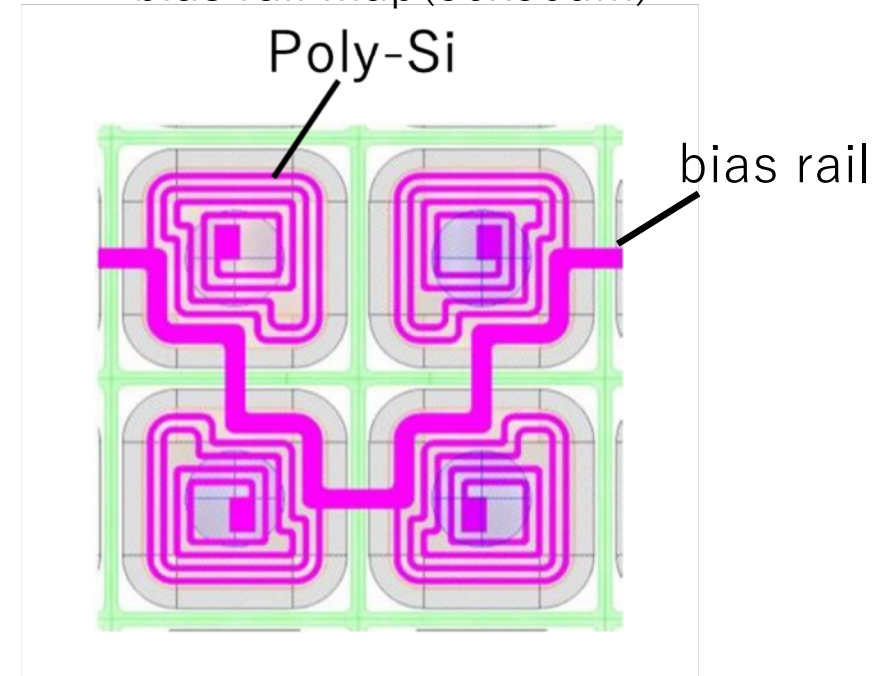
n+ in p bulk structure

No need to be full depletion to collect signal

Japan group introduce bias rail structure for HV test without ASIC when production.

bias rail connect all pixel, and drop ground level.

bias rail map(50x50um)



bias rail sensor is large noise and low efficiency compare to w/o bias rail sensor. to solve these issue,

low noise sensor w/ bias rail

■ large poly-Si resistor

■ small Al size

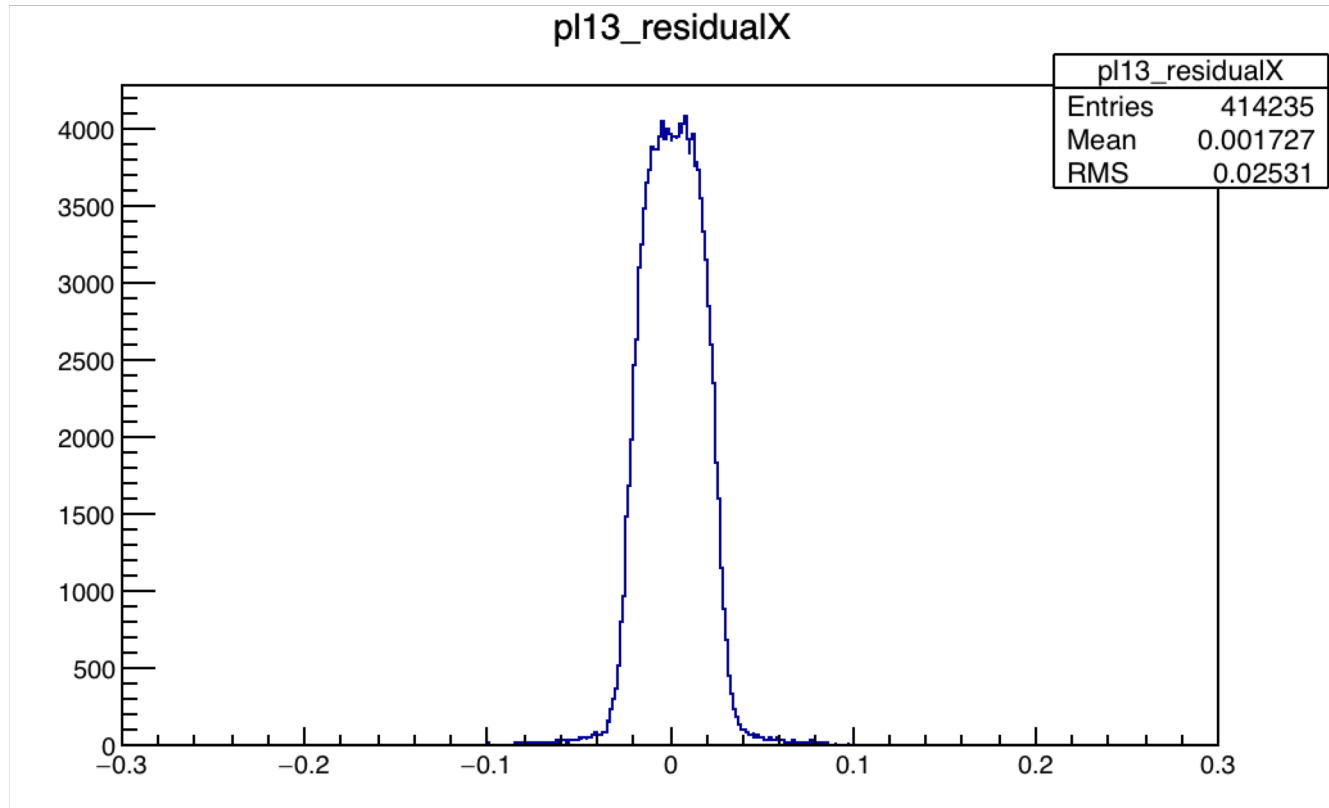
for high efficiency w/ bias rail

■ large n+ pad



# position resolution

test beam @CERN SPS



pixel size 50x50um sensor

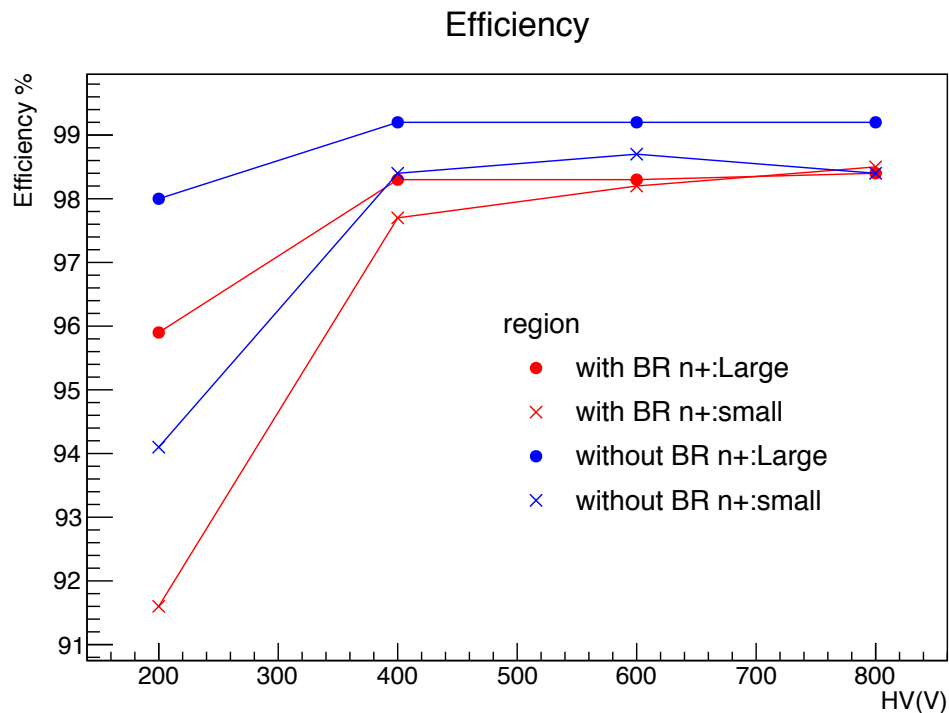


# Radiation resistant

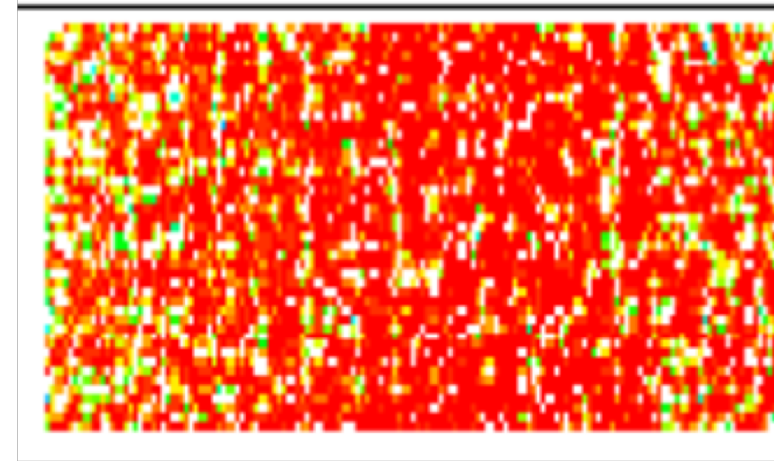
3<sup>rd</sup> sensor's fluence is  $3.0 \times 10^{15}$  1MeV  $n_{eq}$  during 10 years.

ATLAS request: Efficiency is  $>97\%$  after radiation damage.

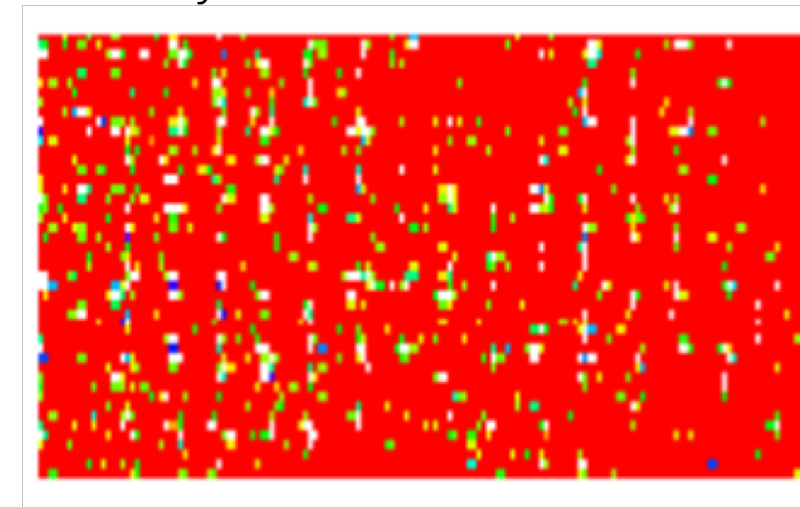
proton irradiation at CYRIC Tohoku University  
result of testbeam, w/ bias rail sensor efficiency is over 97% when 400V bias voltage



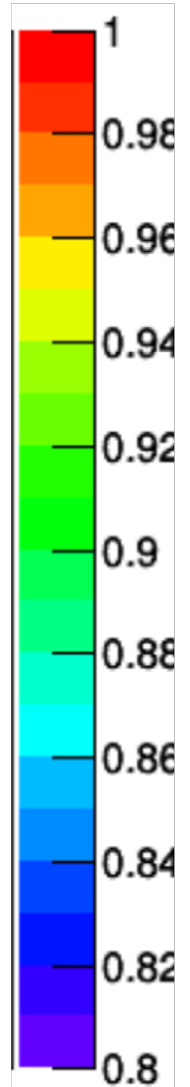
600V



w/ bias rail structure large n+  
efficiency  $98.33 \pm 0.02$



w/o bias rail structure large n+  
efficiency  $99.23 \pm 0.01$



# other test

- RD53A ASIC probe test  
before flip chip, RD53A operation check using probe card  
remove broken RD53A before flip chip, because flip chip  
is high cost.
- Threshold tuning test  
FEI4 pixel detector set in current ATLAS tracker has  
problem about tuning threshold.  
check about RD53A.

