Development of SOI Monolithic Pixel Detector for Fine Measurement of Space and Time SOFIST

K. Hara (Univ. Tsukuba)
for SOIPIX Collaboration

筑波大学
University of Tsukuba

SOIPIX
Silicon-On-Insulator Pixel Detector Project

SOFIST development:
U. Tsukuba: K. Hara, D. Yamauchi, R. Abe, S. Iwanami, H. Murayama, K. Watanabe
KEK: T. Tsuboyama, M. Yamada, S. Ono, Y. Arai, Y. Ikegami, I. Kurachi, M. Togawa, J. Haba
Tohoku U.: Li. Taohan

Project supported by
JSPS Grant-in-Aid for Scientific Research on Innovative Areas (2013-2017)

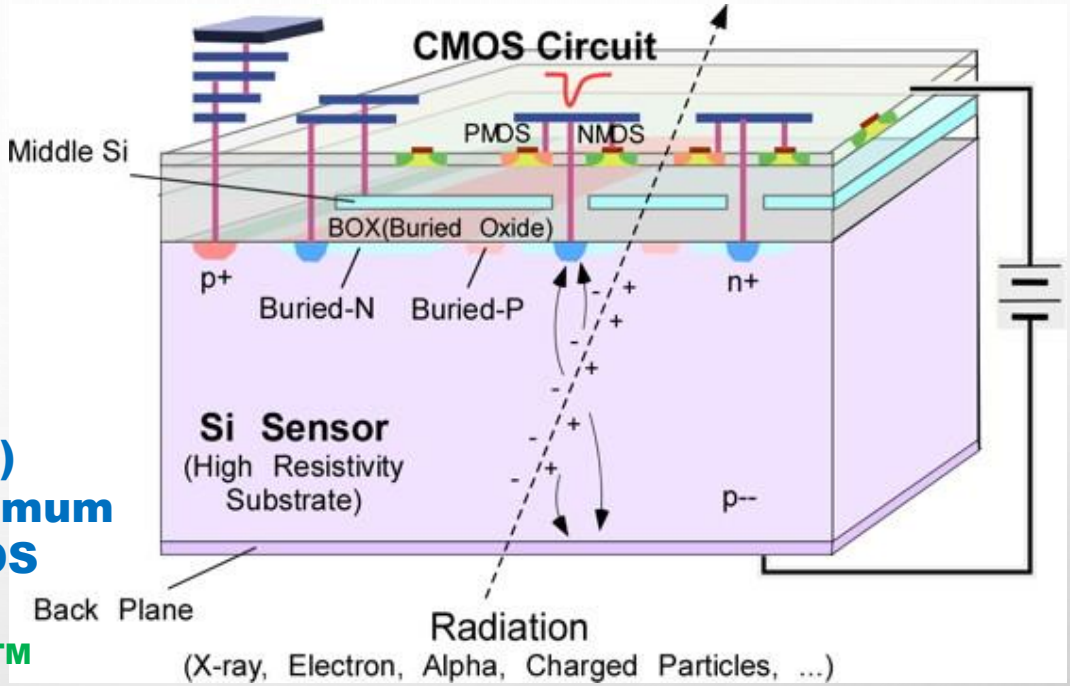
OUTLINE

1. SOI PIXEL Sensor Development – Introduction
2. Highlights of Achievements
3. SOFIST
   - design & developments
   - SOFIST-1 position resolution
   - SOFIST-2 timestamp resolution
   - SOFIST-3 quick evaluation
4. SOFIST-4 3D stacking
5. Summary

SOI PIXEL DEVICES

SOI: SILICON-ON-INSULATOR

CMOS circuitry fabricated on buried oxide(BOX)
LAPIS 0.2um FD-SOI



Features:

- **Monolithic (no metal bumps)**
- **SOI-CMOS (FETs fully isolated)**
- **Can choose* substrate of optimum resistivity (fully depleted CMOS sensors possible)**

***SOITEC SmartCut™**

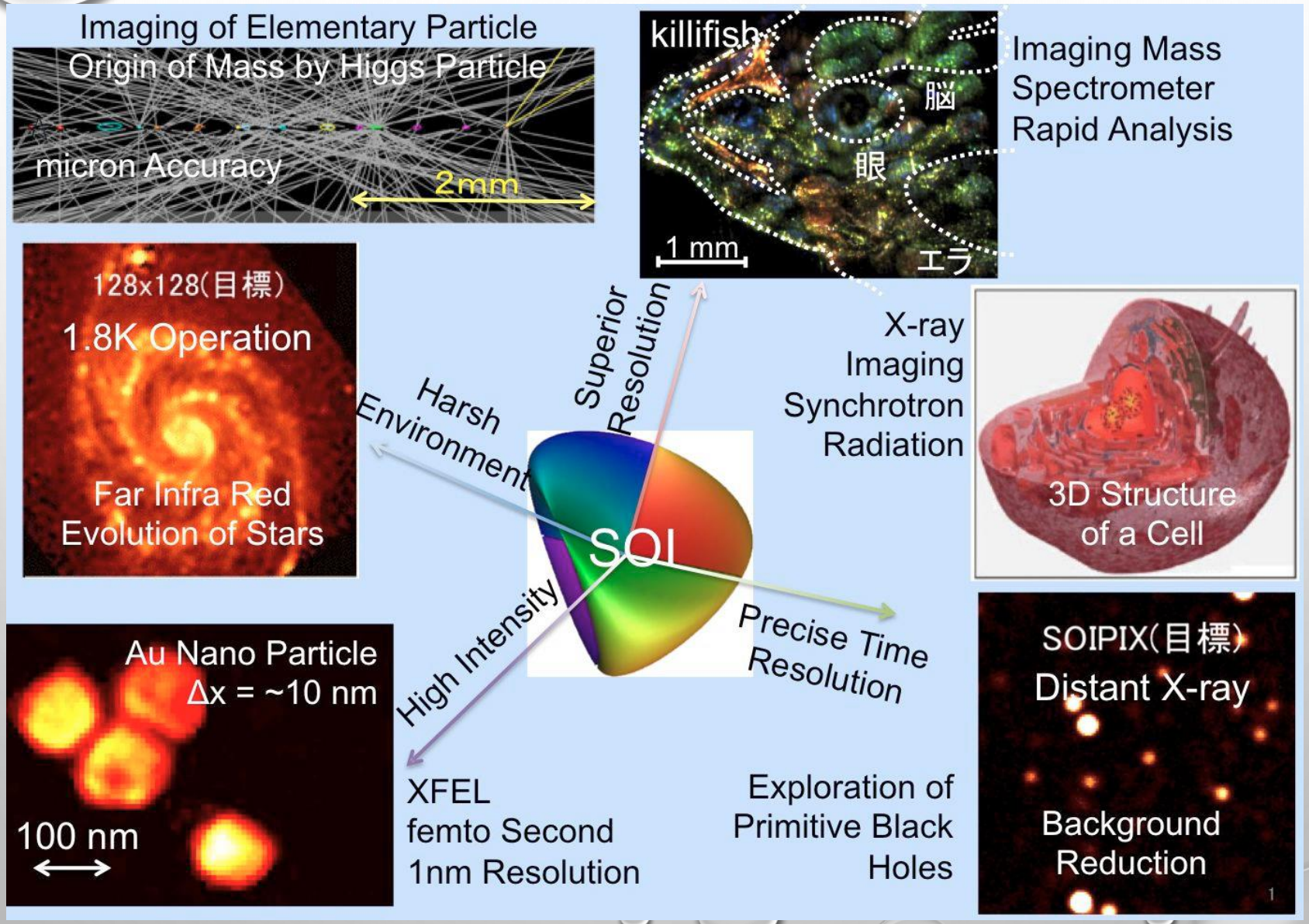
many excellent features

- **Material budget**
- **S/N**
- **power dissipation**
- **speed**
- **cost**
- **Pixel size**
- **single event effects**
- **latch up**
- **Operation temp. (0.3K～570K)**

TID tolerance improved to 1MGy by introducing double SOI wafer (HSTD11)

GRANT-IN-AID (FY2013-17)

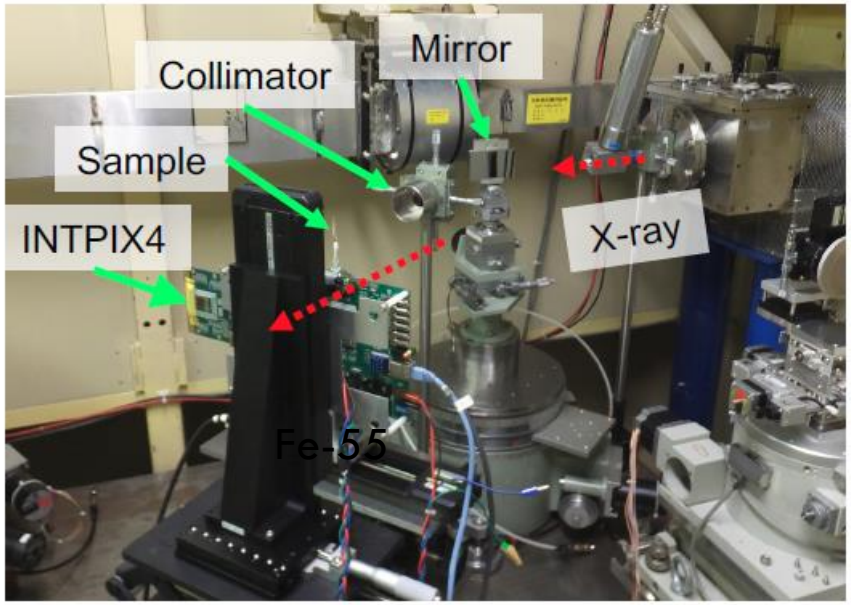
INTERDISCIPLINARY RESEARCH ON QUANTUM IMAGING OPENED WITH 3D SEMICONDUCTOR DETECTOR

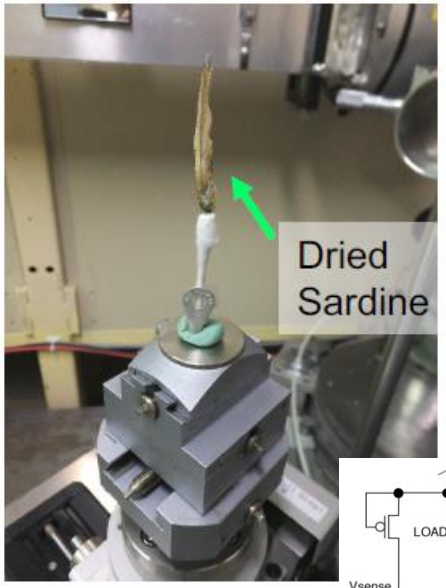


HIGHLIGHT-2 (INTPIX4)

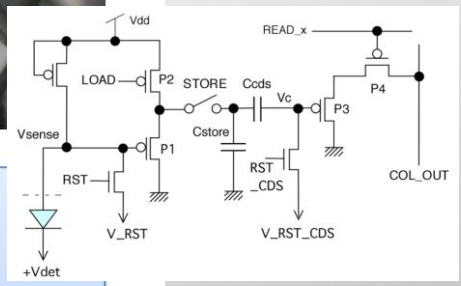
3D CT Imaging at KEK PF

INTPIX

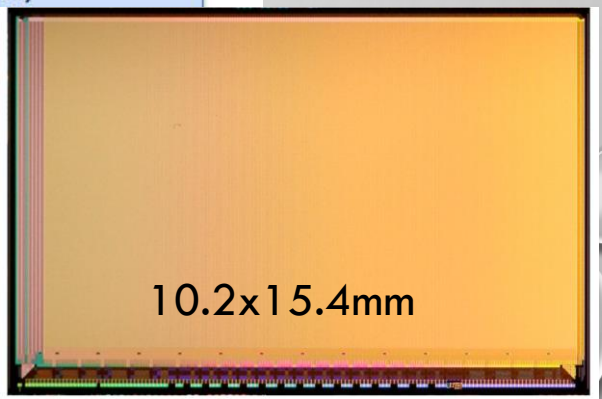




Integration
&global shutter

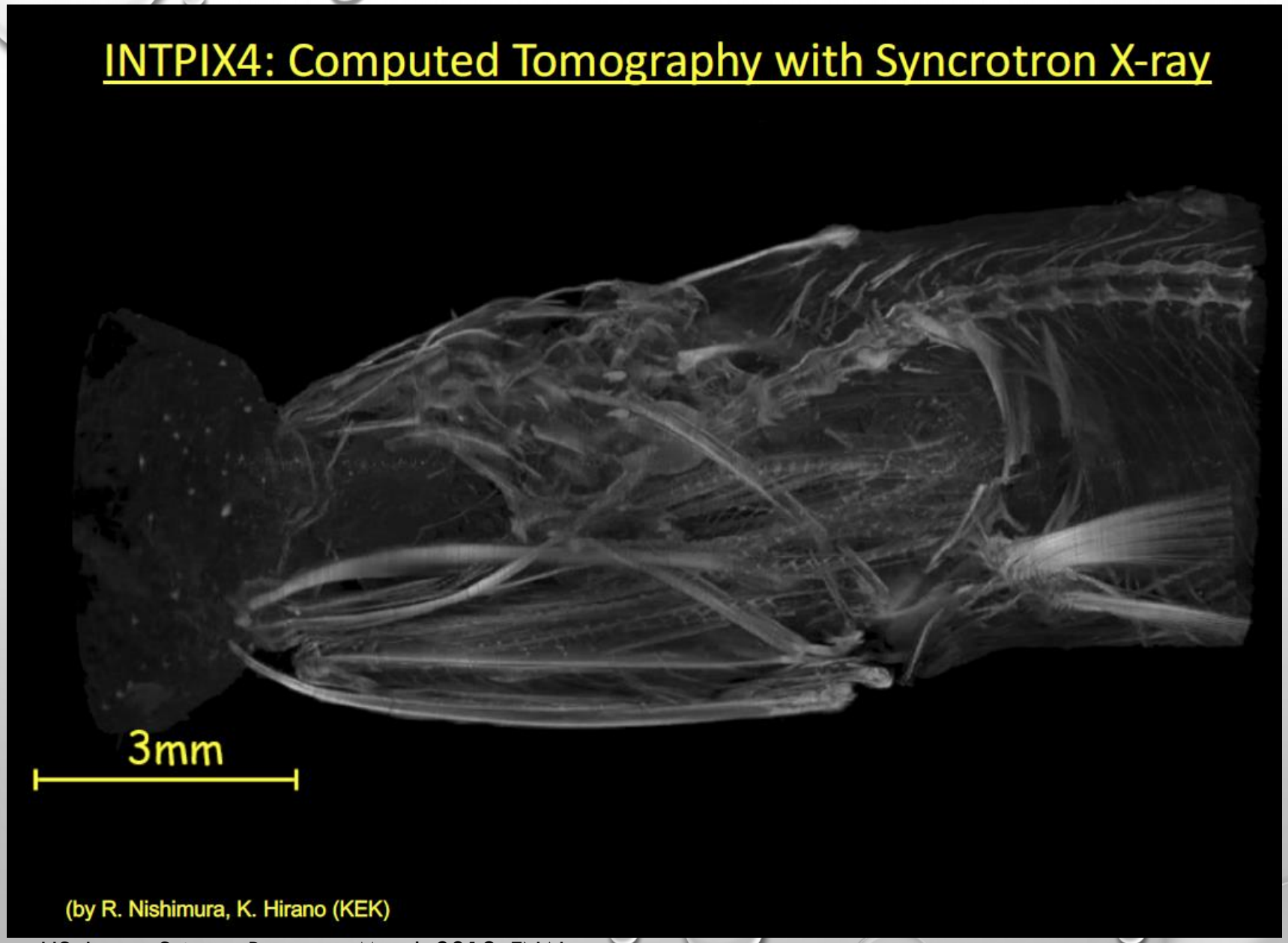


- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V、Integration Time : 1ms、ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0~180° at every 1 degree.

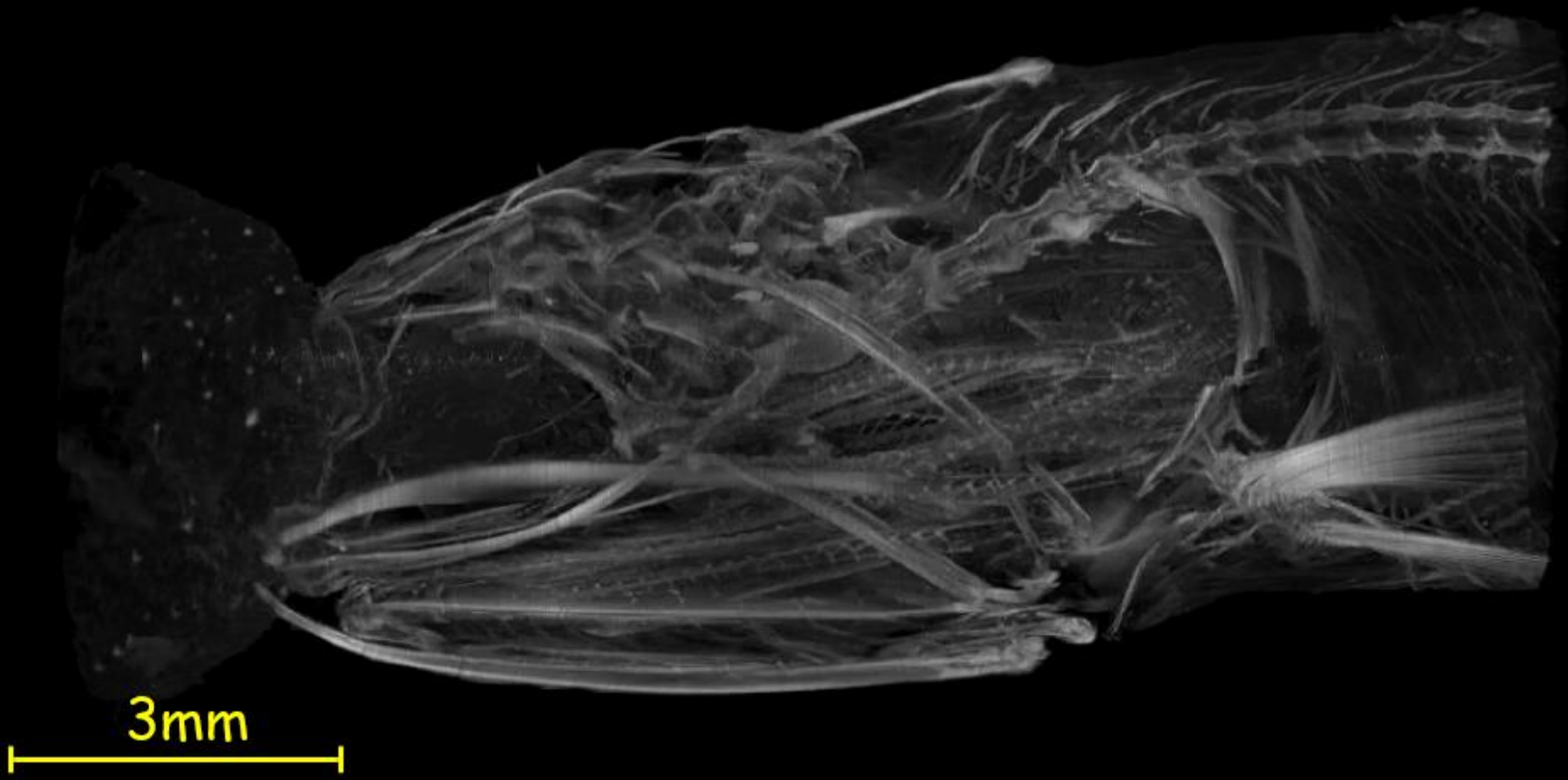


(by R. Nishimura, K. Hirano (KEK)

HIGHLIGHT-2 (INTPIX4)



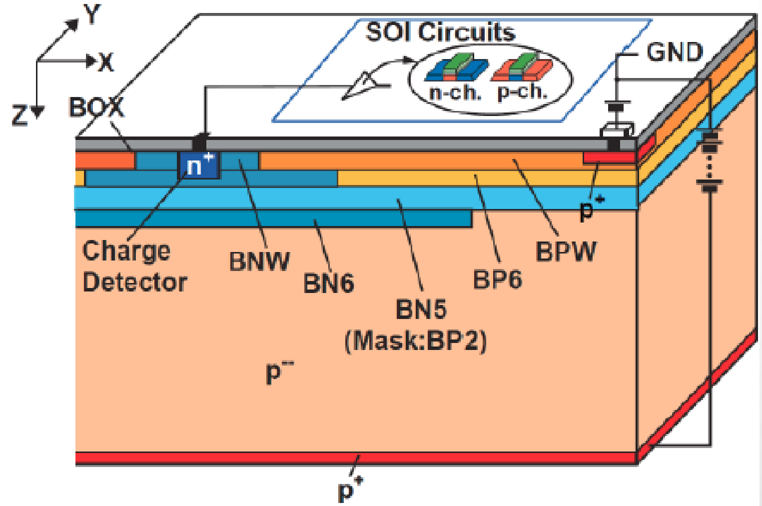
INTPIX4: Computed Tomography with Syncrotron X-ray



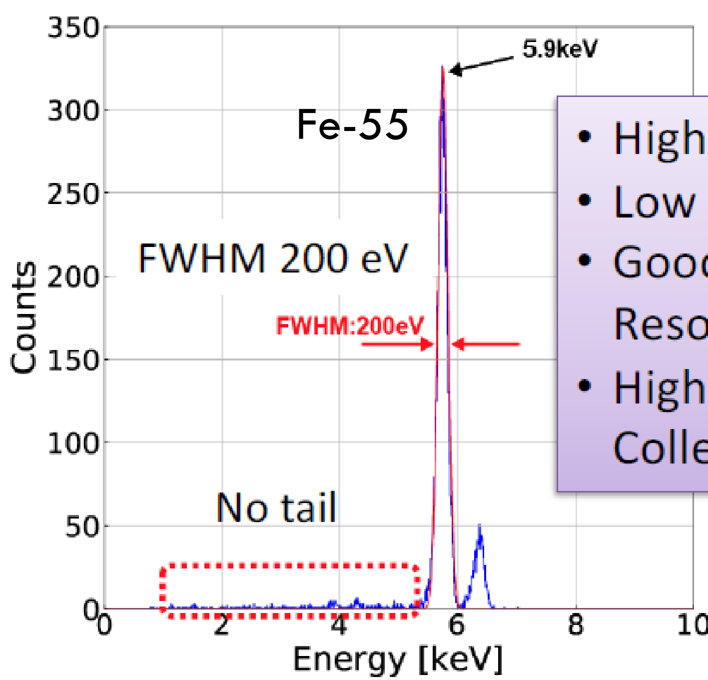
(by R. Nishimura, K. Hirano (KEK)

HIGHLIGHT-1 (SOIPIX-PDD)

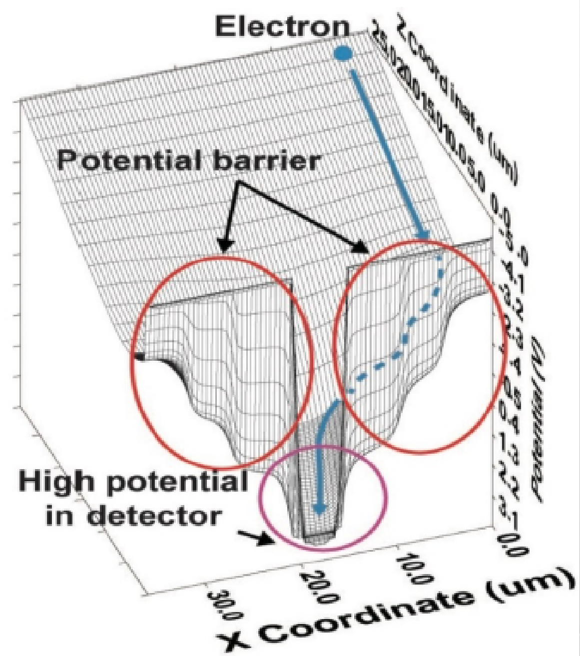
New Sensor Structure: Pinned Depleted Diode (SOIPIX–PDD)



Gain = 70 μV/e-
Noise = 11.0 e-
Dark Current = 57 pA/cm2 @-35˚C

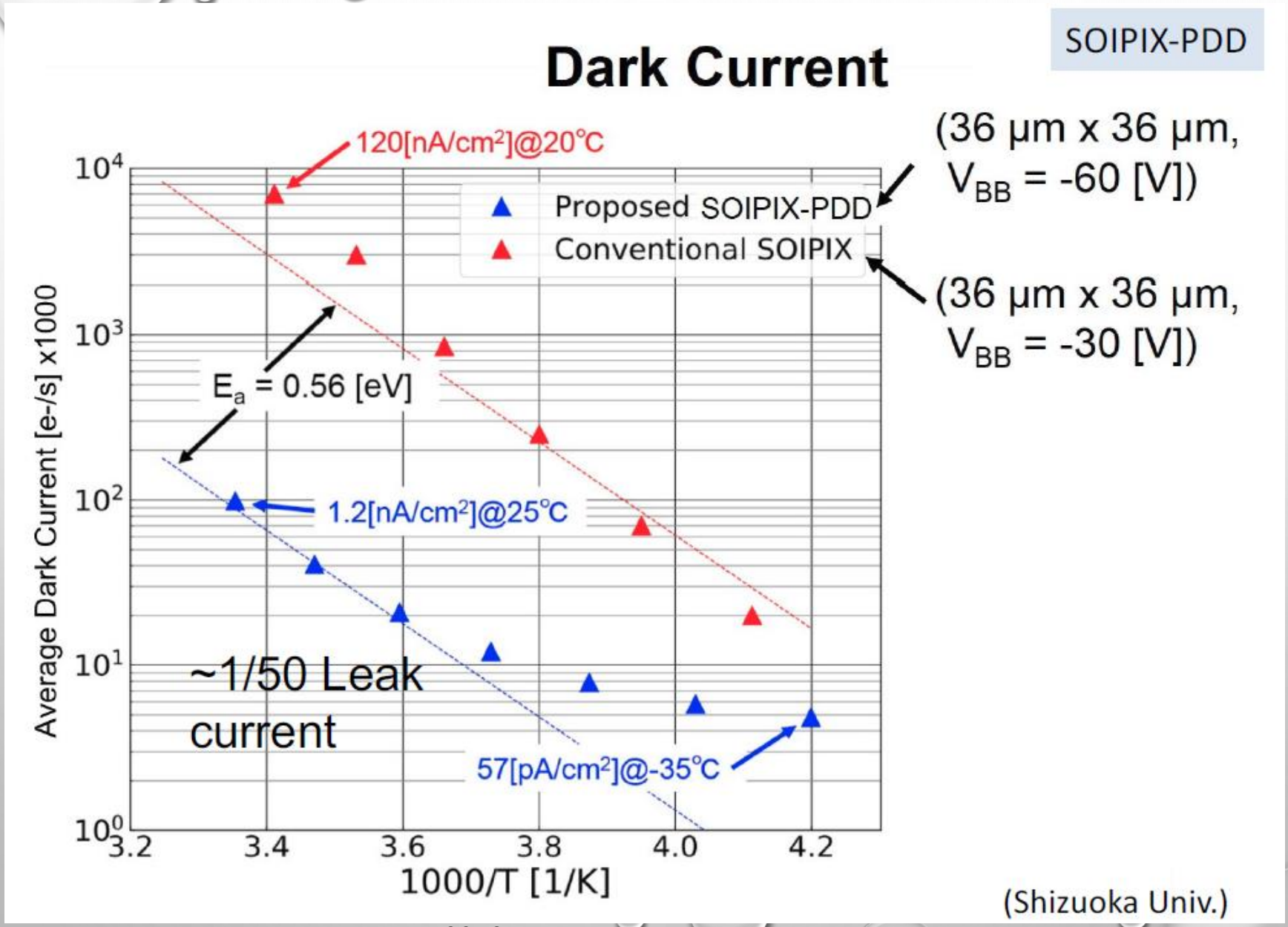


- High Gain
- Low Leak Current
- Good Energy Resolution
- High Charge Collection Efficiency



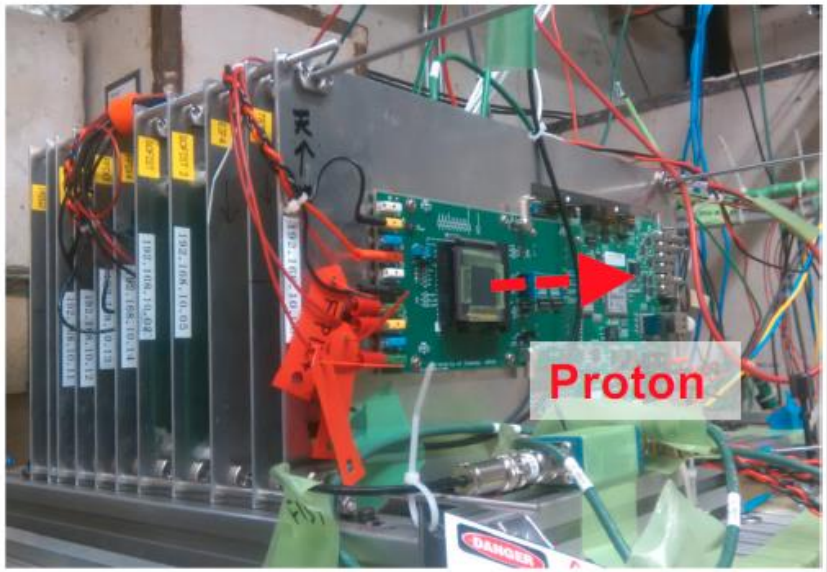
(Shizuoka U.　川人研)

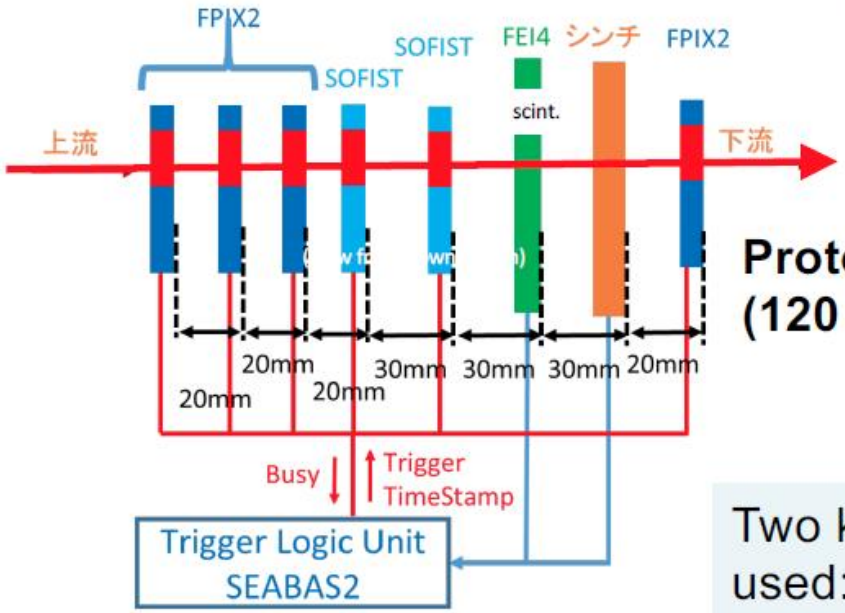
HIGHLIGHT-1 (SOIPIX-PDD)



HIGHLIGHT-3 (FPIX2)

Tracking Resolution:
High-Energy Beam test @Fermi National Accelerator Lab.





Proton Beam (120 GeV/c)

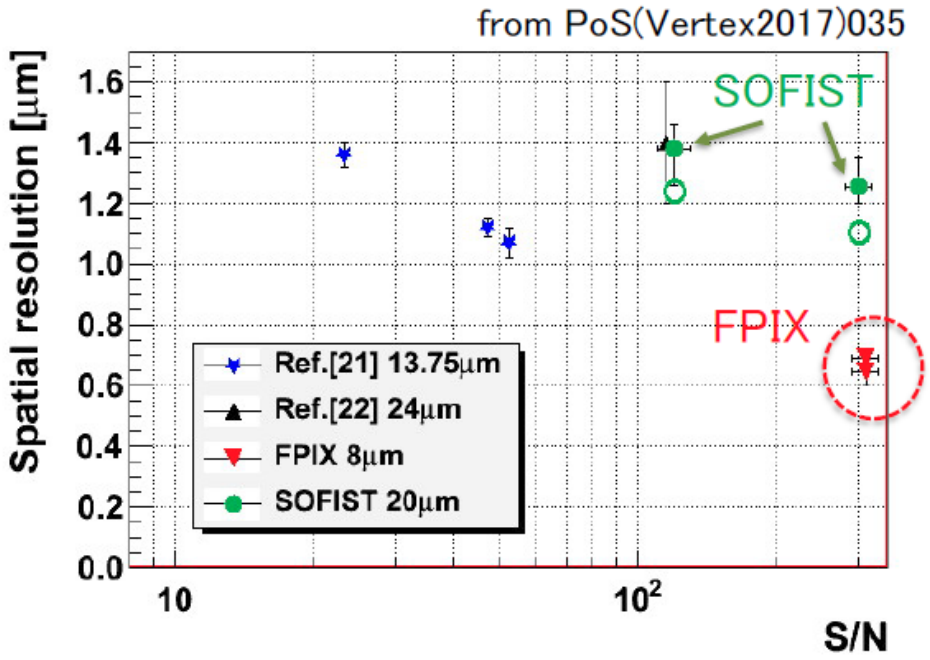
Two kinds of SOIPIX-DSOI detectors are used:

- FPIX2 x 4: 8 μm square pixel detector
- SOFIST1 x 2: 20 μm square pixel detector

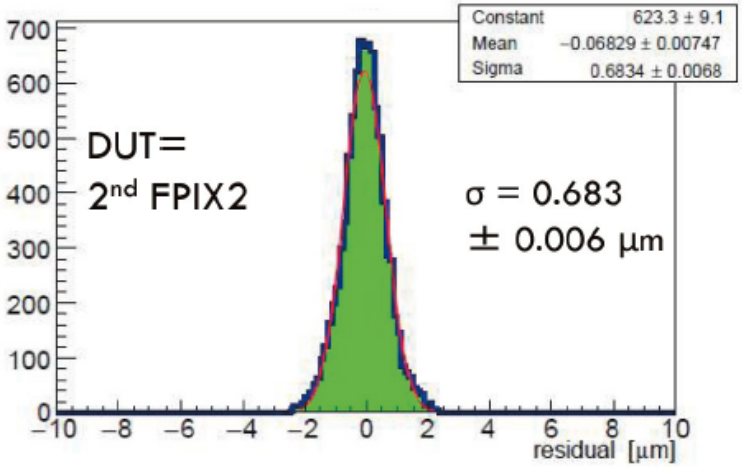
U Tsukuba/KEK

HIGHLIGHT-3 (FPIX2)

SOI Vertex Detector (FPIX、SOFIST)



Detector	Pixel size	Resolution
ATLAS Pix	13.75 μm	1.1 μm
DEPFET	24 μm	1.4 μm
SOFIST	20 μm	1.2 μm
FPIX	8 μm	**0.65 μm**

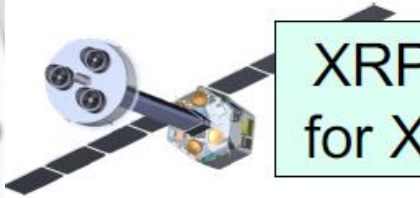


Better than 1 μm Position Resolution for high-energy charged particle is achieved first in the world !

Concurrent Timing Measurement with 1.9 ~~1.6~~μs resolution is also performed.

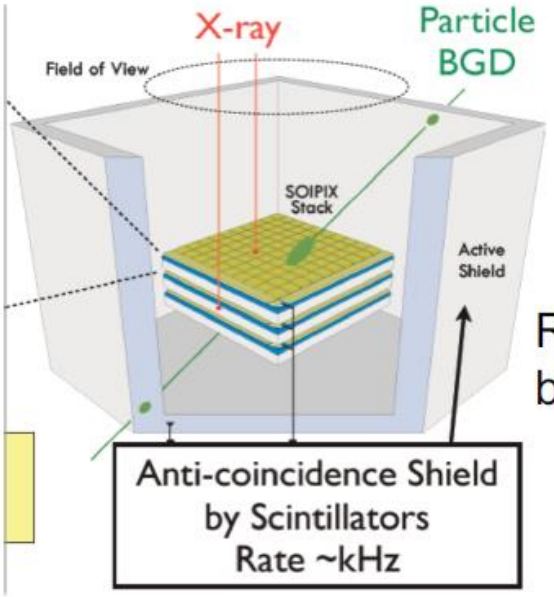
Ref.[21] ATLAS sensor, ATLAS-CONF-2013-005
Ref.[22] DEPFET detector, https://cds.cern.ch/record/1967037

HIGHLIGHT-4 (XRPIX5)



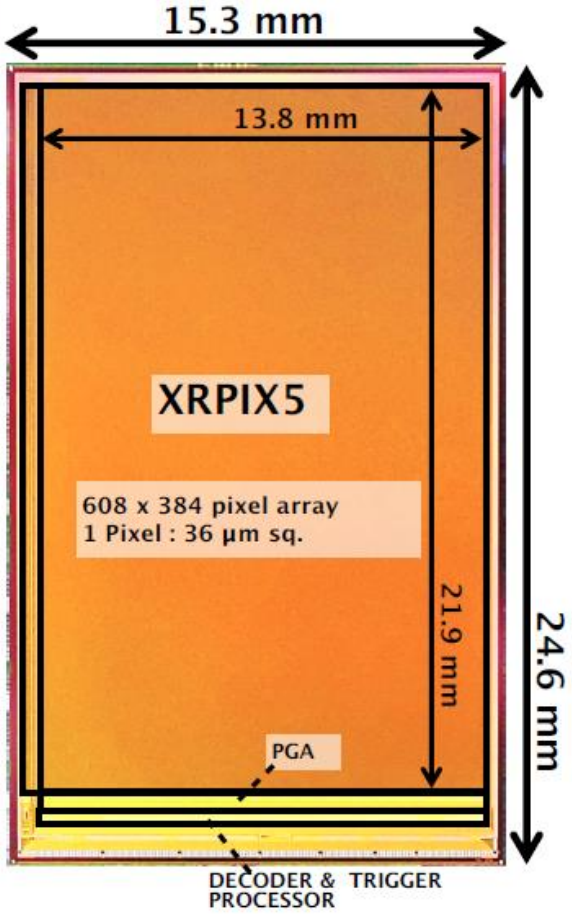
XRPIX: Event-Driven Detector for X-ray Astronomical Satellite

Timing resolution of CCD is too poor to make anti-coincidence.



Prompt hit signal generation

Remove cosmic-ray back ground.

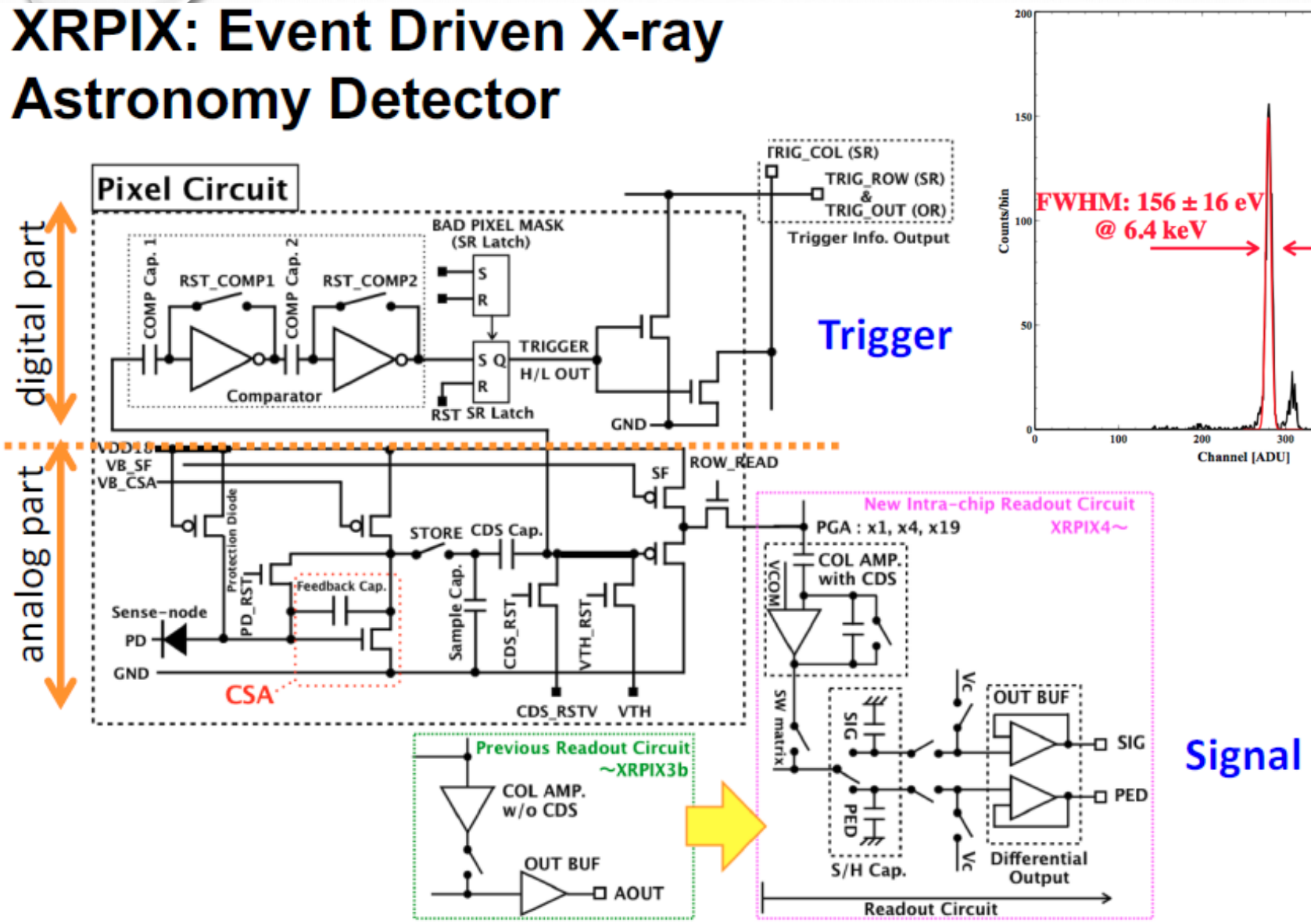


Aiming to install in the next satellite FORCE (Forcusing On Relativistic universe and Cosmic Evolution)

(Kyoto U. etc.)

HIGHLIGHT-4 (XRPIX5)

XRPIX: Event Driven X-ray Astronomy Detector



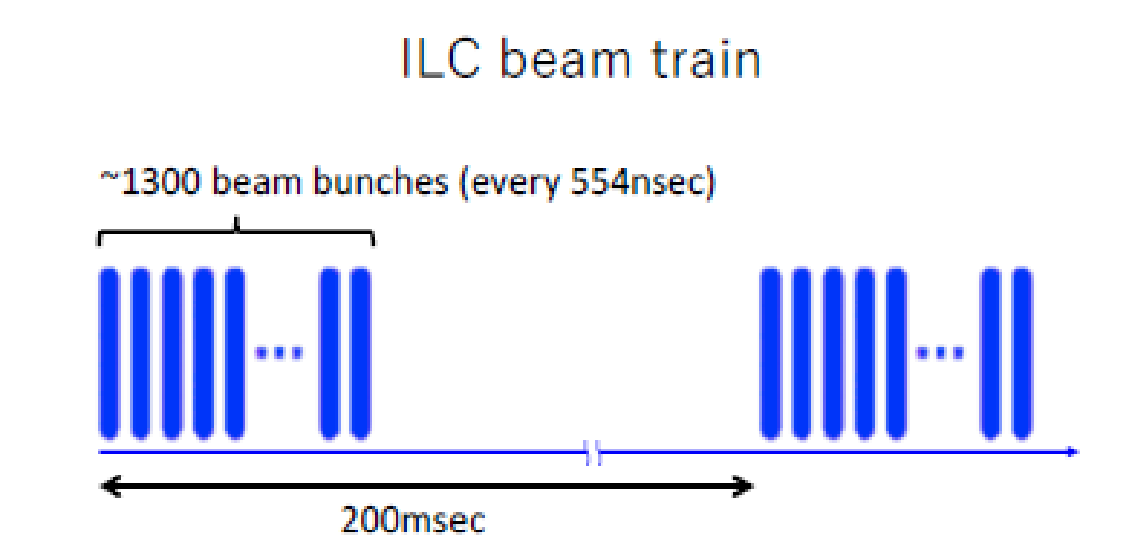
HIGHLIGHT-4 (XRPIX5)

	Hitomi CCD	eROSITA pnCCD	XRPIX
Pixel Size	24 μ m	75 μ m	36 μ m
No. of Pixel	1200 x 1200	384 x 384	608 x 384
Depletion Thickness	200 μ m	450 μ m	300 μ m
Energy Resolution (@6.4keV)	165eV	150eV	156eV (Test Chip、1 pix)
Timing Resolution	4 sec	50 msec	→ 10 μsec x5000 fast !
Anti Coincidence	X	X	O
Operating Temp.	−120℃	−95℃	−20℃

Energy resolution as good as CCD's
Much faster!
Muon veto possible

SOFIST SOI MONOLITHIC PIXEL DETECTOR FOR FINE MEASUREMENT OF SPACE AND TIME

Allows time and space point measurement
Design specified to meet the requirements for the ILC experiment



Main requirements:

- Position resolution <3um
- Low material <0.2%Xo/layer
- TID~1kGy/year
- NIEL ~$10^{11} n_{eq}/cm^2$/year

Readout between trains
bunch ID highly preferred
Power dissipation: <50mW/cm^2

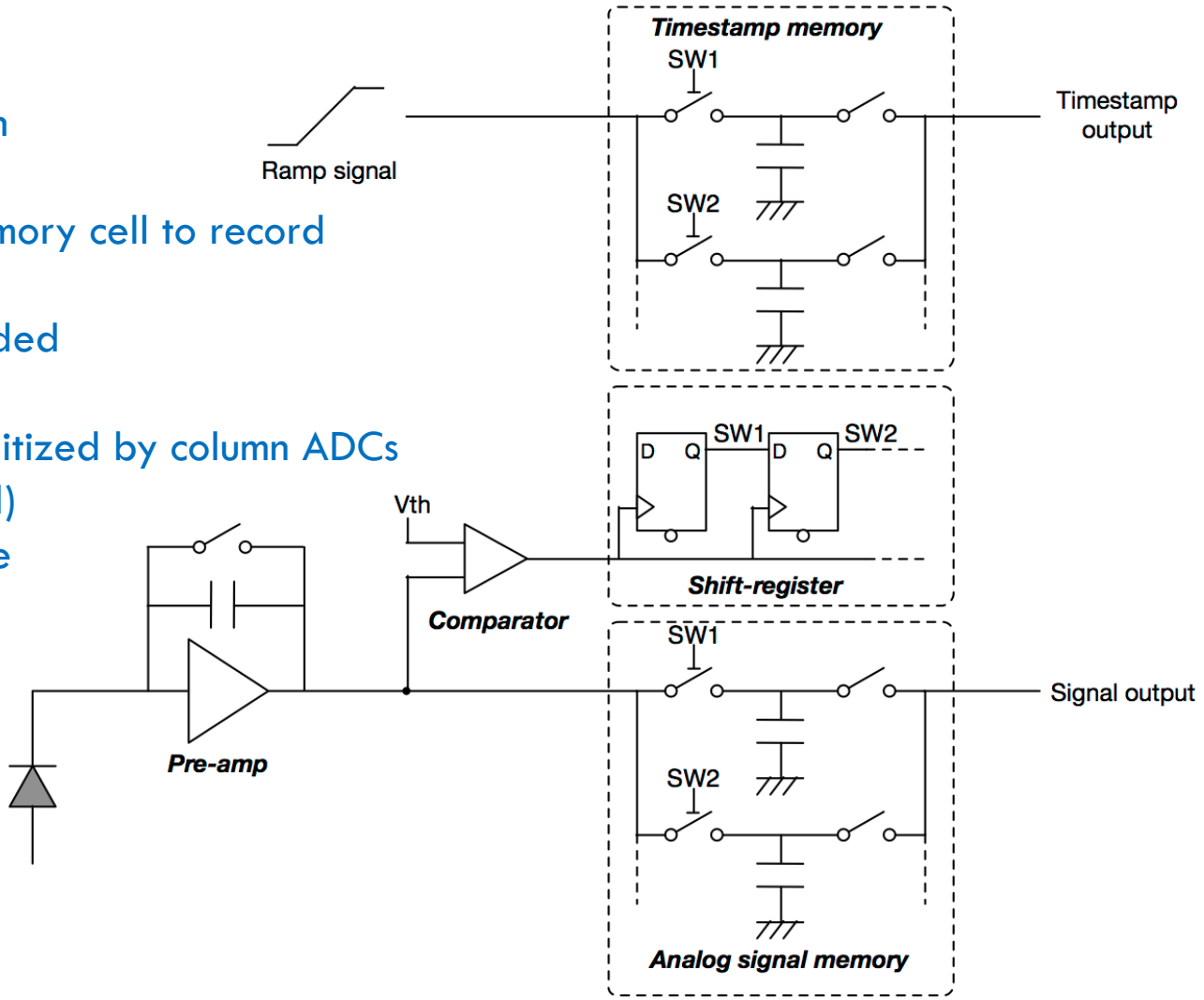
The goal is a sensor with both good spatial resolution of <3um and time resolution <1us.

- ✓ pixel size ~20um-sq with analog readout
- ✓ timestamp recording the ramping voltage
- ✓ store the data allowing multiple hits on the same pixel
- ✓ on-chip ADCs &zero-suppression for fast data transfer

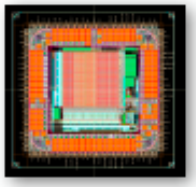
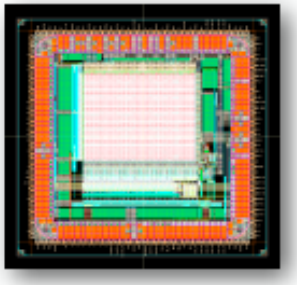
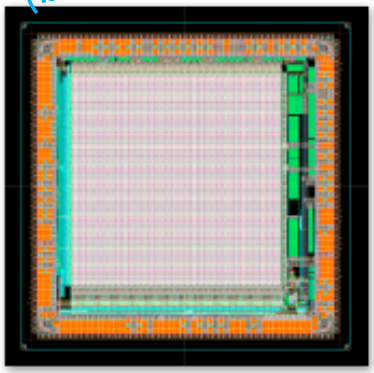
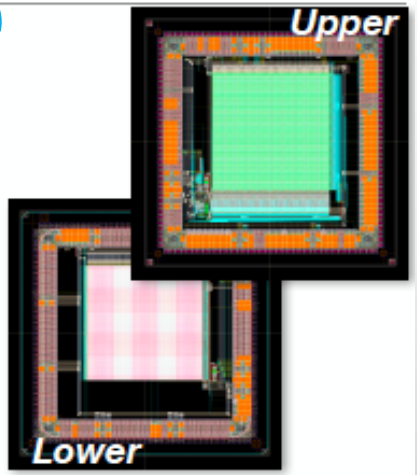
SOFIST PIXEL ARCHITECTURE

Start Vramp per beam train
Signals exceeding Vth
shift-register chooses* memory cell to record
analog signal recorded
timestamp voltage recorded

Recorded memories are digitized by column ADCs
(8bit has been implemented)
Zero-suppression applicable



SOFIST – IN DEVELOPMENT

	MX1850	MX2040	MX2166	
SOFIST	ver.1	ver.2	ver.3	ver.4 (3D)
	FNAL Beamtested (only analog)	FNAL Beamtested (both but in separate pixels)	Under evaluation (both in same pixel)	
				
Chip Size (mm^2)	2.9 x 2.9	4.45 x 4.45	6 x 6	4.45 x 4.45
Pixel Size (μm^2)	20 x 20	25 x 25	30 x 30	20 x 20
Pixel Array	50 x 50	64 x 64 (Time Stamp) 16 x 64 (Analog Signal)	128 x 128	104 x 104
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n* -type (Single SOI)	Cz *p* -type (Double SOI)	FZ *p* -type (Double SOI)	FZ *p* -type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Under evaluation	Delivered (Jan. 2017)		

delivered — Under 3D

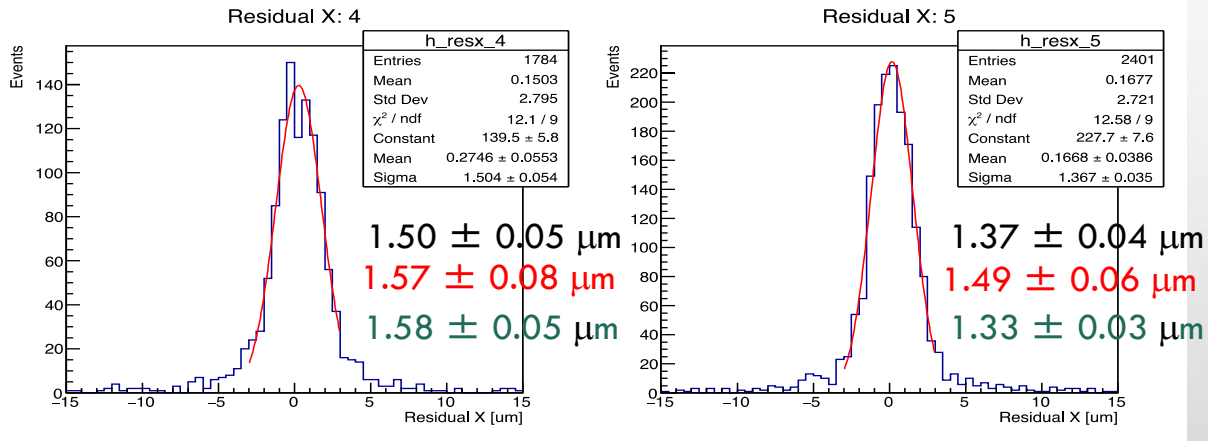
SOFIST-1 SPATIAL RESOLUTION

SOFIST residual to FPIX track (σ_track~0.57/0.65μm)
Bias=130V (~500um depletion) =>15V (~200μm depletion)
Readout: external 12-b ADCs =>on-chip 8-b ADCs

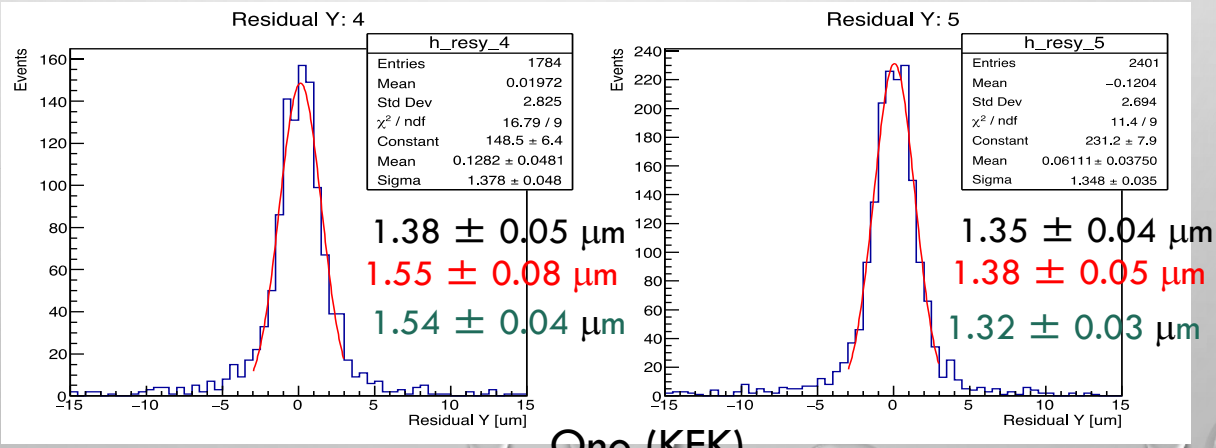
SOFIST#1(BPW14x14) SOFIST#2(BPW16x16)

plots for "black case"

Residual X



Residual Y



S/N~300 (130V)
~120 (15V)

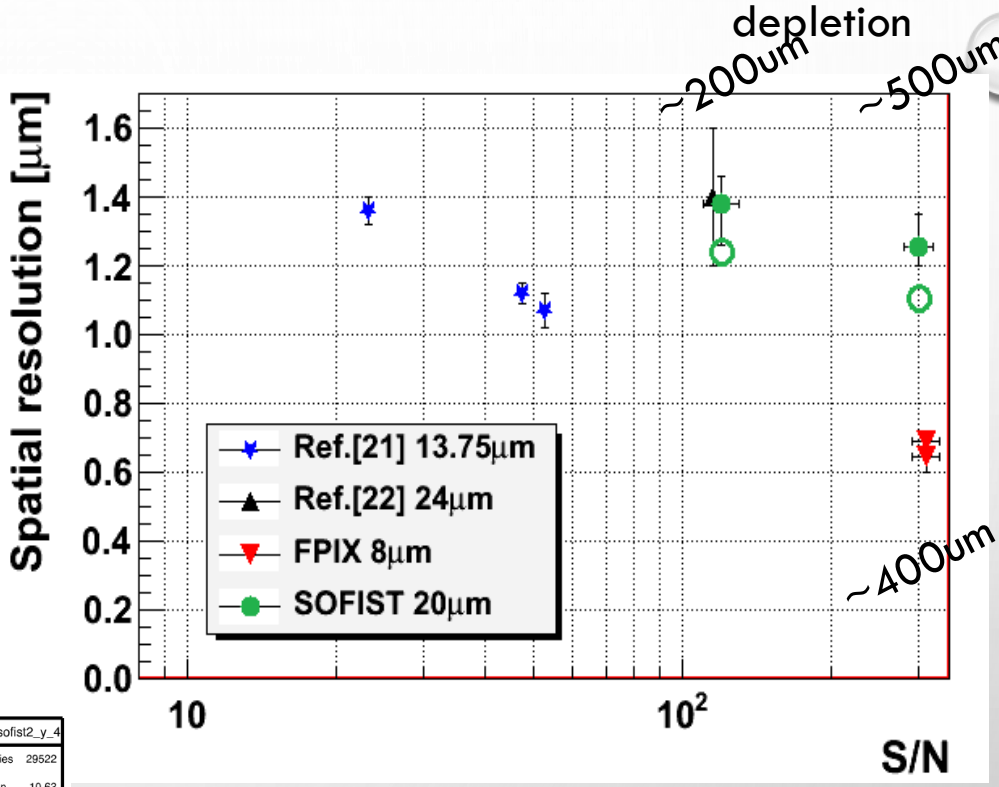
Ono (KEK)

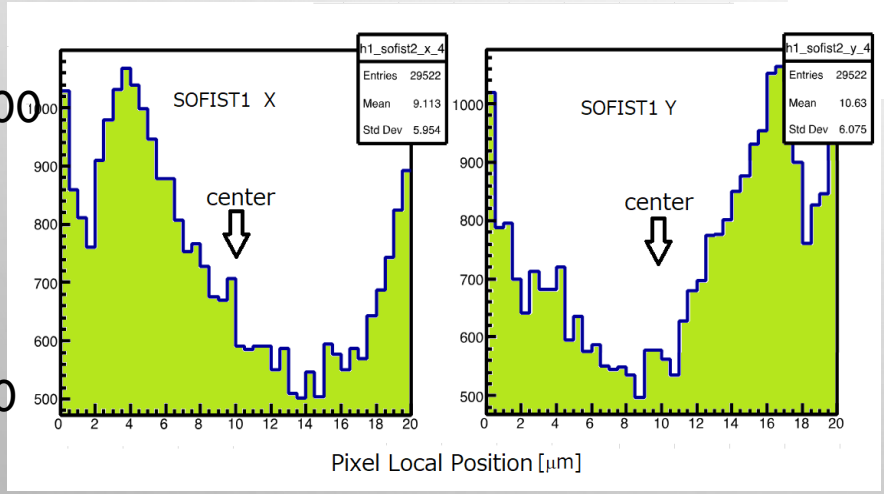
SOFIST-1 SPATIAL RESOLUTION

- Track uncertainty (0.6um) subtracted

  Compatible with DEFFET ([22])

- η correction may improve further

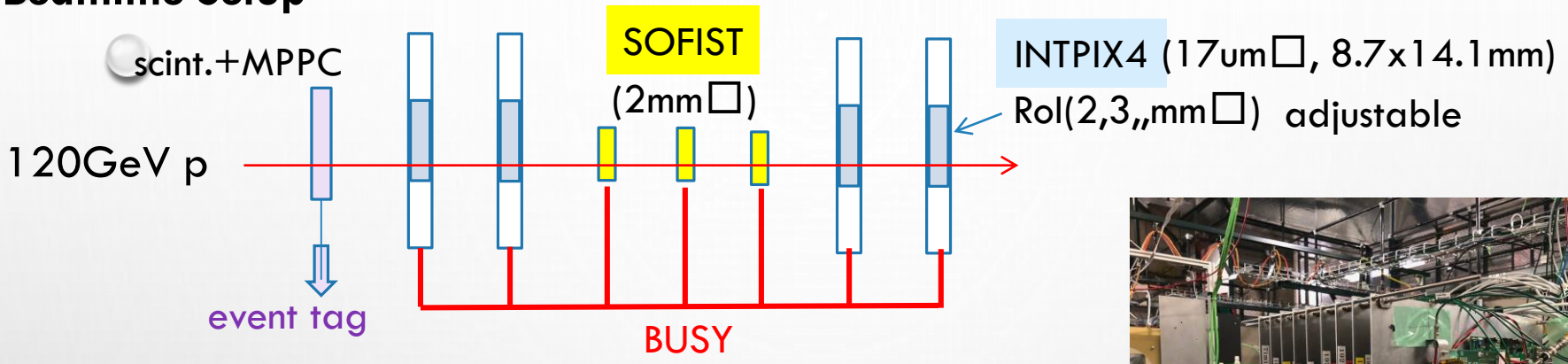


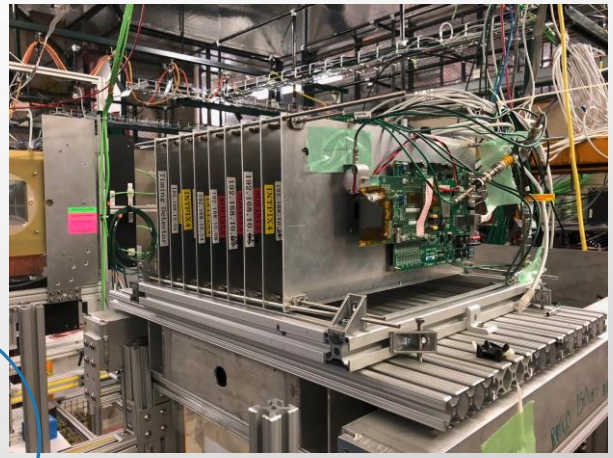


Ono (KEK)

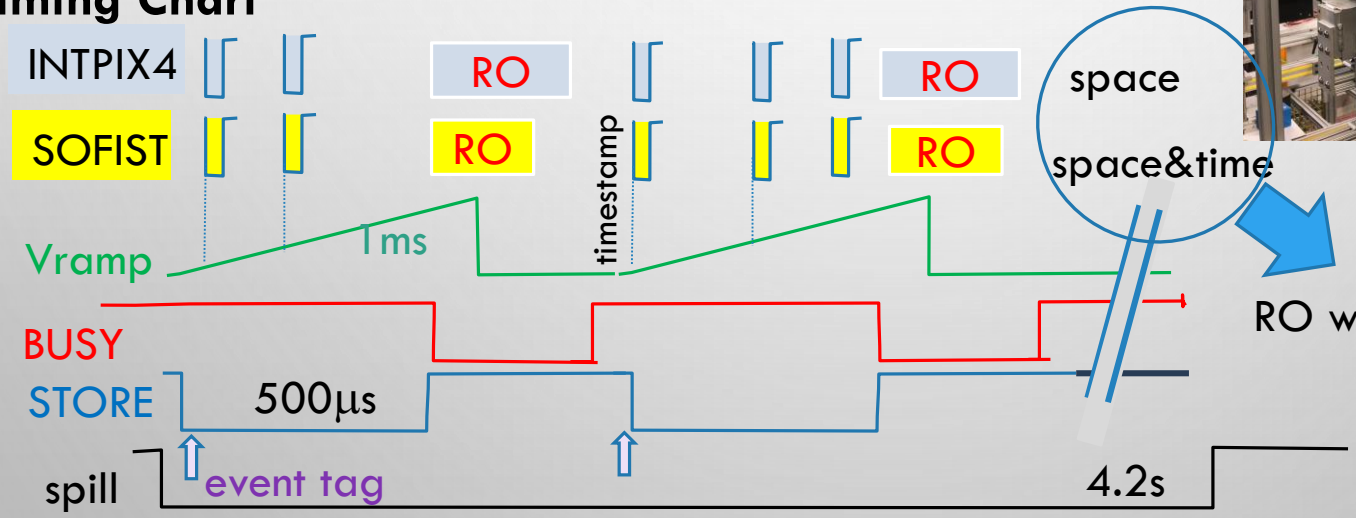
SOFIST-2 BEAM TEST 2018MAR

Beamline Setup





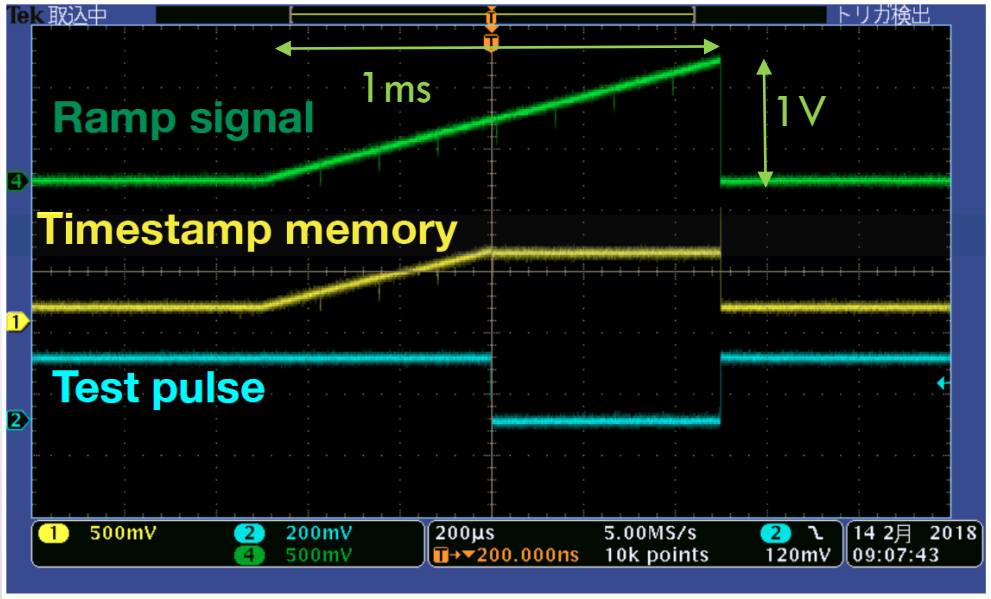
Timing Chart

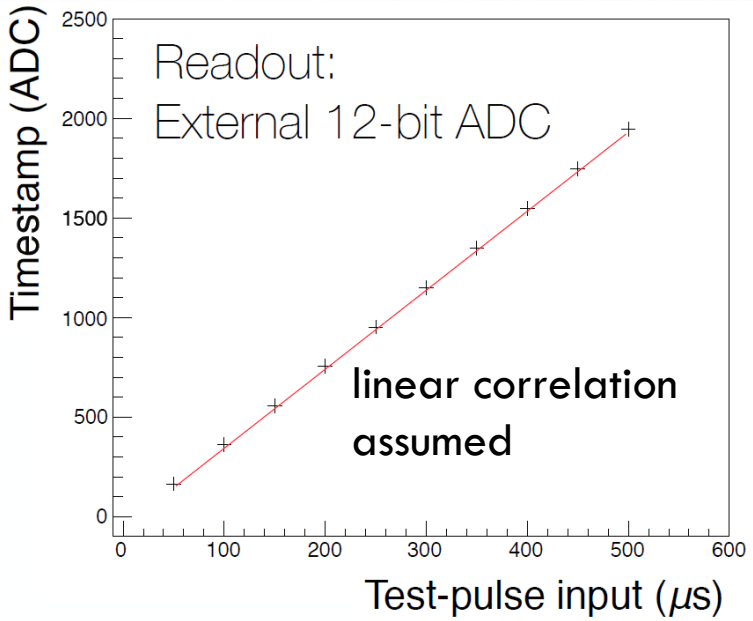


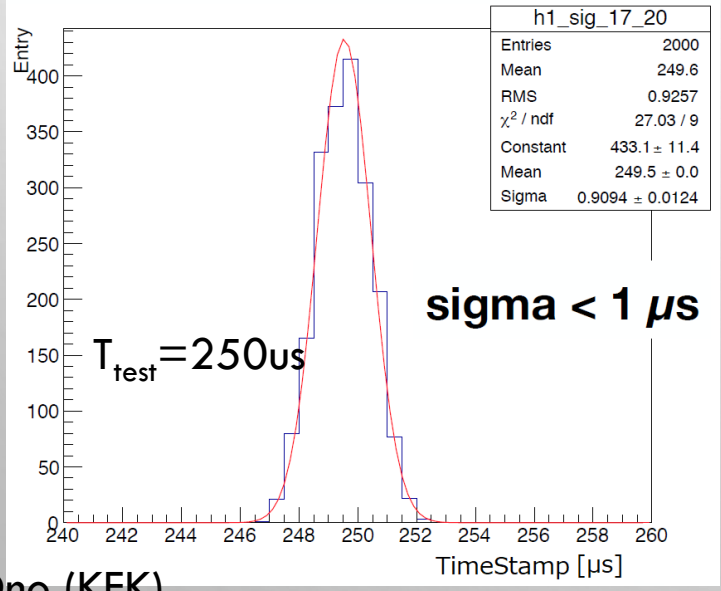
RO with external 12-bit ADCs

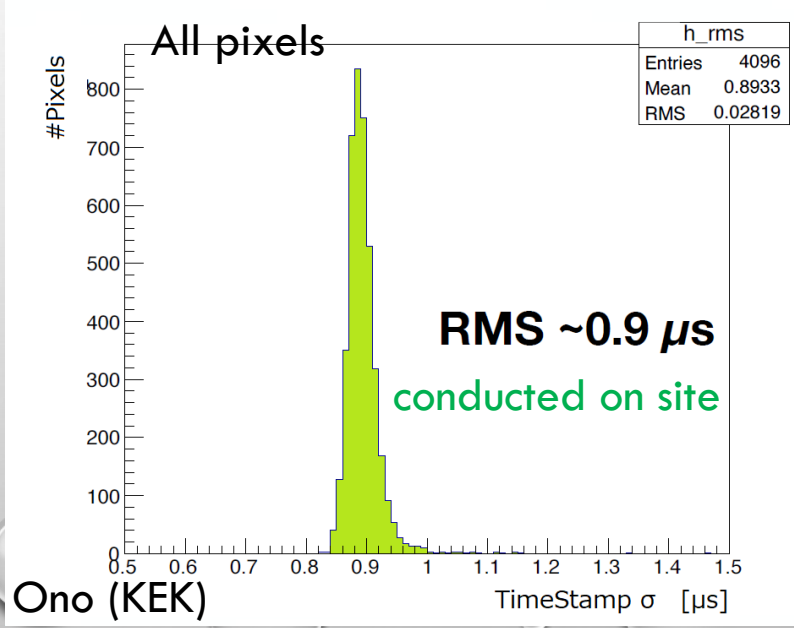
SOFIST-2 TIMESTAMP CALIBRATION

conducted on site







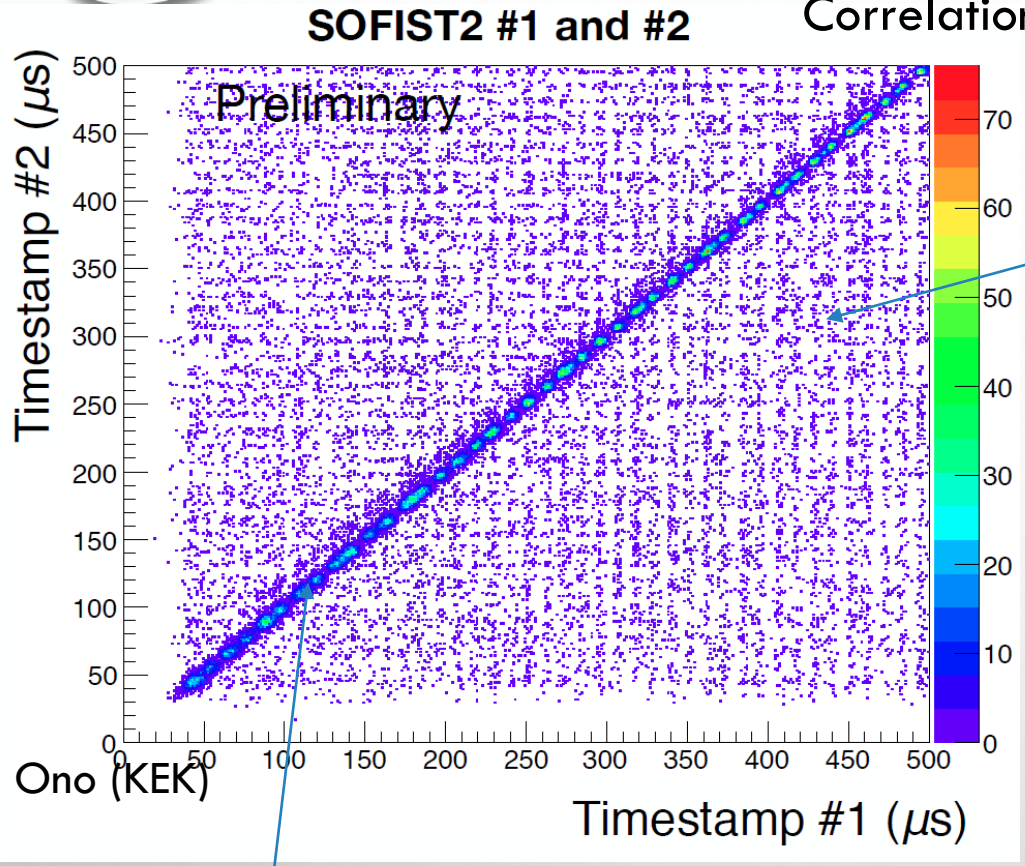


Ono (KEK)

Ono (KEK)

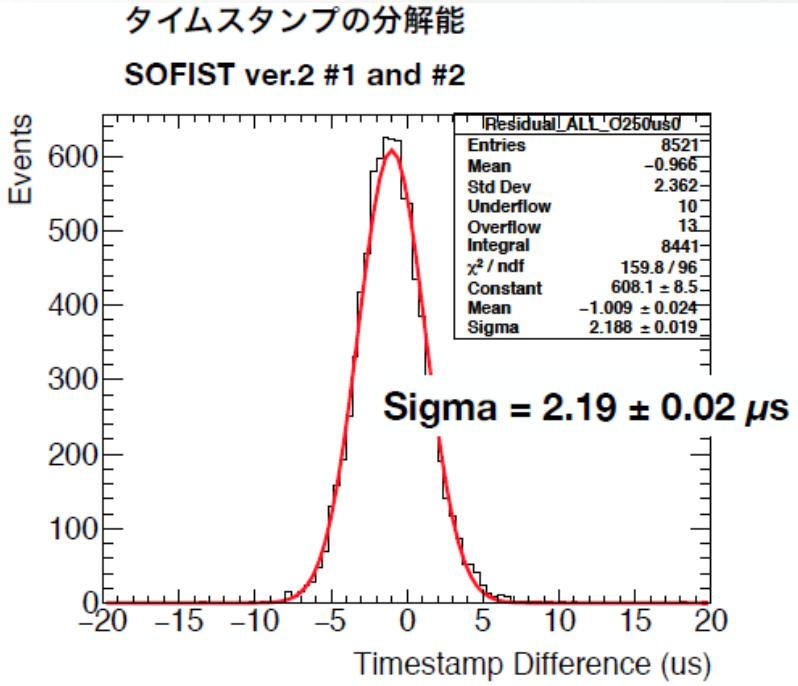
SOFIST-2 TIMESTAMP CORRELATION

Correlation of timestamps in two SOFISTs



Ono (KEK)

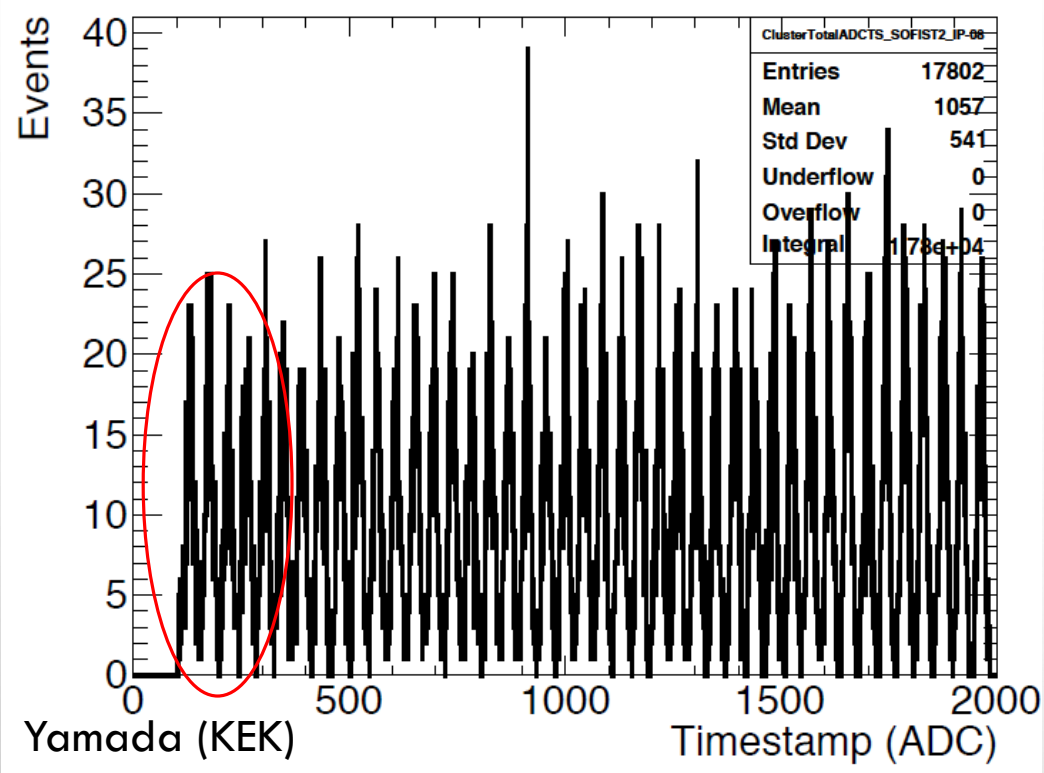
Overlapping events in same 500us gate

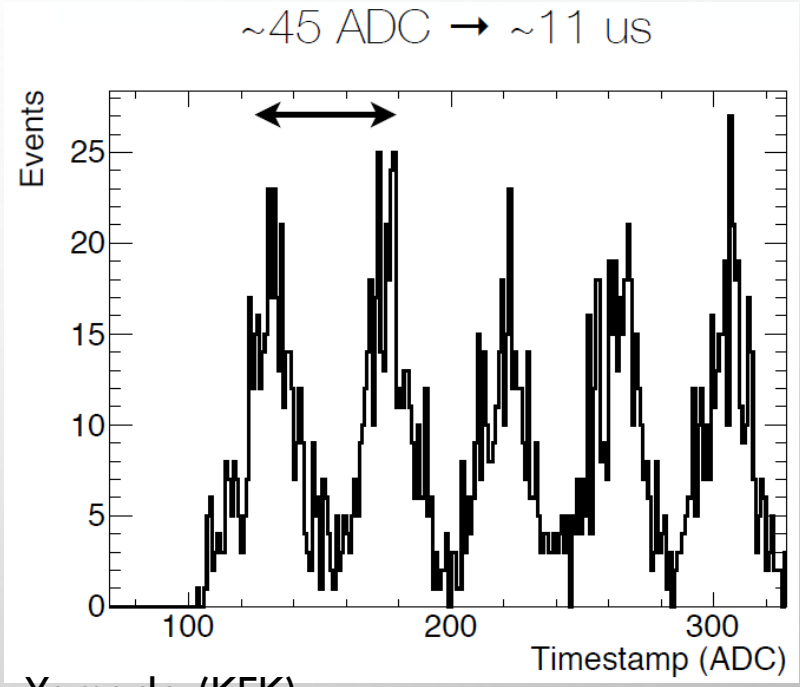


Intrinsic resolution: 2.19/√2 ~ 1.55 μs

Periodic clusters?

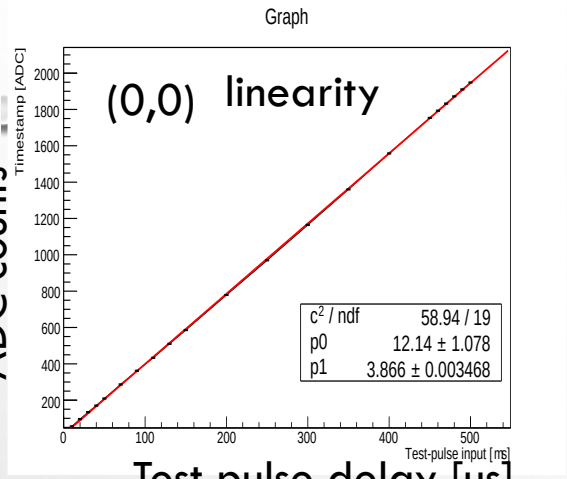
SIZE OF FNAL MAIN INJECTOR (MI)





Beam structure due to bunch rotation in the MI: 11us→3.3km (3319m actual)

SOFIST-2 TIMESTAMP PRECISION

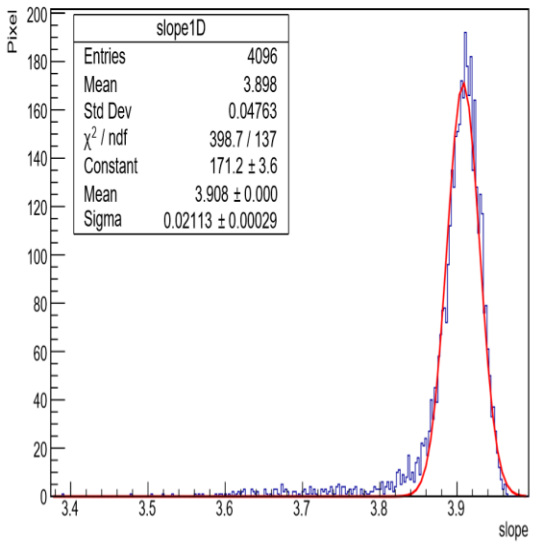


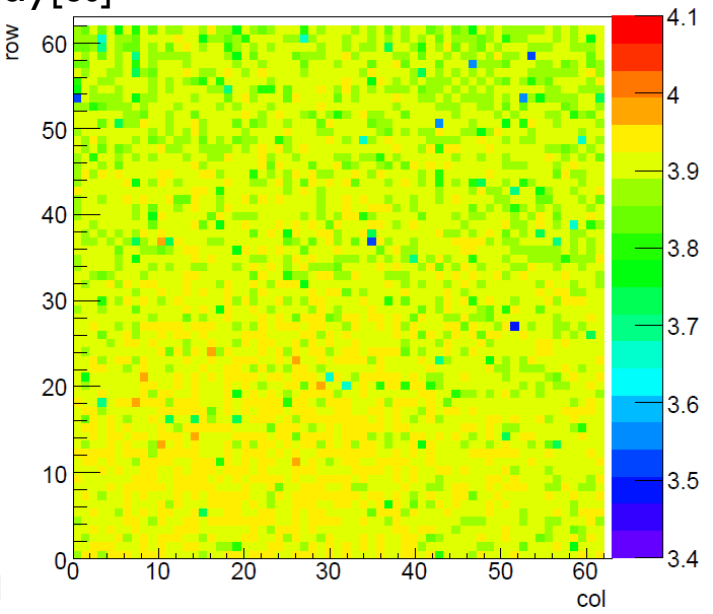
Test pulse delay [us]

Murayama (Tsukuba)

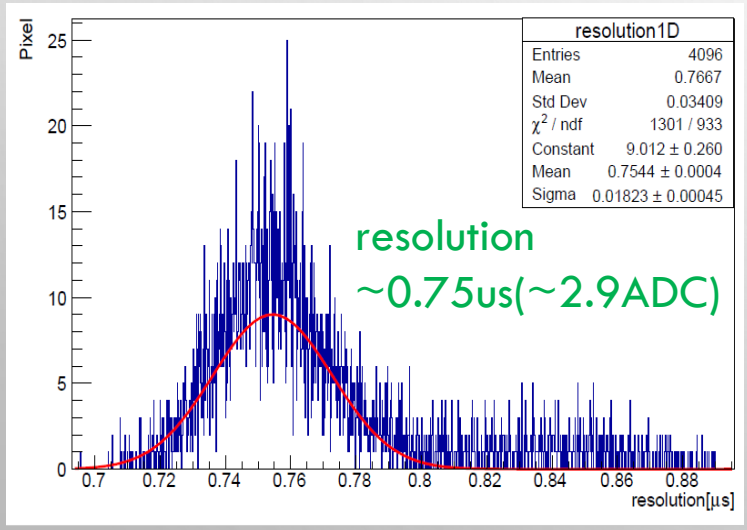
conducted on testbench

ΔADC/Δdelay[us]

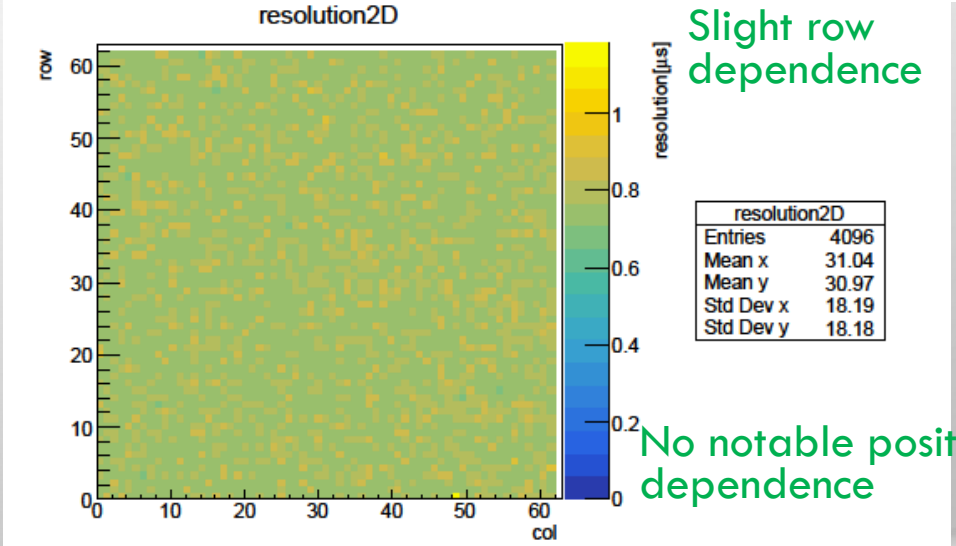




Time spread for 500us delay pulses



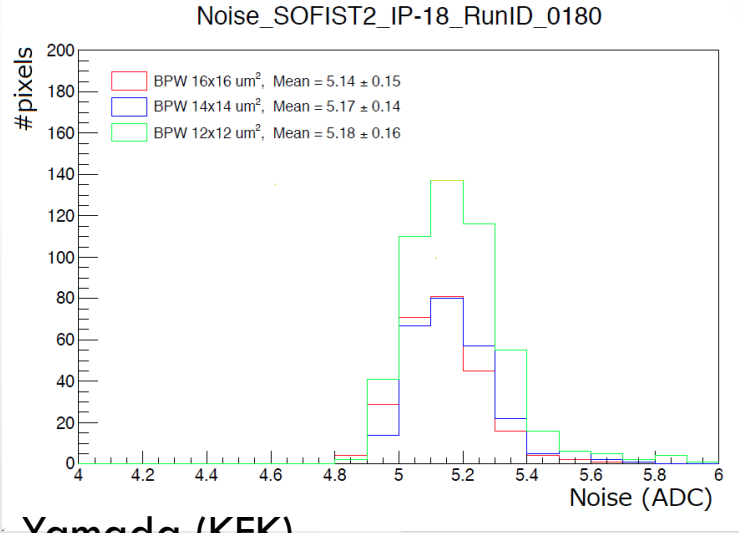
resolution
~0.75us(~2.9ADC)

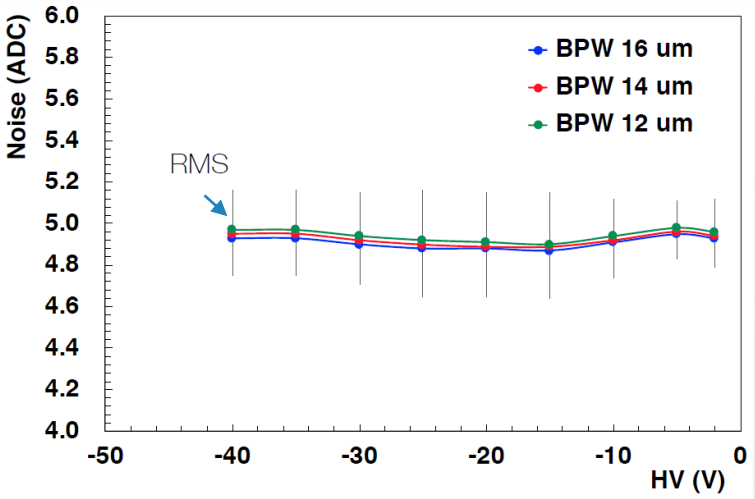


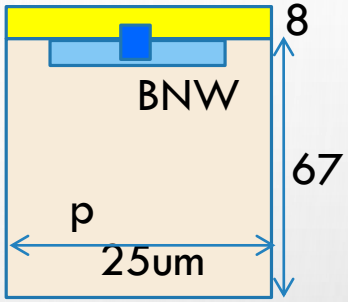
Slight row dependence

No notable position dependence

SOFIST-2 ANALOG SIGNAL

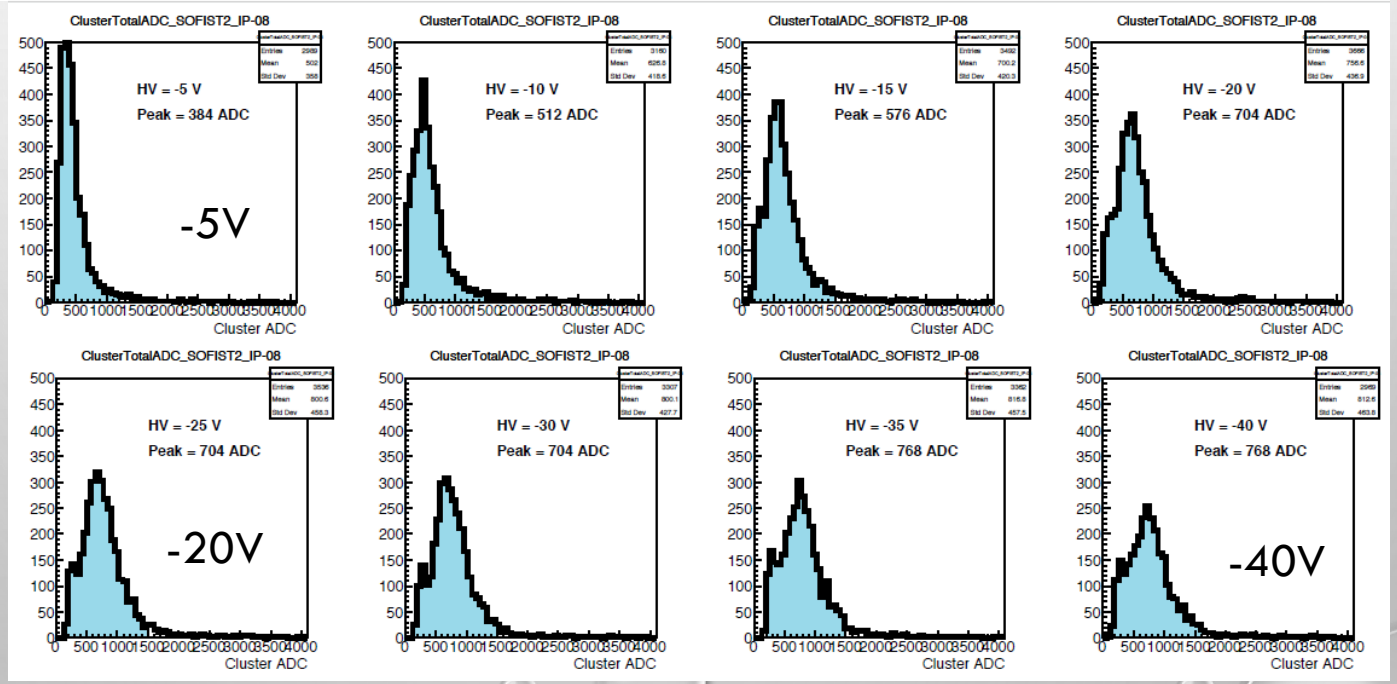






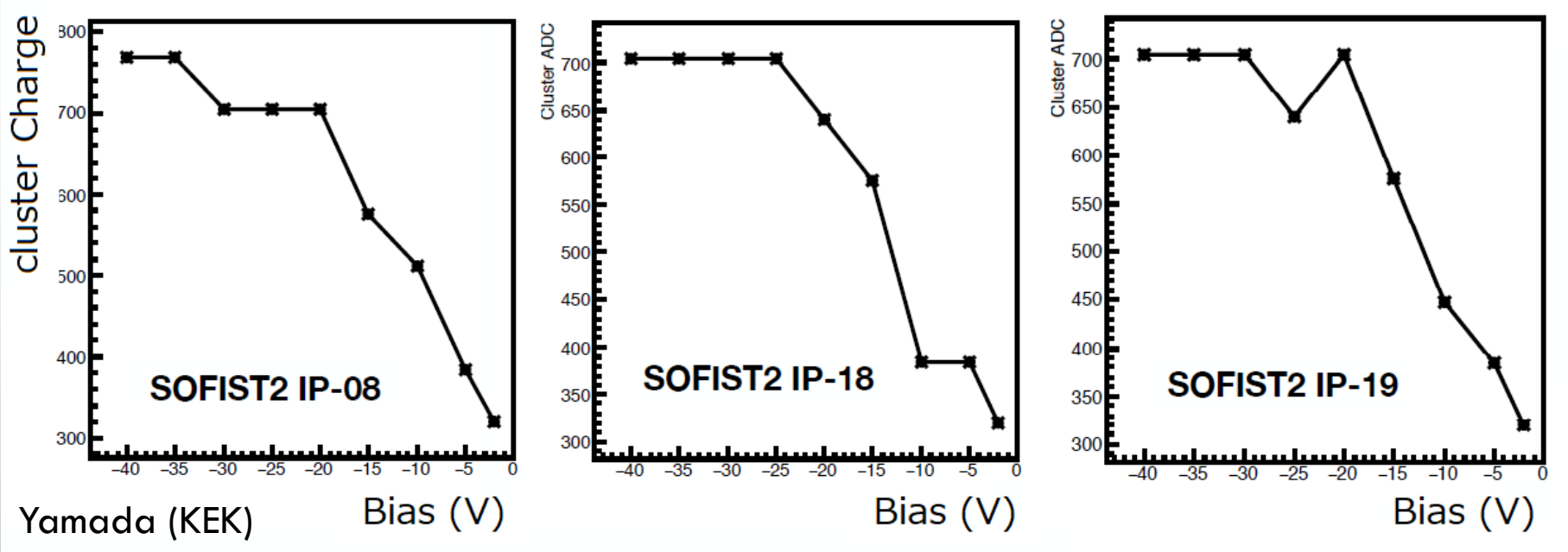
Yamada (KEK)

Cluster charge
(HV dependence)



Yamada (KEK)

SOFIST-2 FULL DEPLETION



Yamada (KEK)

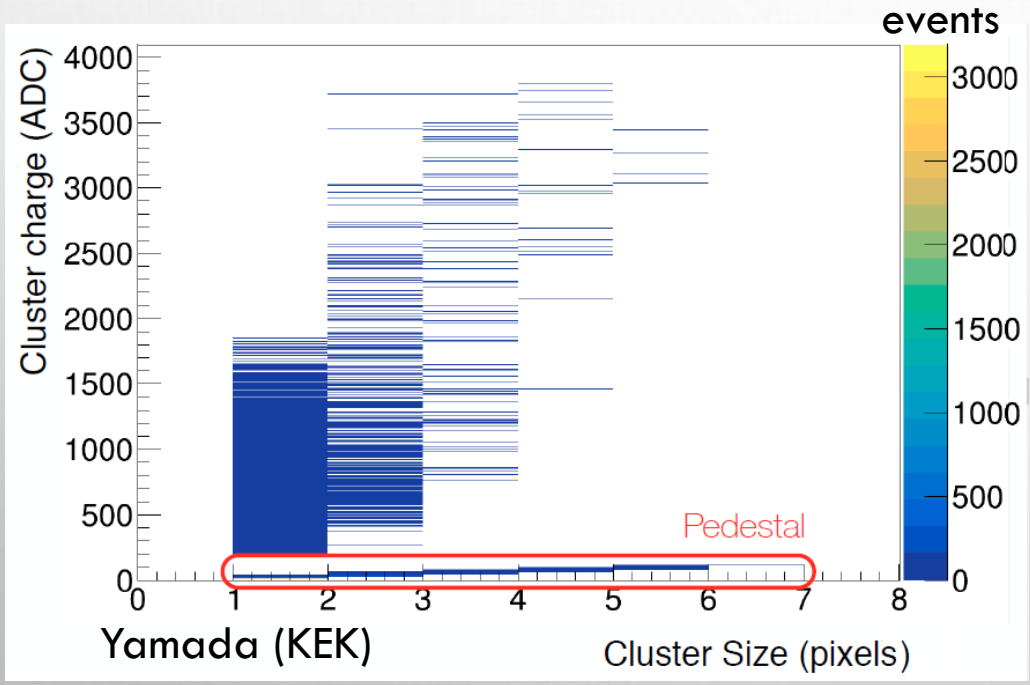
Full depletion expected ~30V for $9 \times 10^{12}/cm^3$ (0.5kΩcm) concentration (measured)

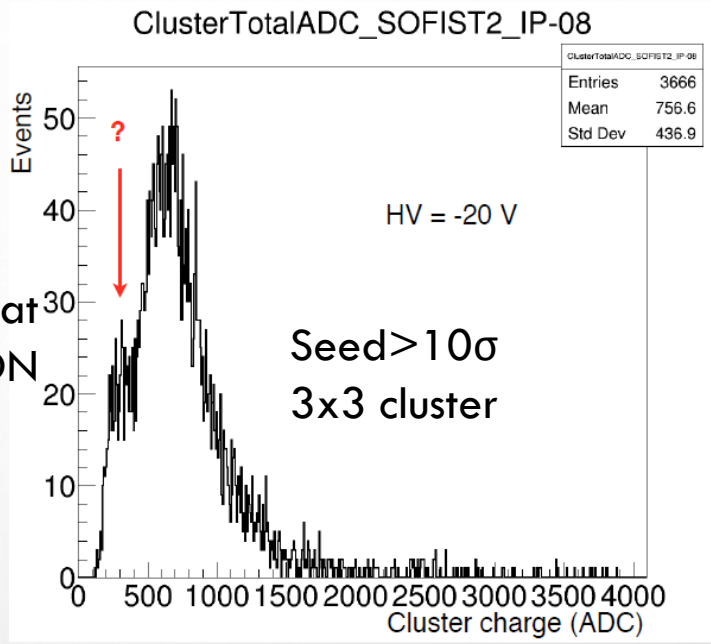
S>700 ADC (N~5 ADC) for 67um thickness

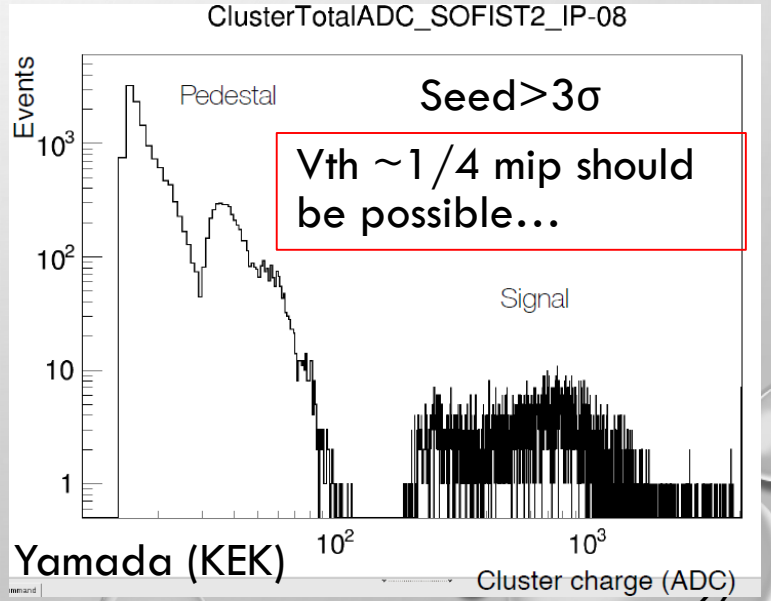
SOFIST-2 CLUSTER CHARGE

Mostly one-cluster events
Vth ~1/2 mip

peak~300ADC: X-talk at Comparator ON



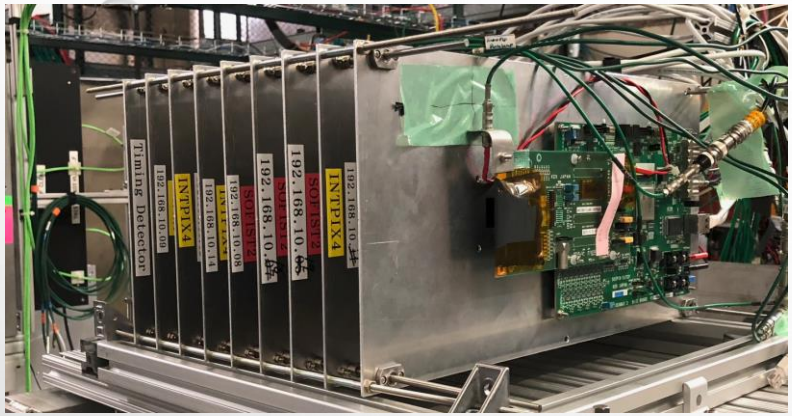




SOI Testbeam@FNAL (2018 Feb/Mar)

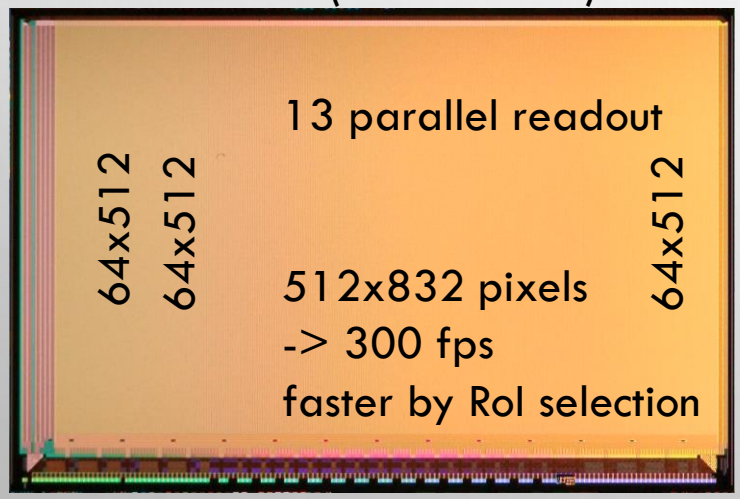
Tracker for SOFIST testbeam

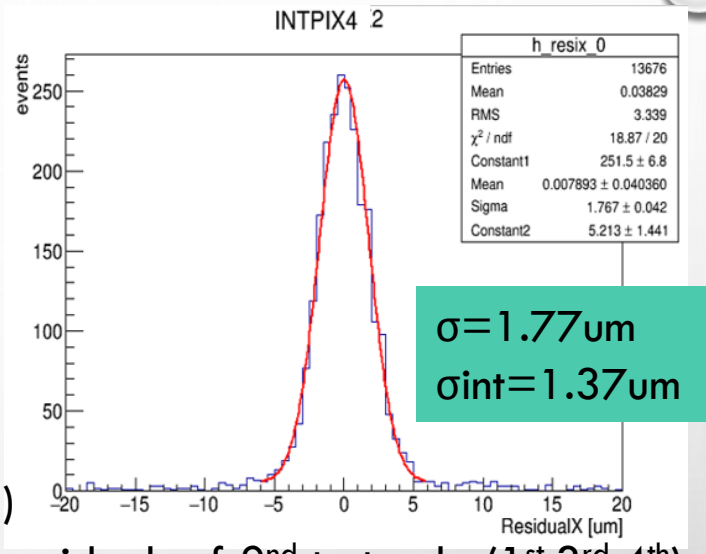
Using 4 plaes of large-area INTPIX4



Pixel size : 17x17um

Sensitive area (8.7x14.1mm)



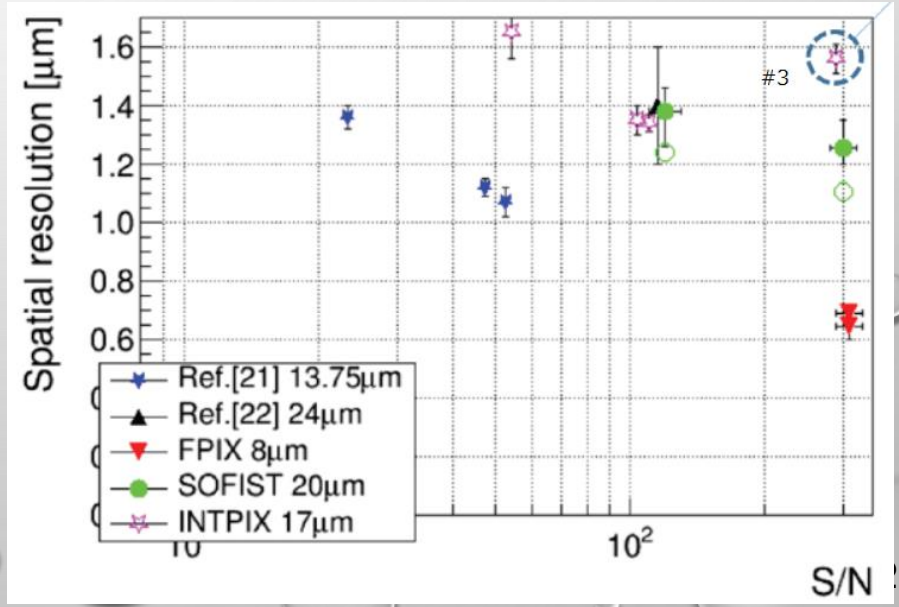


σ=1.77um

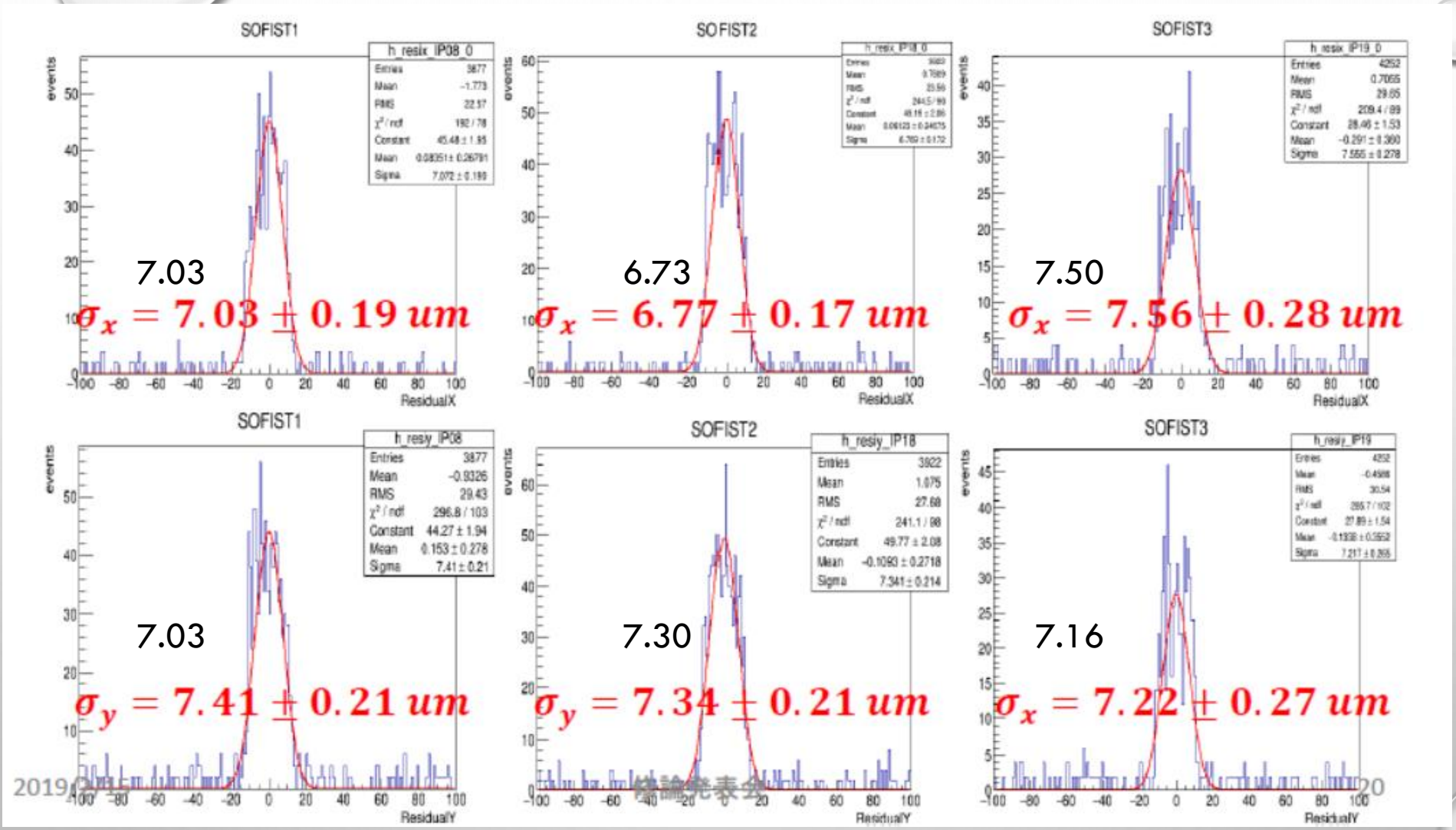
σint=1.37um

(山内, 修論)

Hit residuals of 2nd to tracks (1st,3rd,4th)



SOFIST2 SPATIAL RESOLUTION

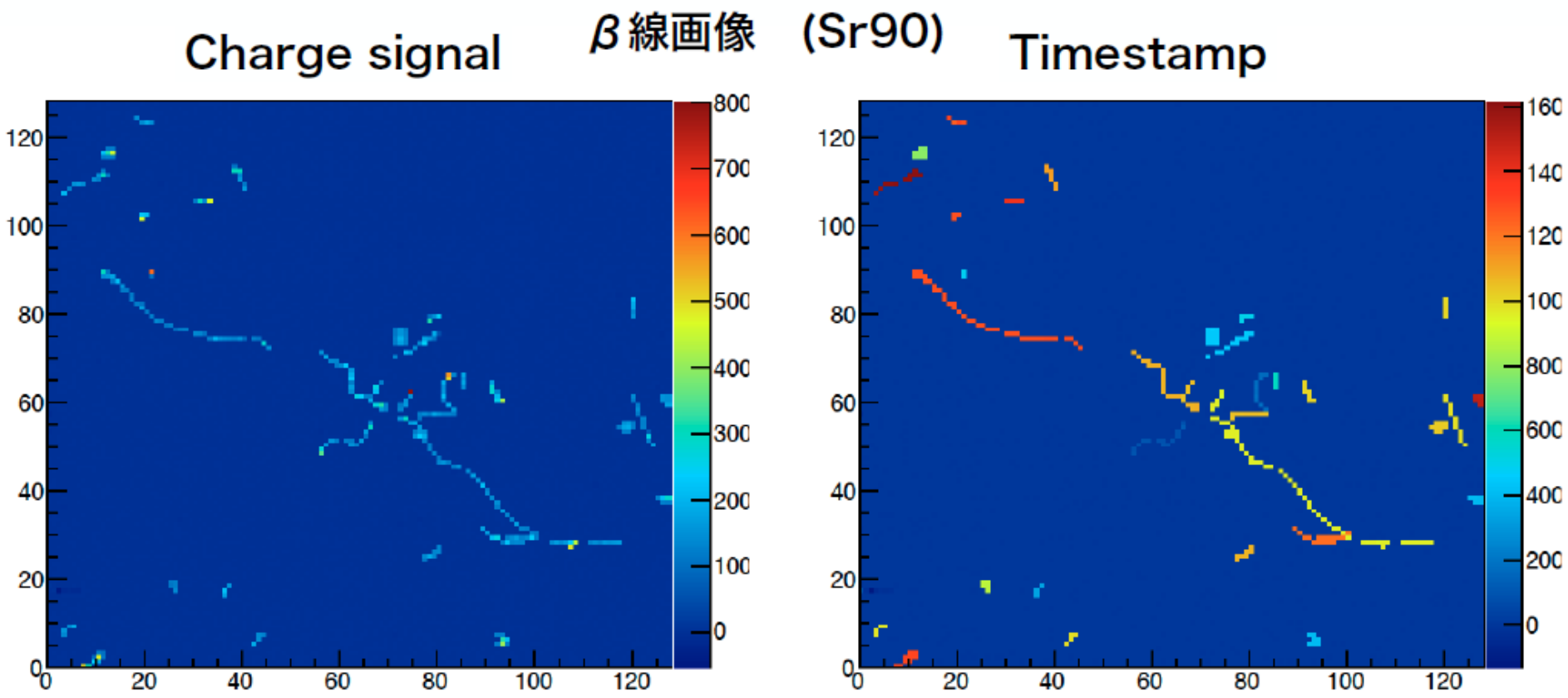


Due to a high Vth applied in the testbeam, hits are with ~single cluster
⇒25um/√12~7.2um expected

SOFIST-3 – QUICK TEST

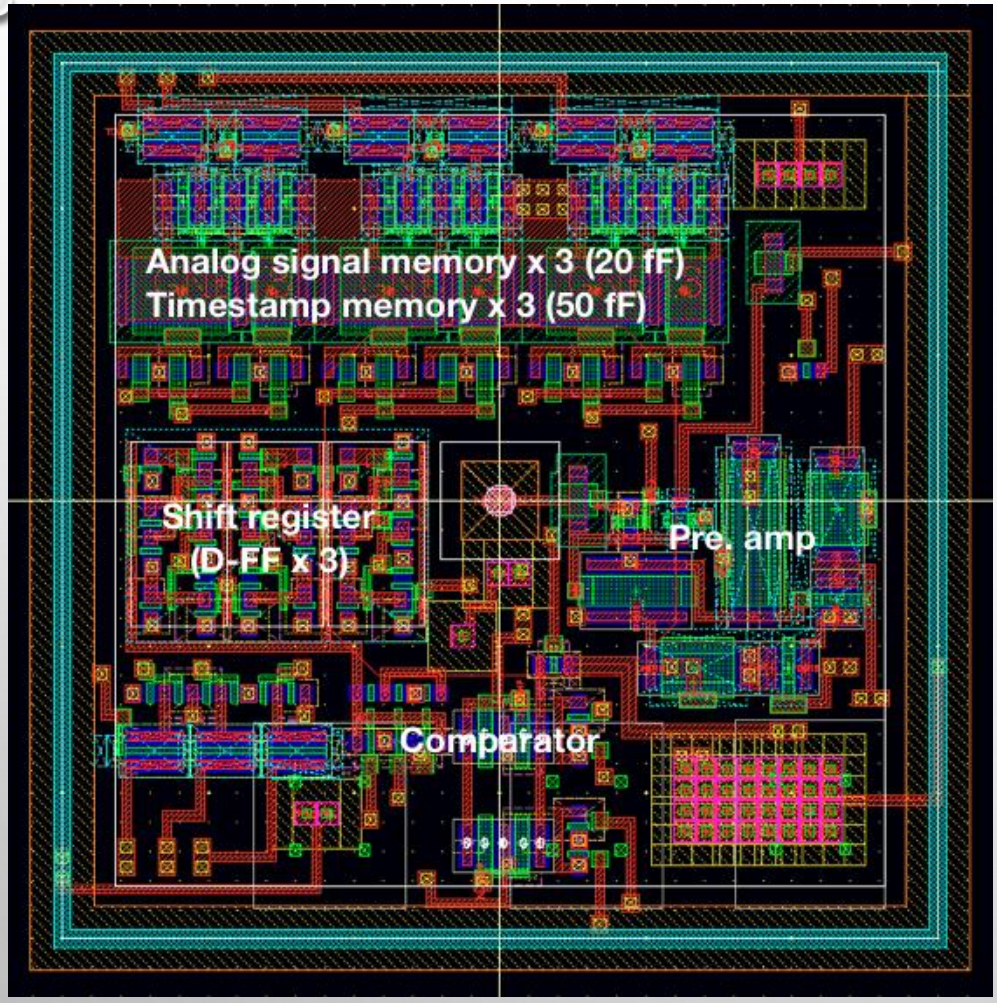
Both functions implemented on 30um pixels

Under testbeam @ FNAL



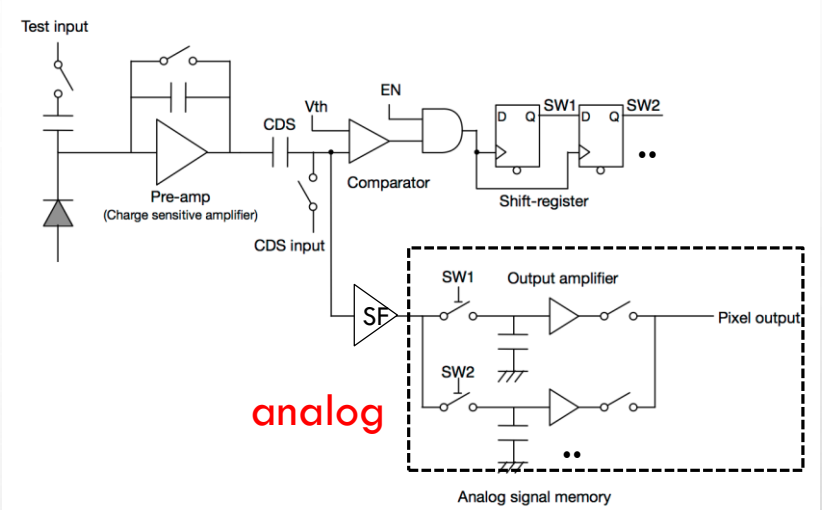
S. Ono(KEK)

SOFIST-3 – PIXEL LAYOUT

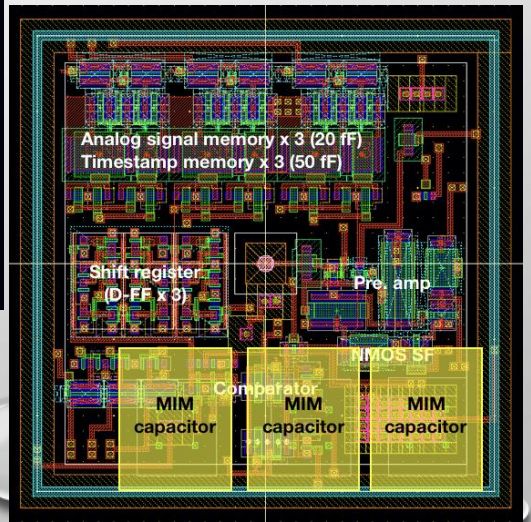


30um

Yamada (KEK)



X2 for
timestamp



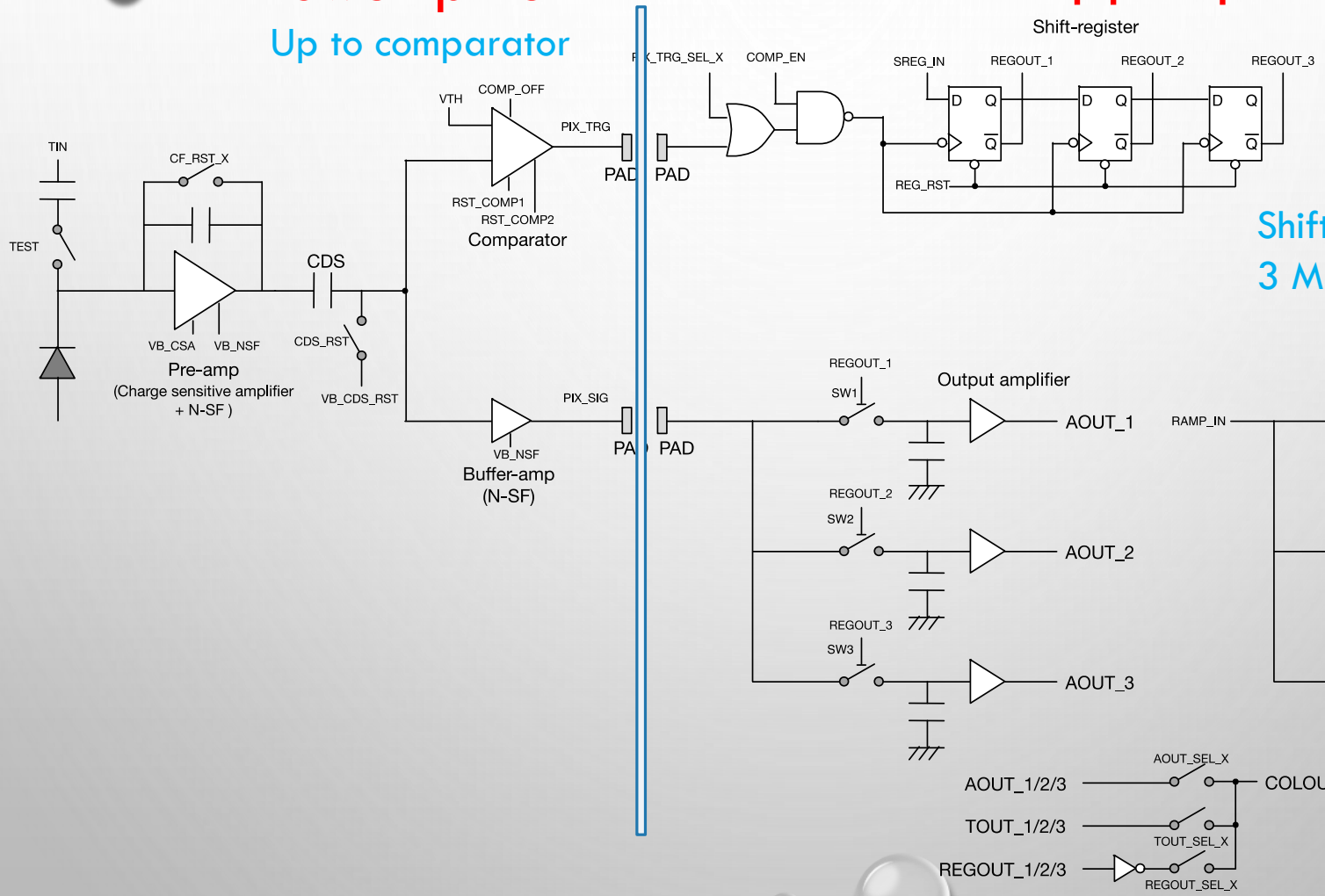
MIM(50fF, 1.5fF/um^2)
1 for CDS
2 for comparator

SOFIST VER.4

Lower pixel

Up to comparator

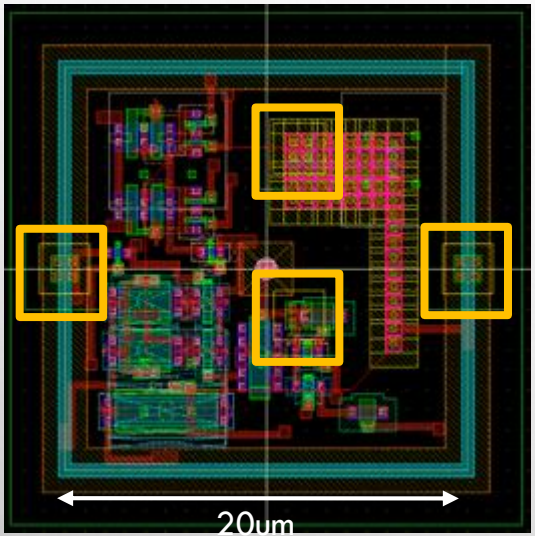
Upper pixel



Shift-registers
3 Memory cells each

SOFIST-4: PIXEL LAYOUT

Lower pixel
- Pre-amp
- Comparator

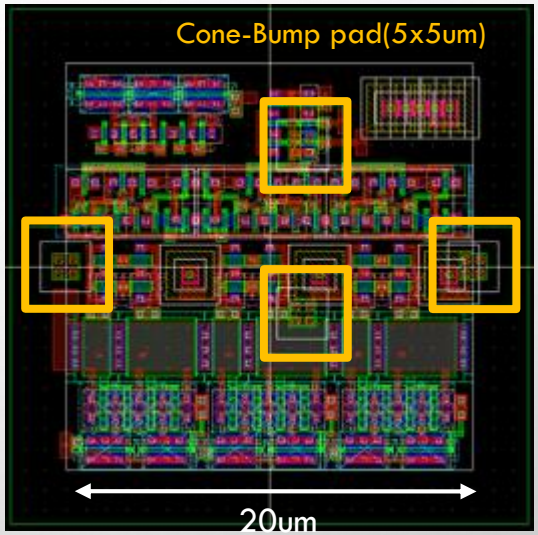


3 bumps/pixel

Au cone bump

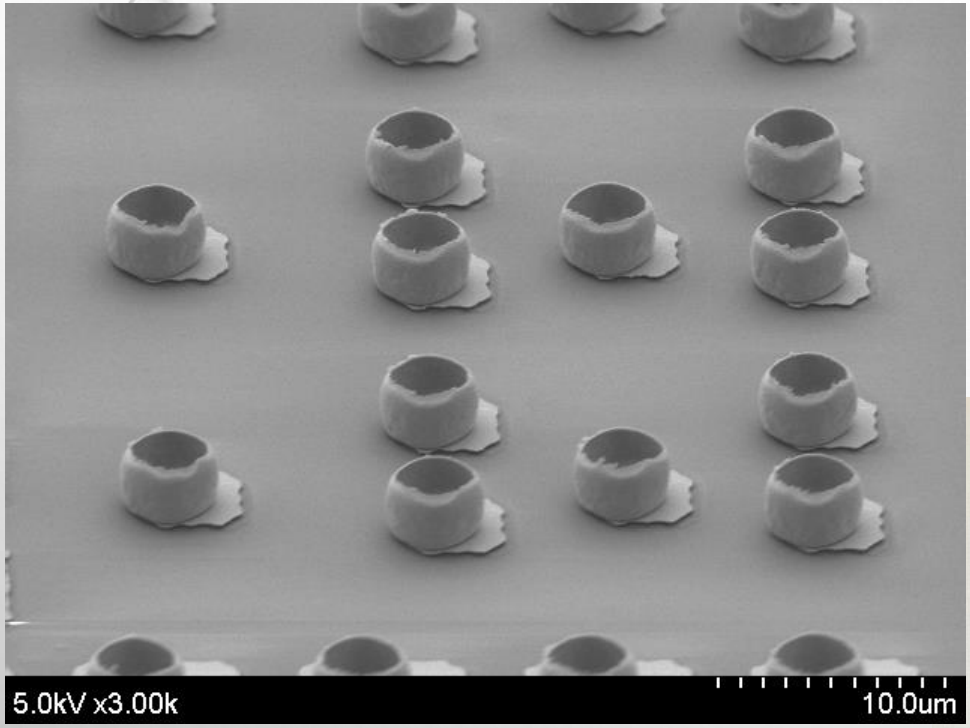
Reported LAST YEAR

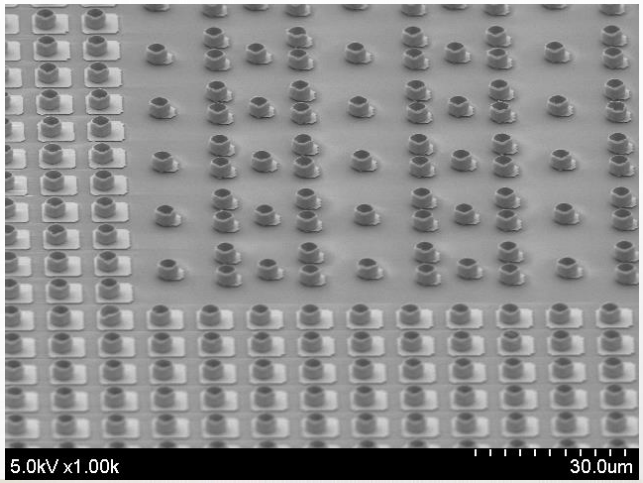
Upper pixel
- Shift-register
- Analog memory x3
- Timestamp x3



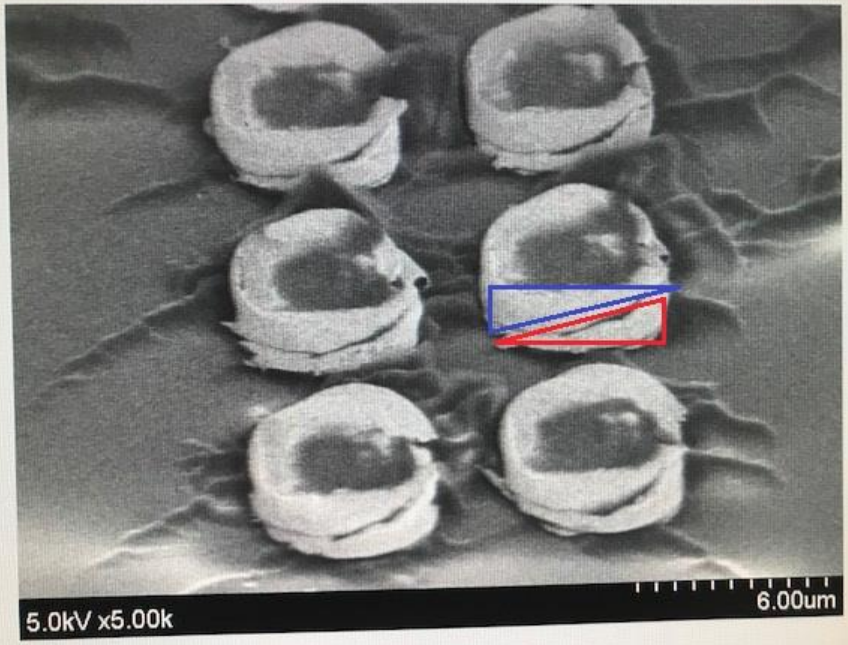
3D IS COMING (SOFIST-4)

Cylinder-type is more reliable





T-Micro slight mis-alignment to UBM ⇒corrected

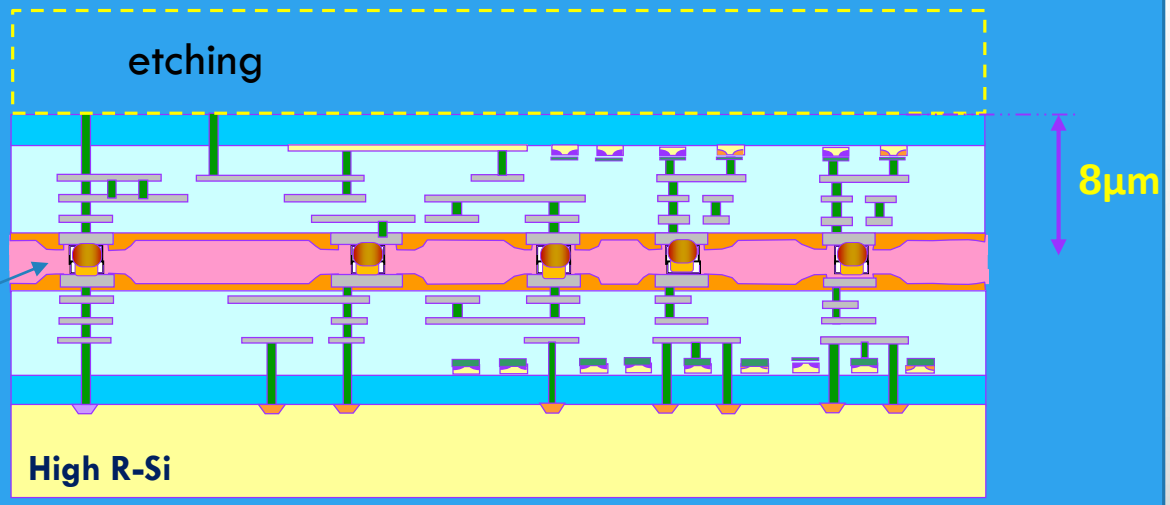


Upper&lower bumps are stacked well
(peel off one sensor layer)
Bonding<200degC

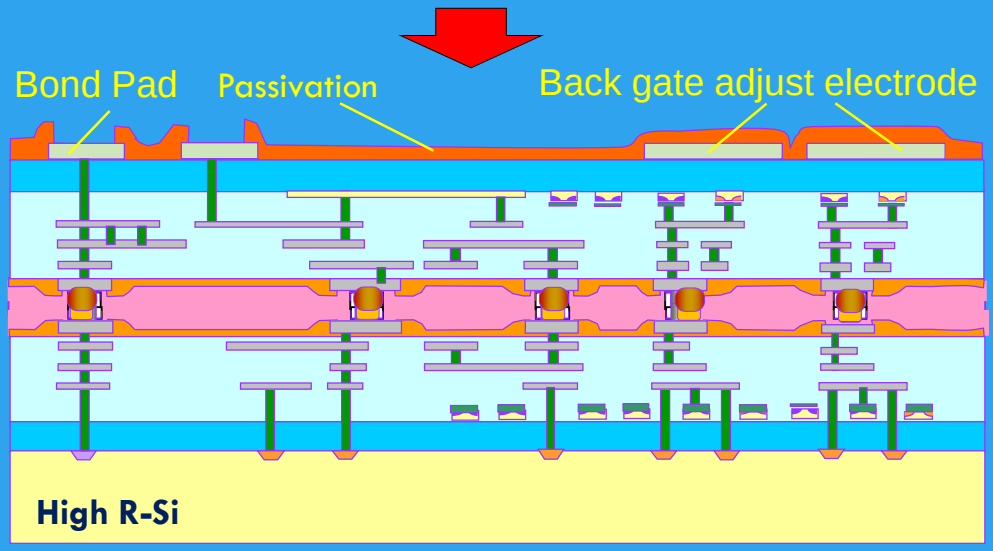
K. Hara, US-Japan Science Program, March 2019, FNAL

REMAINING PROCESSES (SOFIST-4)

(d) Bulk-Si removal



(e) Pad patterning and passivation



T-Micro

SUMMARY

- 5-year Grant-in-Aid (2013-2017) accelerated development/application of various SOI devices.

- SOFIST has been tested in FNAL beam

  SOFISTv1 <20um pixel size>

  spatial resolution:

  1.3 um(500um)-1.4 um (200um) with no η-correction applied

  SOFISTv2 <25um pixel size>

  time resolution: 1.89us (linear calibration)

  good S/N~120 for 67um thickness

  cluster size~1 (Vth was set slightly high)

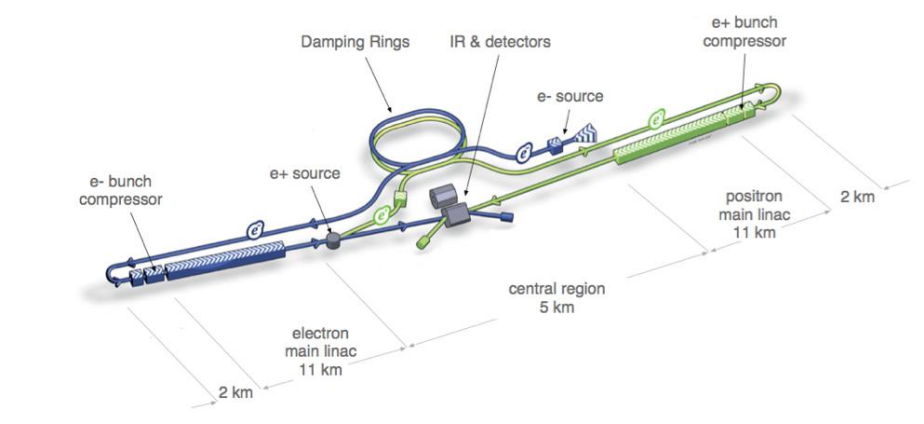
  - spatial resolution ~8um as expected from pixel si

- SOFISTv3 is beam tested
- SOFISTv4 fabrication is underway

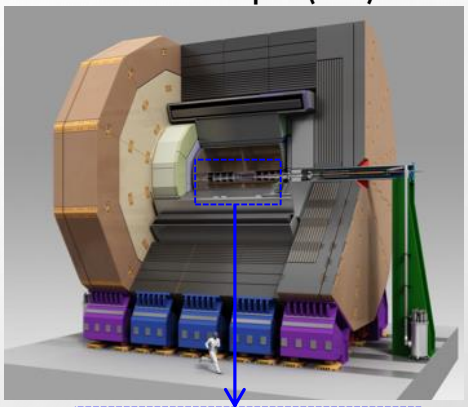
SPARES

INTERNATIONAL LINEAR COLLIDER

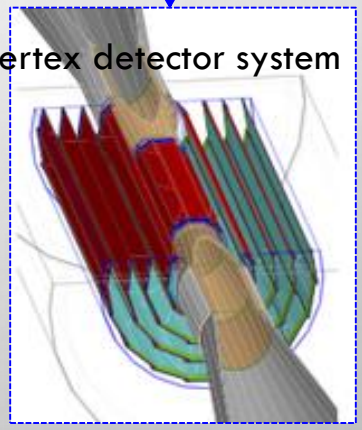
- ILC EXPERIMENT
  - E+E− LINEAR COLLIDER
  - CENTER OF MASS ENERGY: 250 - 500 GEV
  - PRECISE MEASUREMENT OF THE HIGGS BOSON



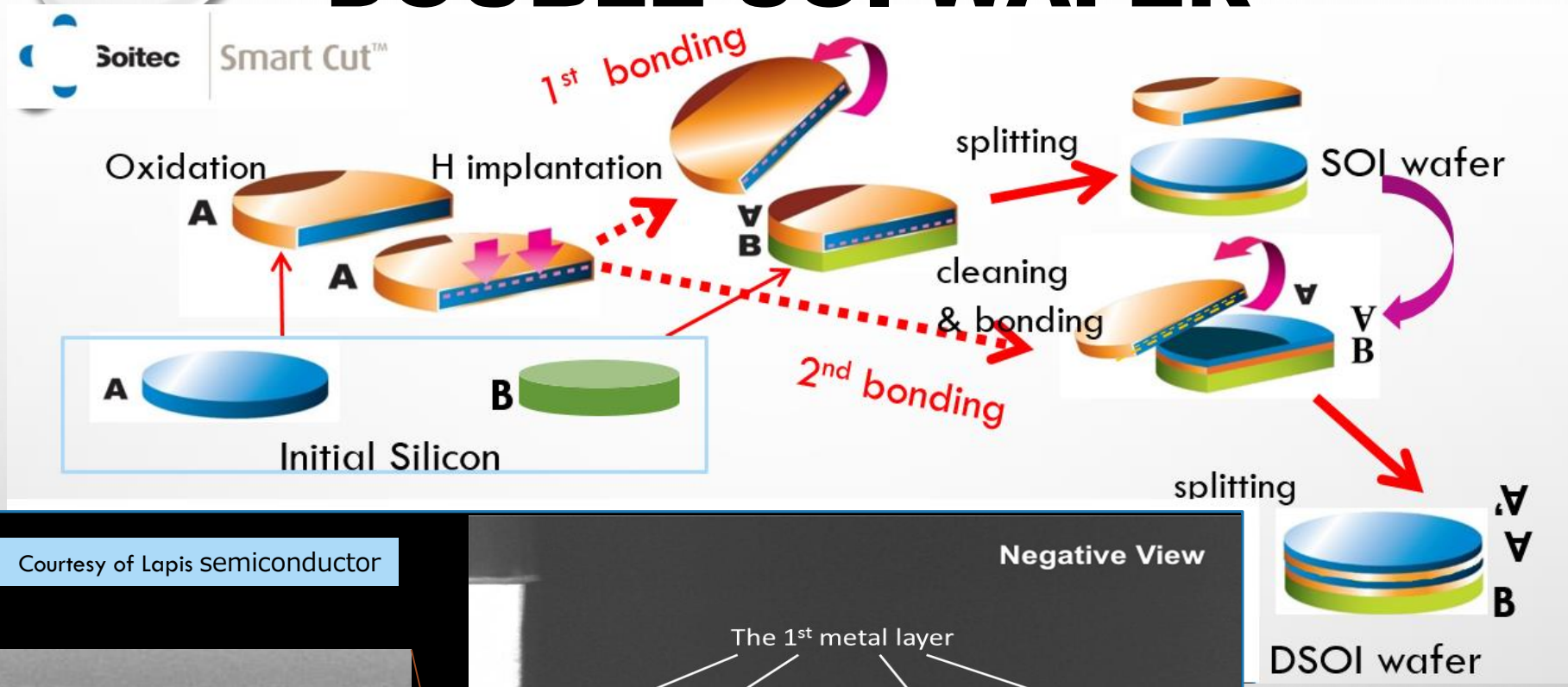
ILC detector concept (ILD)

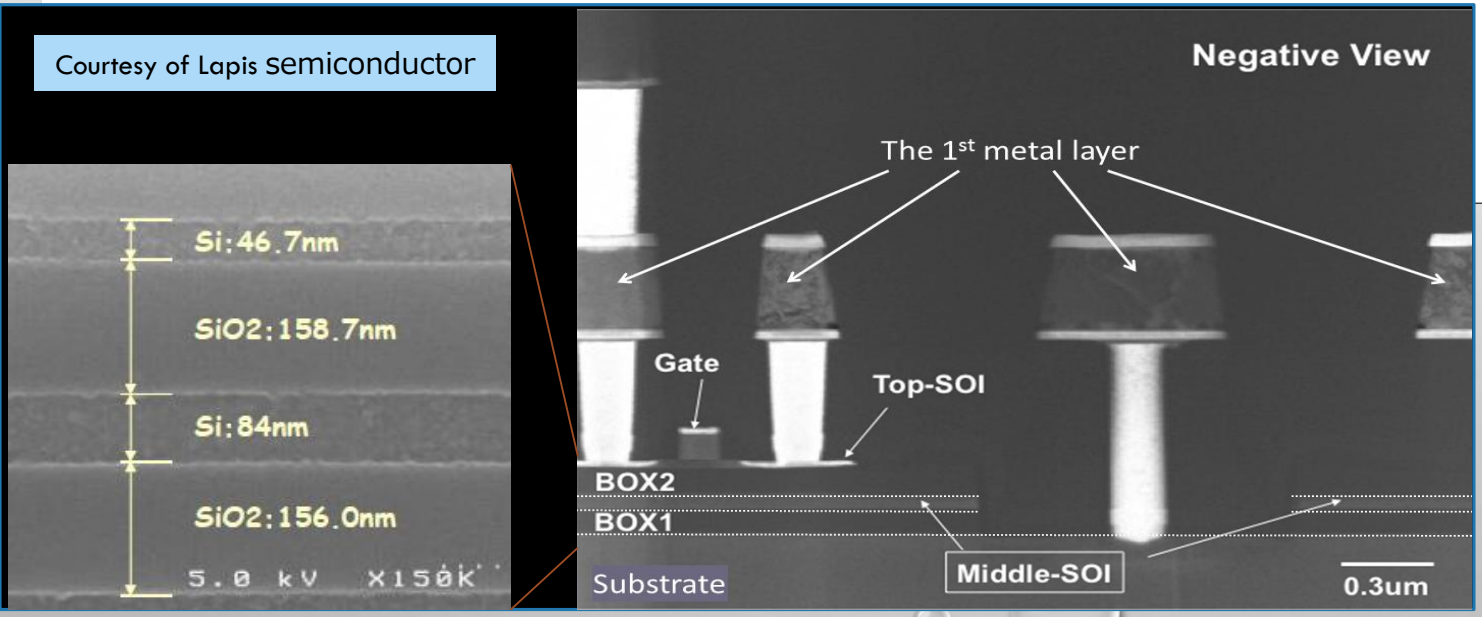


Vertex detector system



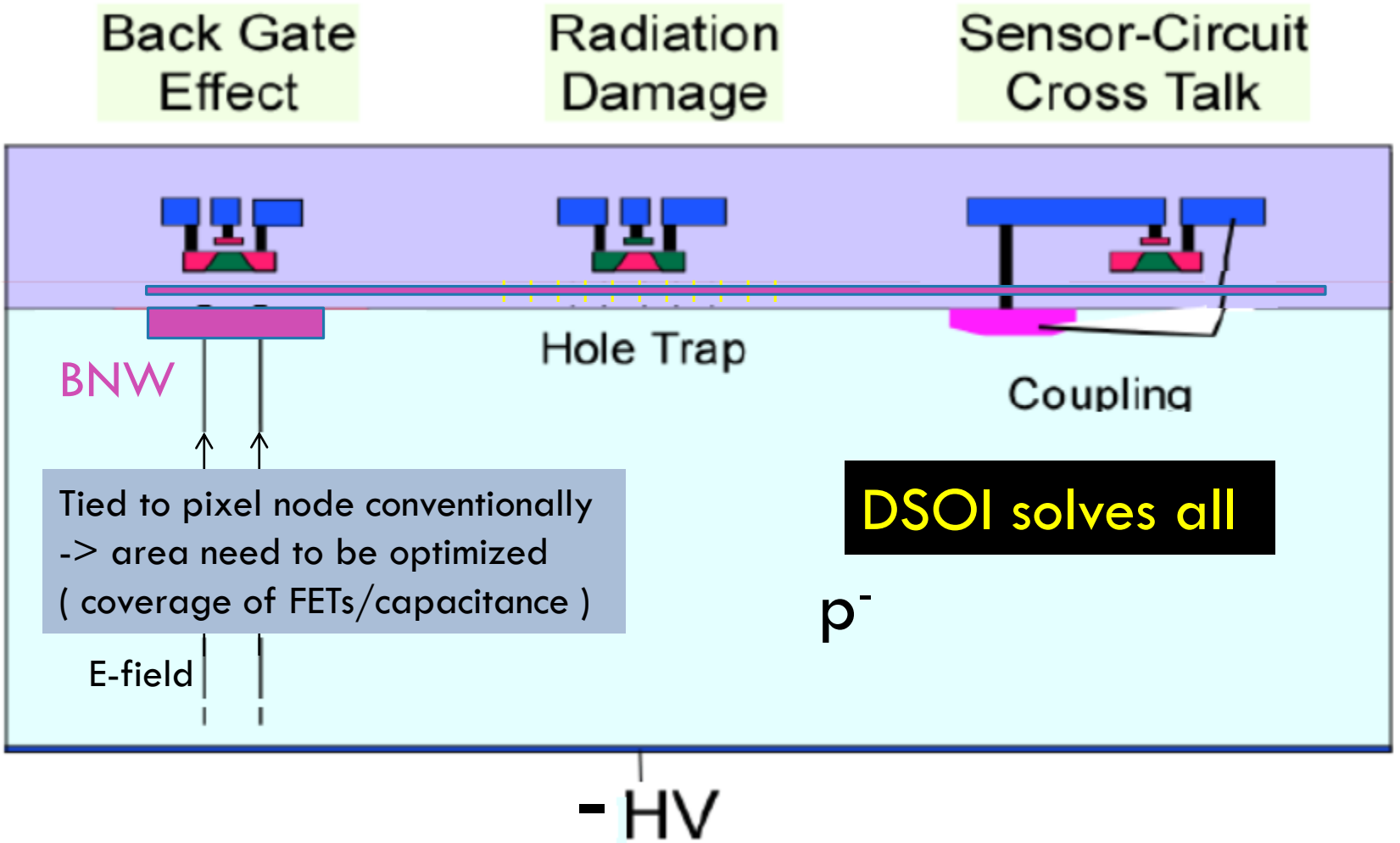
DOUBLE SOI WAFER





ISSUES TO OVERCOME

In application of SOI to pixel devices …..



WAFER TYPES

Lapis Semiconductor: 0.20um FD-SOI process

- Optimum wafer selectable (single p/n, various resisitivities):
- One type for double: getting better!

Layer	Single SOI	D-1 (SOITEC)	D-2 (Shinetsu)	D-3(Shinetsu) MX2166
SOI1	p-type 88 nm, <10 Ω•cm	p-type 88 nm, <10 Ω•cm	p-type 88 nm, <10 Ω •cm	p-type 88 nm, < 10 Ω •cm
BOX1	200 nm	145 nm	145 nm	145 nm
SOI2	-	p-type 88 nm, <10 Ω •cm	n-type 150 nm, <10 Ω •cm	n-type 150 nm, 3-5 Ω •cm
BOX2	-	145 nm	145 nm	145 nm
Substrate 725um	n-type/p-type CZ, FZ, Low-Ox CZ,,, 0.7~25 kΩ •cm	n-type CZ >700 Ω •cm	p-type Low Oxygen CZ >1.0 kΩ •cm	p-type FZ > 5.0 kΩ •cm

On-going MPW