Overview of CMS HCAL Barrel Phase 1 Upgrade

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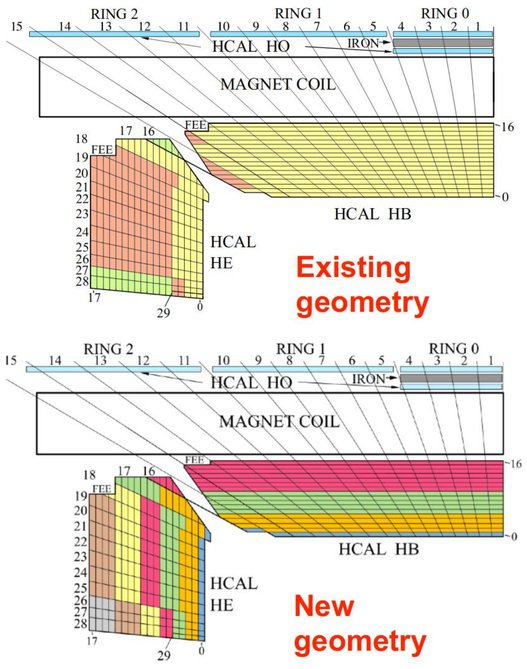
Design and Motivation



Long Shutdown 2 (LS2) will see the completion of the CMS Hadron Calorimeter (HCAL) Phase 1 Upgrade with the installation of the new HCAL Barrel (HB) front end electronics.

Upgraded Photodetectors

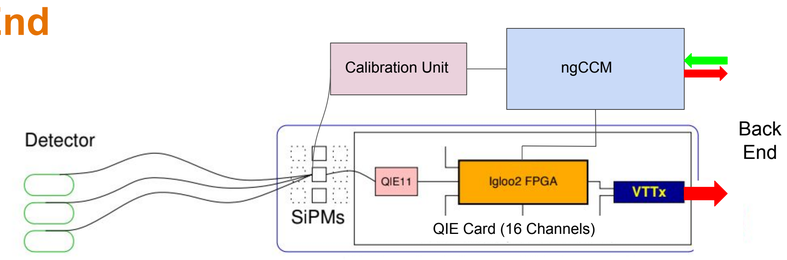
- Silicon Photomultipliers (SiPMs) replace HPDs (hybrid photodiodes)
- SiPMs eliminate the high amplitude noise and premature aging of the HPDs
- SiPMs have greater light sensitivity to compensate for scintillator radiation damage

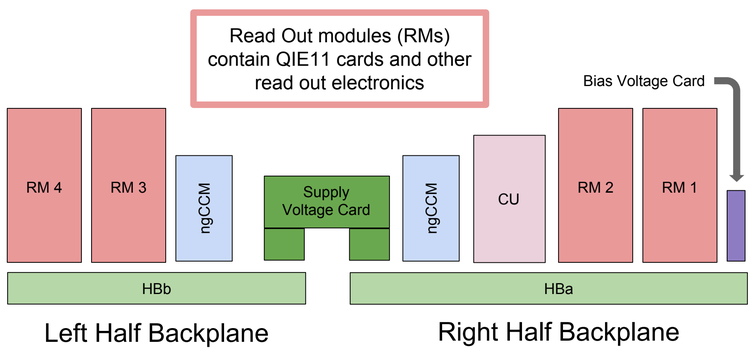
Increased Depth Segmentation

- Improves particle identification
- Improves pileup mitigation

The New Front End

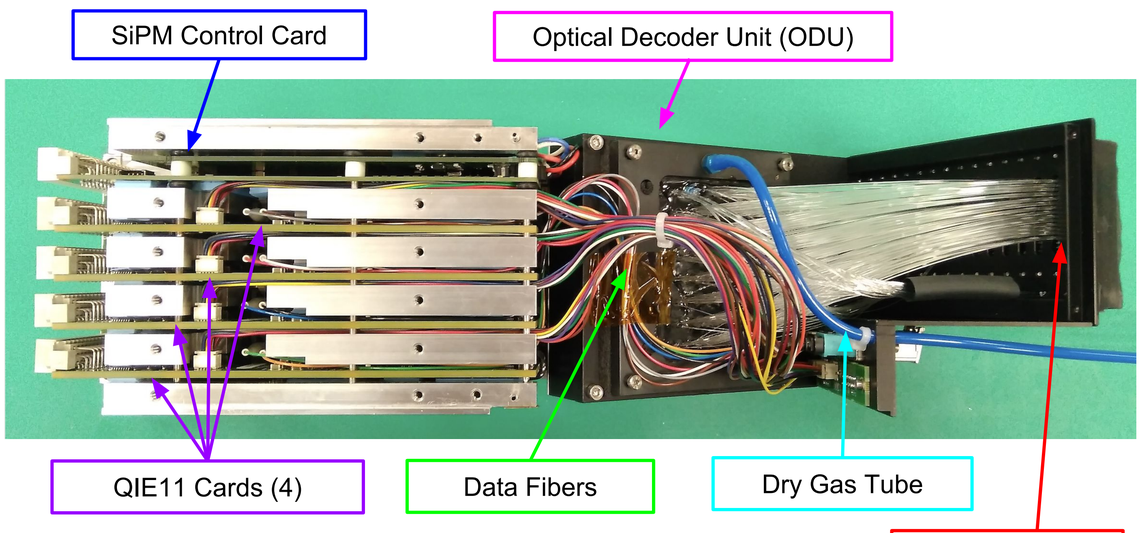
The new front end incorporates the first large scale use of SiPMs in a collider experiment, and each SiPM is independently biased and monitored. The SiPMs are followed by new 16-channel QIE11 Cards, providing the charge integration and ADC for the upgraded HCAL, with a new readout speed of 4.8 gbps. The control chain receives new SiPM control cards, Calibration Units (CUs), and Next Generation Clock Control Modules (ngCCMs). The ngCCMs have a bidirectional control link of 2.4 gbps. The control system upgrade increases the control granularity of the HCAL Barrel by a factor of two.





RM and CU Assembly

Read Out Modules (RMs) : 144 needed for detector



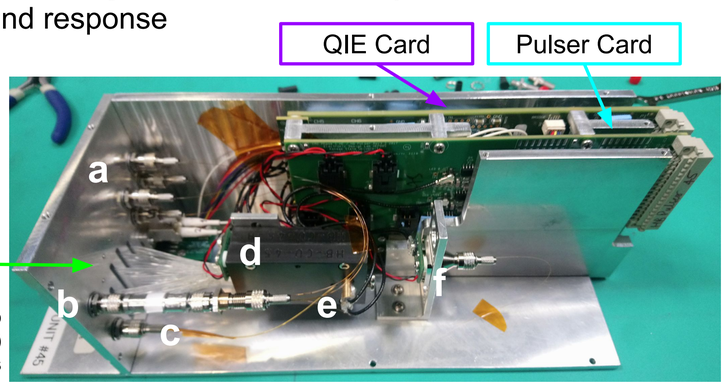
HCAL scintillator light is converted to digital signal within each RM. The **main components** of an RM are:

- Four QIE11 Cards →charge integration and analog to digital conversion (ADC)
  - 576 cards for detector install
- One SiPM Control Card
- One Optical Decoder Unit (ODU) →mapping for SiPMs to megatiles
- One SiPM Mounting Board + Peltier →holds 8 SiPM arrays (9216 channels total)

Calibration Units : 36 needed for detector

Provides known laser pulses to the megatiles and SiPM arrays within each Read Out Box (RBX) for calibration and response measurement. There are two distinct assembly and QC tasks:

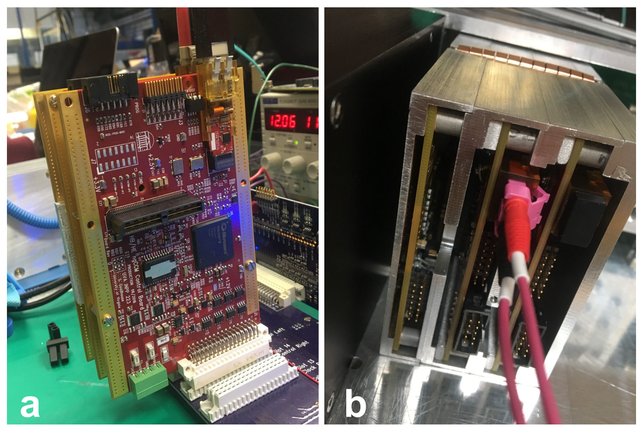
- electronics assembly
- optical assembly



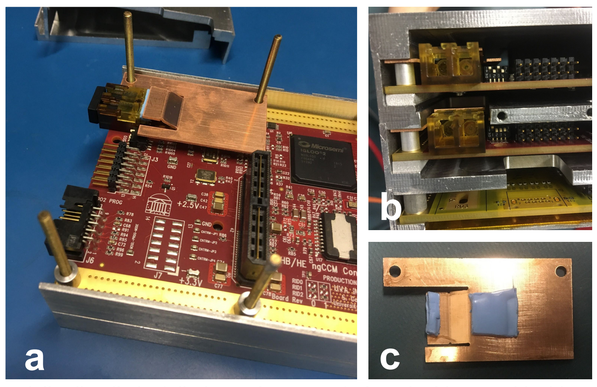
a.) Laser to megatile outputs. b.) Laser to megatile input. c.) Laser to SIPM input. d.) Optical mixer/splitter. e.) LEDs. f.) PIN Diodes

ngCCM Assembly

The Next Generation Clock Control Module (ngCCM) provides controls for each RBX. The HB ngCCM has a three card design with one clock card and two fully redundant control cards. Each RBX has two ngCCMs, each controlling two RMs. The ngCCM in the right half-backplane also controls the CU. A cooling fin was added to the housing design mid-assembly for prolonged VTRx lifetime.



a.) HB ngCCM without housing on testing stand. b.) HB ngCCM in housing being installed into an RBX in burn-in.

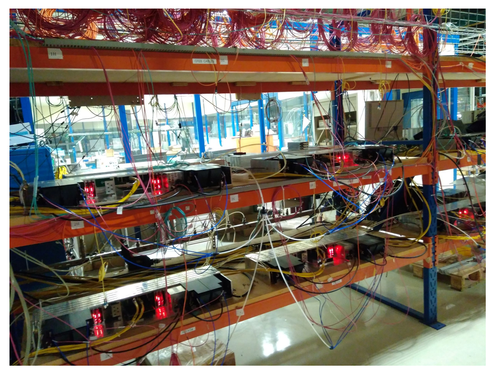


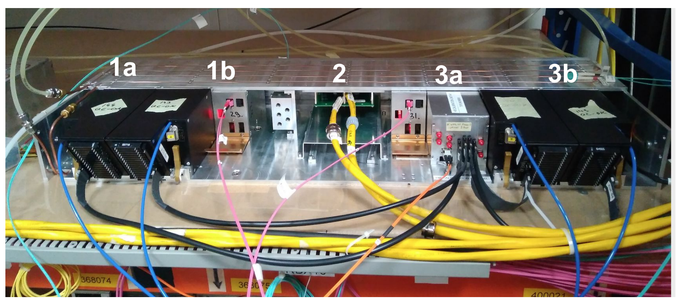
a.) Cooling fin installed on primary control card mid-assembly. b) Top view of fins installed in complete assembly. c) Fin with thermal pad placement.

- 72 ngCCMs needed for installation
  - 72 clock cards
  - 144 control cards
- Quality control tests include:
  - Link health
  - Board-to-board connections
  - Power consumption
  - I2C protocol
  - Input/output

Burn-in

"Burn-in" is a pre-installation phase that mimics detector running. Electronics are installed in production RBX mechanics and operated for two weeks. Burn-in takes system wide scans of basic parameters of the front end to ensure uniformity and performance. This includes QIE chip pedestal scans, SiPM gain measurements, light response, and climate monitoring.

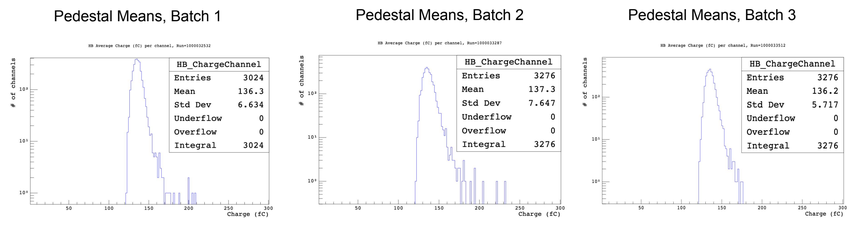




Above: Image of burn-in RBX stands in b904.
Left: Detail burn-in RBX
1: Left Half Backplane
  a: RM4 and RM3 (left to right)
  b: ngCCM
2: Low Voltage Supply
3: Right Half Backplane
  a: ngCCM
  b: CU
  c: RM2 and RM1 (left to right)

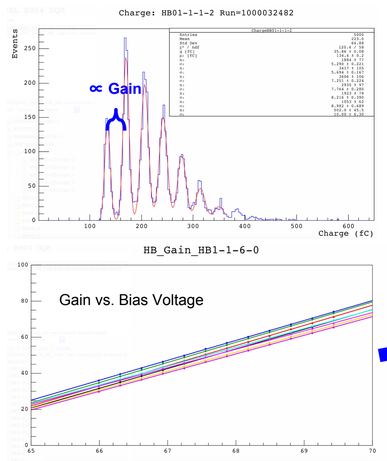
Pedestal Runs

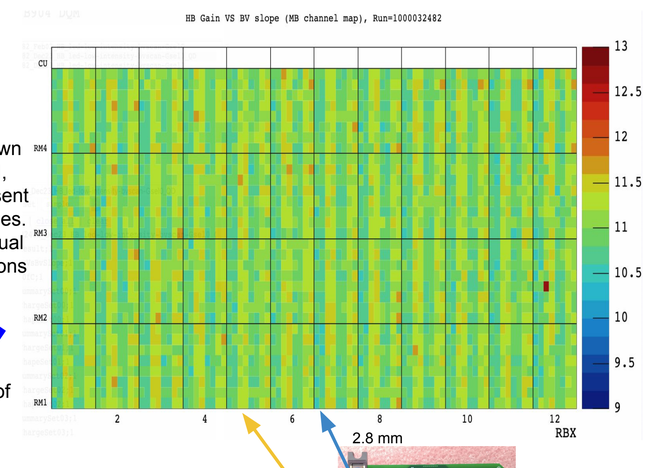
Pedestal runs check the uniformity of the QIE chip pedestal (noise levels) and pedestal setting functionality.



SiPM Gain Characterization

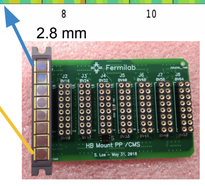
SiPM gain is measured during low intensity LED runs by finding the difference between multi-photoelectron peaks.





Results shown for batch 1, features present across batches. Uses individual QIE calibrations

Slopes across all of burn-in



Different bands of gain vs. SiPM bias voltage slope correspond with different sized SiPMs on the arrays.

SiPM Temperature Monitoring

SiPMs will be operated around 0 °C, with peltier cooling maintaining SiPM temperatures to 0.05°C RMS.