Construction and characterization of the Upgraded Inner Tracking System for the ALICE experiment

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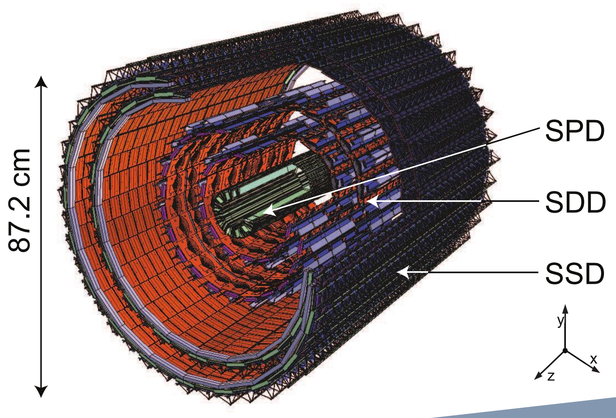
Present ITS



6 layers of silicon detectors
- Silicon Pixel Detectors (**SPD**)
- Silicon Drift Detectors (**SDD**)
- Silicon Strip Detectors (**SSD**)

Geometry
- Layer radii: 3.9 ÷ 43 cm
- Active area: ~6.5 m^2
- Acceptance: $|\eta| < 0.9$

Limits
- Material budget of 1.1% X_0 per layer
- Max readout rate of 1 kHz (SDD)
- Spatial resolution: ~120 μm at p_T = 500 MeV/c

Upgraded ITS 2019 - 2020

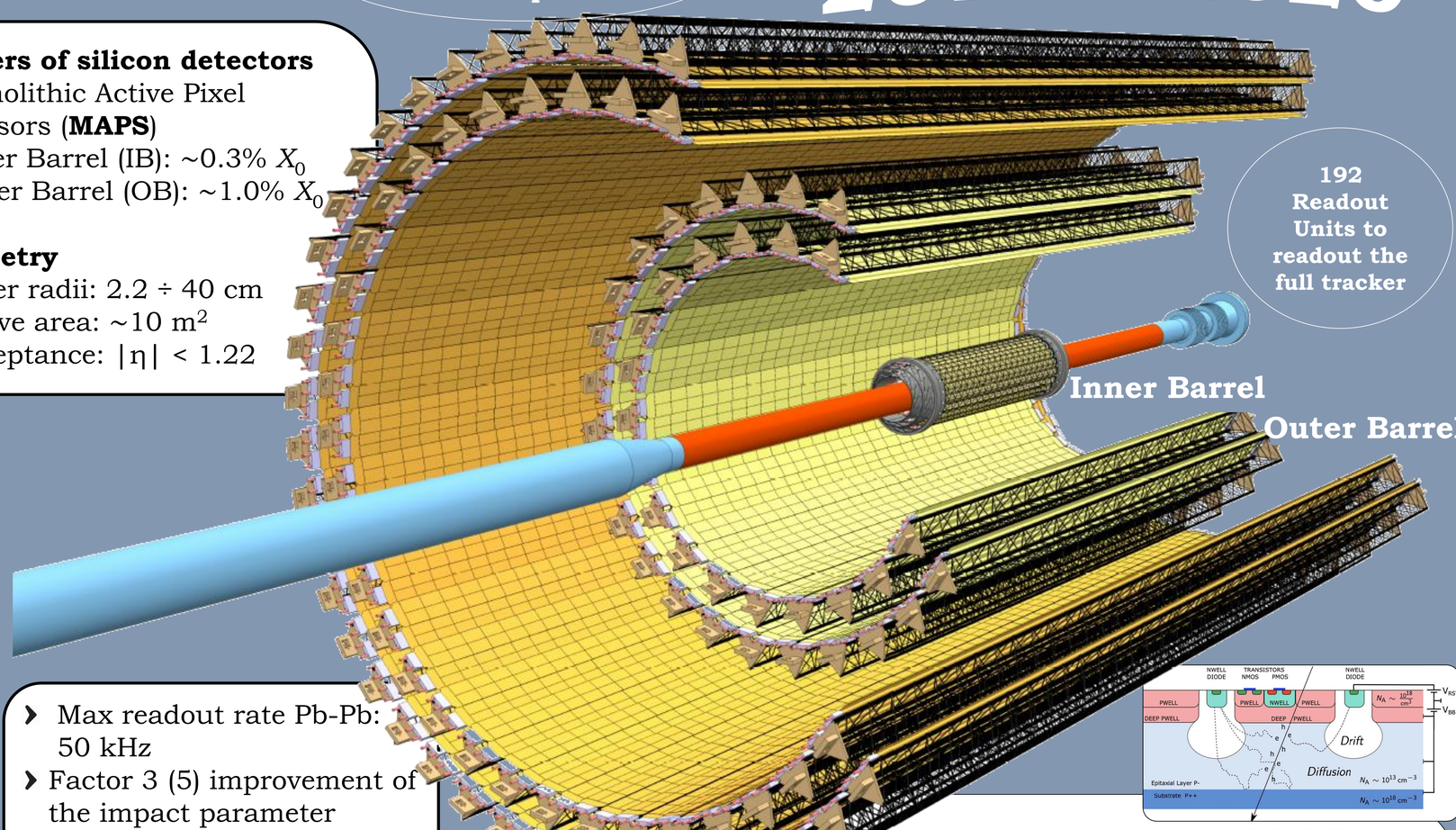
Commissioning starts in April 2020

- Target **integrated luminosity** in Pb-Pb at $\sqrt{s_{NN}}$ = 5.5 TeV: **10 nb^{-1}**
- **Physics goal**:
  - Heavy flavour and quarkonia at very low p_T
    - ☺ *Thermalization and recombination*
  - Vector mesons and low-mass di-leptons
    - ☺ *Chiral symmetry restoration, virtual thermal photons*
  - Light nuclei and hyper-nuclei
    - ☺ *Nucleosynthesis, exotics*

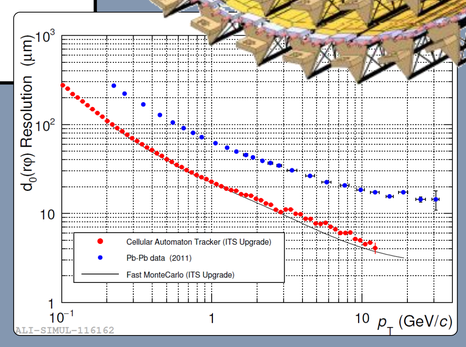
7 layers of silicon detectors
- Monolithic Active Pixel Sensors (**MAPS**)
- Inner Barrel (IB): ~0.3% X_0
- Outer Barrel (OB): ~1.0% X_0

Geometry
- Layer radii: 2.2 ÷ 40 cm
- Active area: ~10 m^2
- Acceptance: $|\eta| < 1.22$

192 Readout Units to readout the full tracker



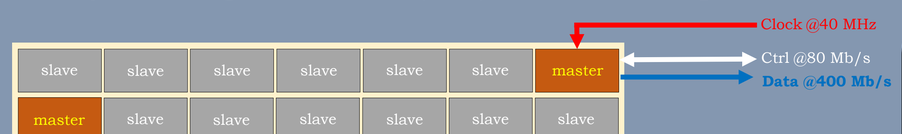
- Max readout rate Pb-Pb: 50 kHz
- Factor 3 (5) improvement of the impact parameter resolution at p_T = 500 MeV/c along z ($r\varphi$)

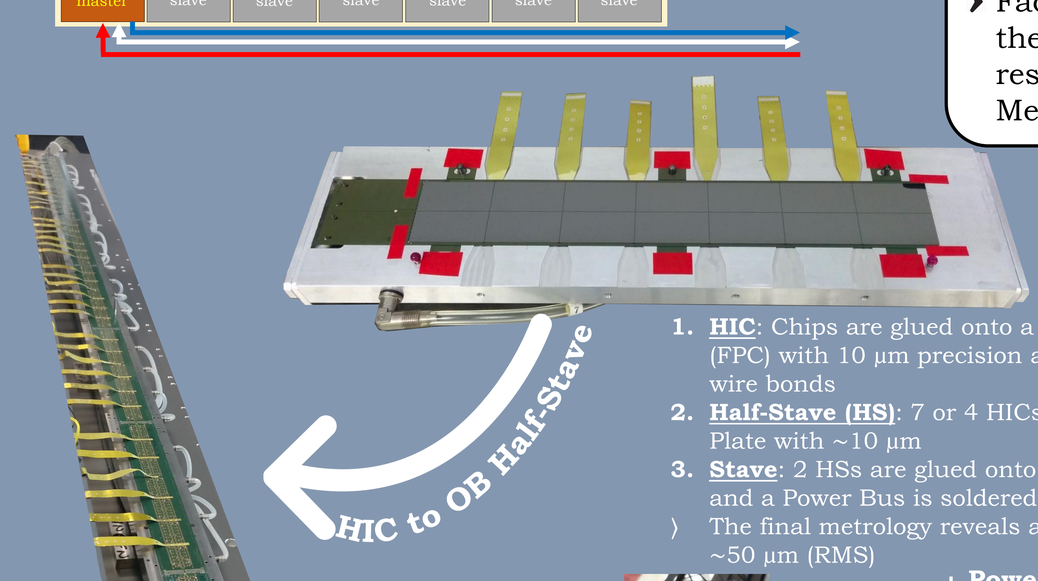


ALPIDE chip

- High resistivity p-type epitaxial layer: 1 ÷ 6 kΩcm
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel → Small capacitance (~fF)
- Deep PWELL shields NWELL of PMOS transistor
- Fast data driven encoder for pixel matrix readout: ~2 μs integration time
- Low power consumption: <40 mW/cm^2
- Sufficient operational margin even after 10× lifetime NIEL dose

OB Hybrid Integrated Circuit (HIC): 14 ALPIDE chips

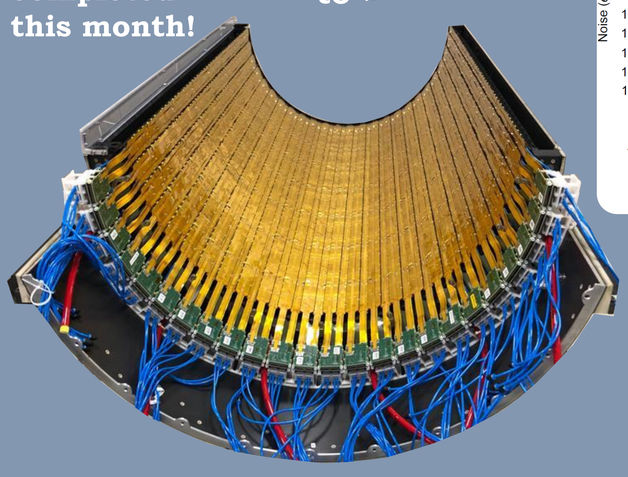


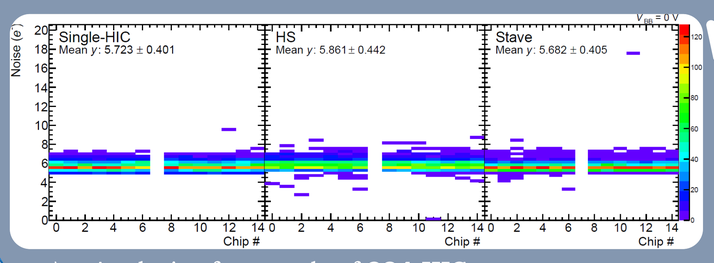


1. **HIC**: Chips are glued onto a Flexible Printed Circuit (FPC) with 10 μm precision and connected through wire bonds
2. **Half-Stave (HS)**: 7 or 4 HICs are glued onto a Cold Plate with ~10 μm
3. **Stave**: 2 HSs are glued onto a carbon Space-Frame and a Power Bus is soldered

- The final metrology reveals an alignment precision of ~50 μm (RMS)

Half-Layer 4 and 6 completed this month!

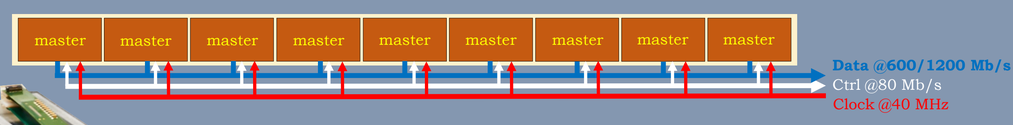


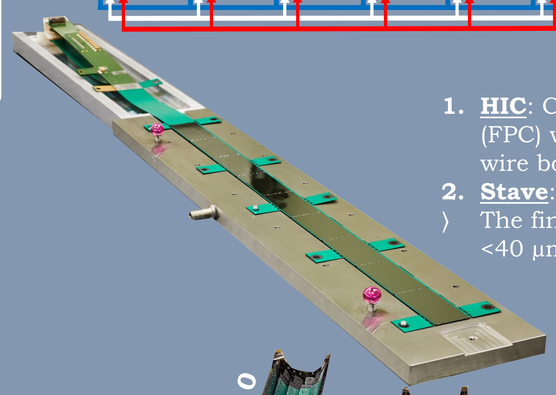


- Analysis of a sample of **284 HICs**
- The **noise** is stable around **6 e^-** from the single-HIC setup to the final Stave

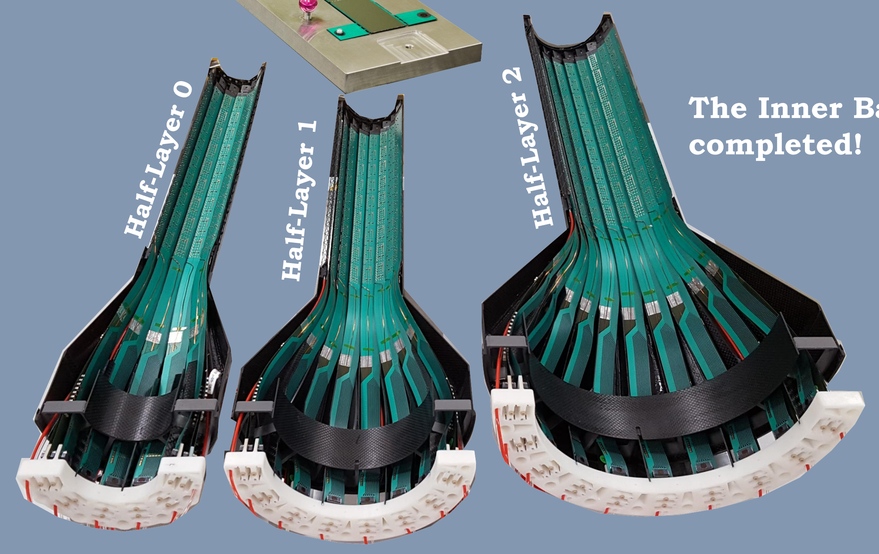
Inner Barrel

IB Hybrid Integrated Circuit (HIC): 9 ALPIDE chips





1. **HIC**: Chips are glued onto a Flexible Printed Circuit (FPC) with 10 μm precision and connected through wire bonds
2. **Stave**: 1 HIC is glued onto a carbon Space-Frame
- The final metrology reveals an alignment precision <40 μm



The Inner Barrel is completed!

Outer Barrel

References
- *J. Phys. G* 41 (2014) 087002
- *J. Phys. G* 41 (2014) 087001