ATLAS Level-1 Topological Processor

Performance during Run-2

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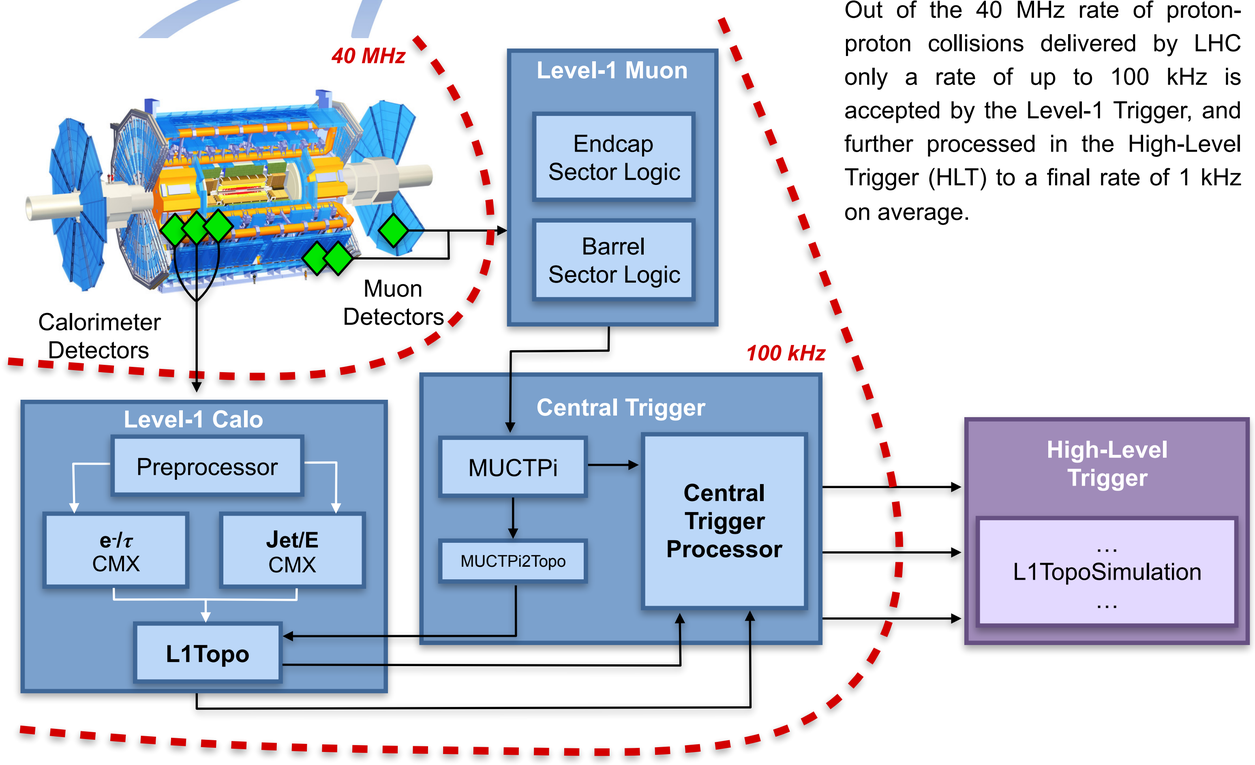
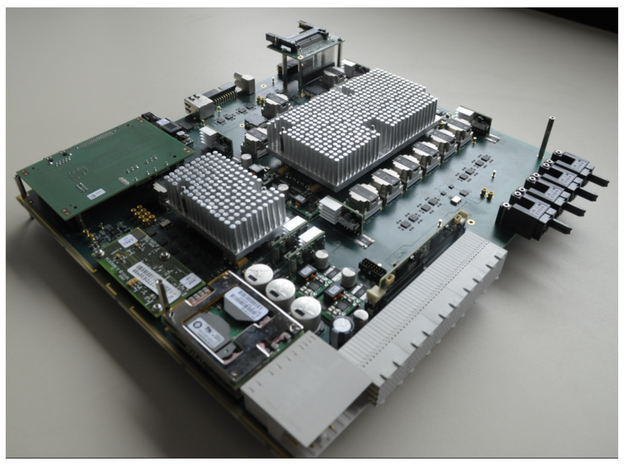
ATLAS Trigger System



Out of the 40 MHz rate of proton-proton collisions delivered by LHC only a rate of up to 100 kHz is accepted by the Level-1 Trigger, and further processed in the High-Level Trigger (HLT) to a final rate of 1 kHz on average.

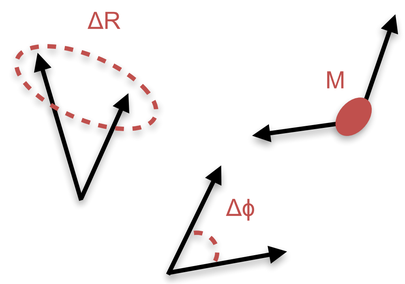
The Level-1 Topological Trigger receives information from both Level-1 Calorimeter and Level-1 Muon Trigger systems and provides decisions based on topological algorithms. A bitwise simulation of these algorithms runs within the High-Level Trigger for each Level-1 accepted event.

Run-2 L1Topo Hardware



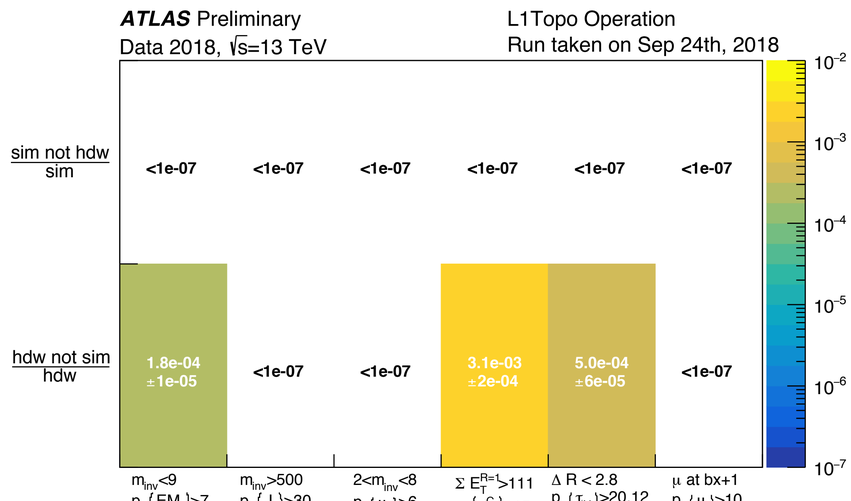
- During Run-2, two identical boards were commissioned and used. In each board:
  - 2 Virtex 7 FPGAs to process algorithms
  - 1 Virtex 7 FPGA for communication and readout
- ~ 1Tb/s input bandwidth per board
- 128 trigger decision bits available
  - **113 were used in 2018**

Functionalities



- Angular selections:
  - Δϕ, ΔR, Δη, angular window, objects disambiguation
- Mass selections:
  - Invariant and transverse mass
- Flexibility of using central and/or forward jets
- Combination of calorimeter and muon detectors information
- Access to trigger objects from different bunch crossings

Simulation Validation Plots

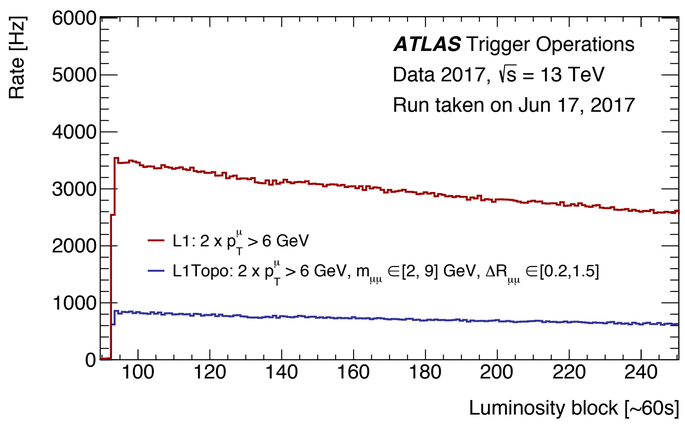


- The simulation running in the HLT allows to validate the hardware decisions
- Rates of decision mismatches between hardware and simulation are displayed online for each algorithm and stored
- The plot shows the rate of hardware false negatives (first row) and hardware false positives (second row) for different topological algorithms

All the algorithms used in physics analyses show a hardware to simulation decisions agreement better than 99%

Performance

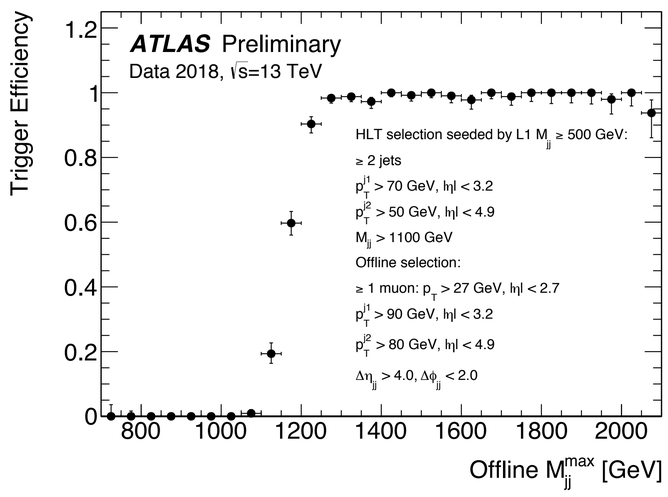
The event rate reduction achieved by the Level-1 Topological Trigger has been essential for many physics analyses. It has also been used for commissioning systems to be used in Run-3, as part of the Fast Tracker (FTK) system.



- This plot shows the trigger rate versus time when the L1Muon (red) or the L1Topo trigger including invariant mass and di-muon distance requirements (blue) are used. **A rate reduction of up to a factor of 4 is achieved with L1Topo**
- L1Topo proved very useful for B-physics analyses targeting final states with very low transverse momentum (p_T) leptons

L1Topo played also an important role for VBF analyses

- The possibility of placing a cut in the invariant mass of jets reduces the multi-jet trigger rate while enhancing the signal over background
- This plot shows the efficiency of the di-jet HLT trigger seeded by the L1Topo invariant mass trigger versus the offline di-jet invariant mass
- The invariant mass L1Topo trigger is used in analyses such as Higgs to di-τ or VBF Higgsino production



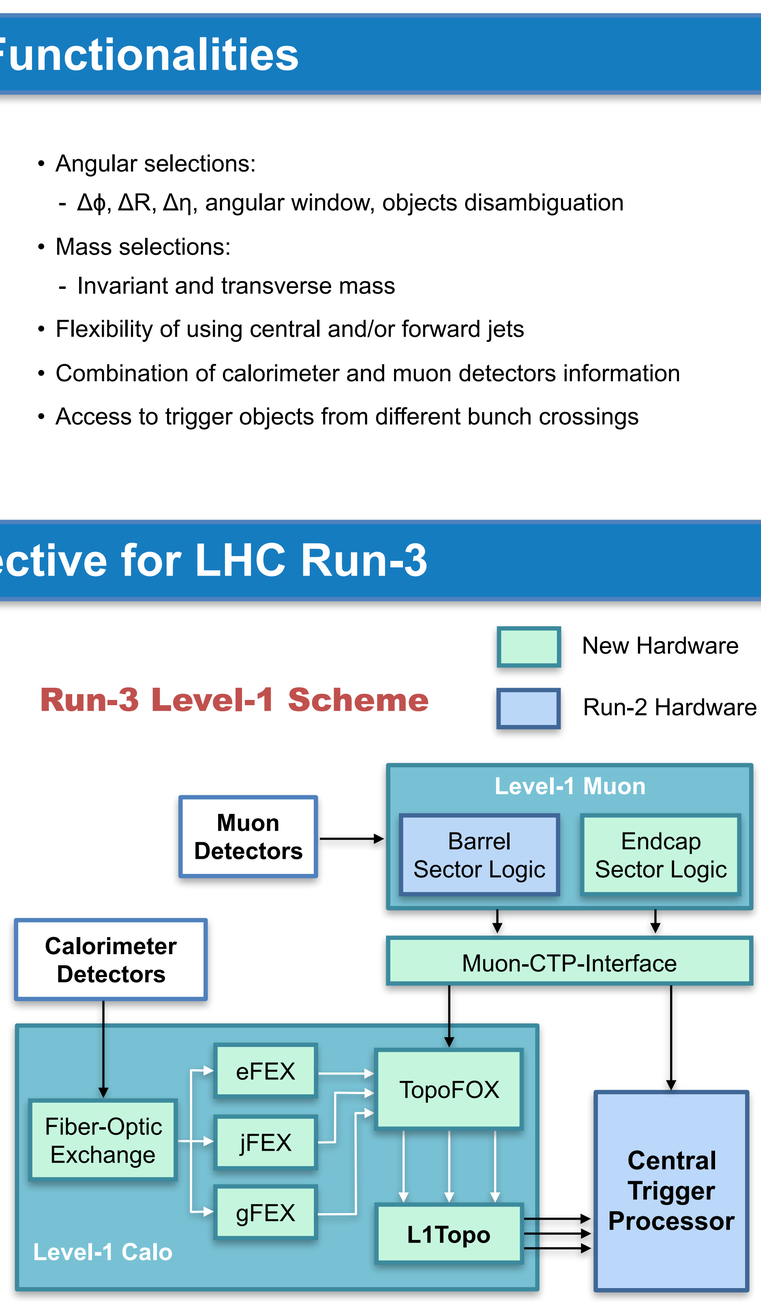
Perspective for LHC Run-3

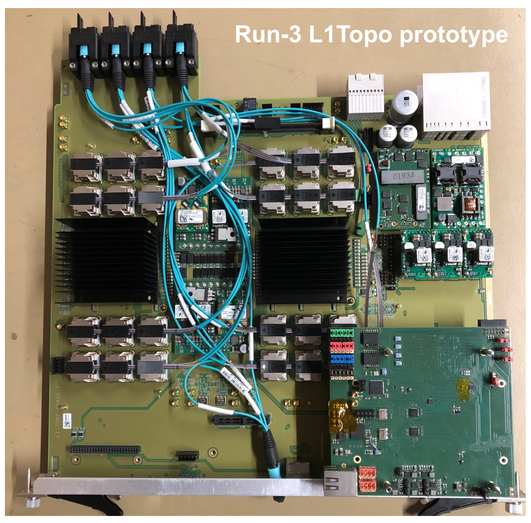
During the second long shutdown, several Level-1 trigger systems will be upgraded:

Changes in L1Calo and L1Muon

- The L1Muon system will undergo a number of changes:
  - End-cap and Barrel Sector Logics enhanced
  - New MUCTPi with extra bandwidth to send more information to L1Topo and CTP
- The L1Calo system will be replaced by **three new types of Feature Extractor boards (FEX)** providing higher granularity trigger towers

Run-3 Level-1 Scheme





Specific changes to L1Topo

- The Run-2 Topological Trigger System will be replaced by a **new system consisting of three boards**, each containing:
  - 2 Xilinx UltraScale+ FPGAs for algorithm computation with enhanced processing power
  - 118 input fibers per FPGA
  - 24 output fibers per FPGA
- In contrast to Run-2, the new L1Topo system will run topological and some non-topological algorithms

The commissioning plan foresees using the Run-2 Legacy system while commissioning the Run-3 system.

Summary

- The Level-1 Topological Trigger has been successfully commissioned and used during Run-2
- It added new features to the Level-1 Trigger, such as the possibility of combining information from both the Calorimeter and the Muon detectors
- It has been crucial for many analyses targeting high rate low p_T trigger signatures
- A bitwise simulation of the algorithms helped in the validation process, and in 2018 all the triggers used for physics showed a hardware-to-simulation agreement better than 99%
- For Run-3, three new L1Topo hardware boards including higher processing power FPGAs will be built and will replace the Run-2 system

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For more information:
[1] ATLAS Collaboration, https://twiki.cern.ch/twiki/bin/view/AtlasPublic/TriggerOperationPublicResults
[2] R. Simoniello, *The ATLAS Level-1 Topological Processor: from design to routine usage in Run-2*, ATL-DAQ-PROC-2018-044 (2018)

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