LAUROC1
Liquid Argon Upgrade Read Out Chip

OMEGA : S. Blin, S. Conforti, C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau

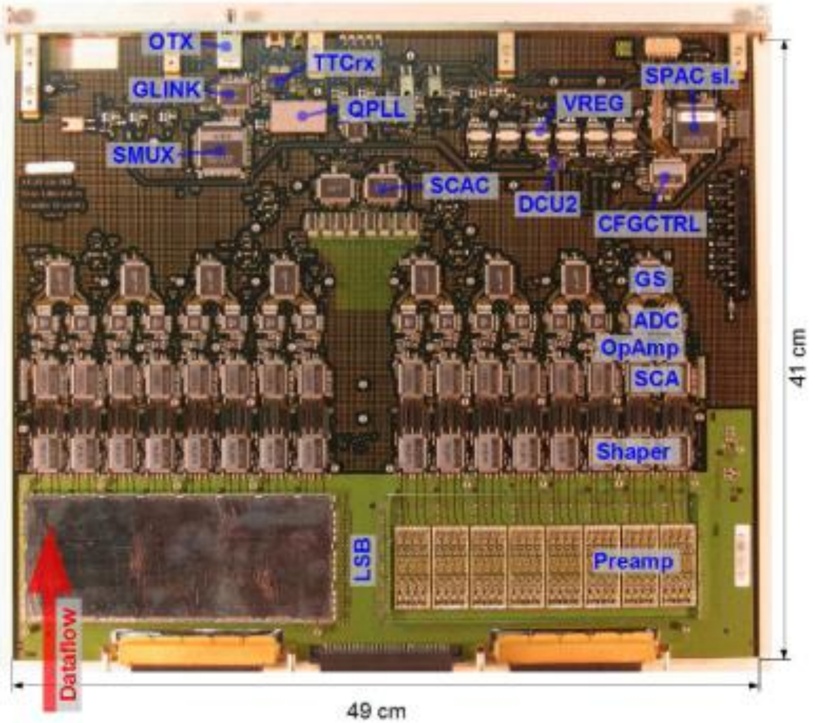
LAL : K. Alkhoury, L. Duflot, N. Morange, L. Serin, S. Simion

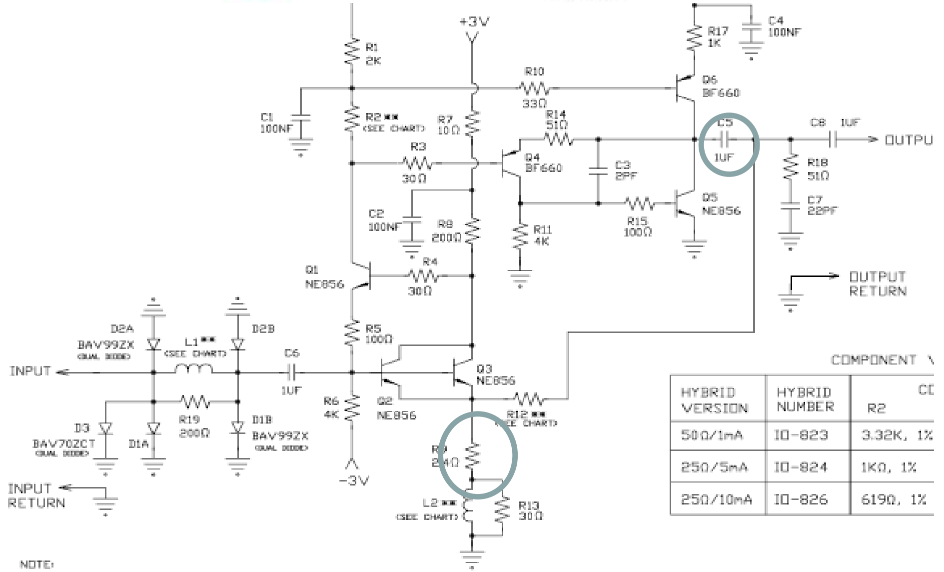
BNL : H. Chen, M. Dabrovski H. Liu

- LAUROC : liquid Argon Upgrade Read Out Chip
- Aurochs [ˈɔːrɒks] : extinct species of Wild Ox
- Strong and bullish
- [Astérix en Hispanie]
- Suggested by Claude Colledani !

Context : ATLAS Liquid Argon calorimeter upgrade

- New design to speed up the digitization up to 40MHz and remove analog memories and obsolete components
- Replace preamps and shapers (and ADCs, SCAs,Glink…)
- Hybrid preamps used (0T configuration) →precise input impedance
  - Very low noise (~0.4 nV/√Hz)
  - Large supplies -6 +12 V
  - Some precision components and uF capacitors
  - 3 flavours : ‘A’, ‘B’, ‘D’
- Shapers used AMS 1.2um BiCMOS

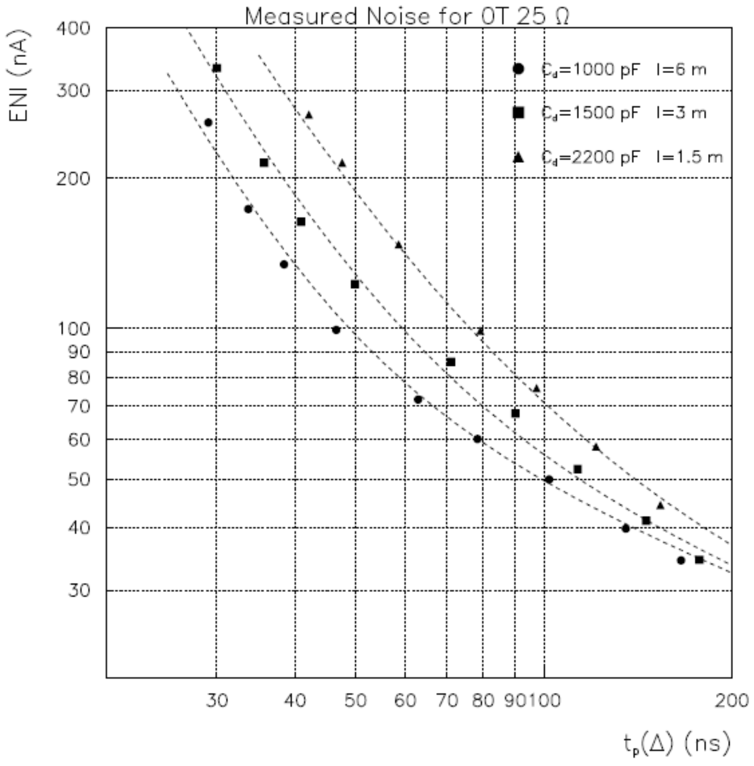




Preamplifier requirements

- Precise input impedance : Z_{in}= 50 Ω (Front) or 25 Ω (Middle/Back) to terminate the cables from the detector

- Low noise < 10 Ω, with C_d= 400 pF (Front) or 1.5 nF (Middle/Back)
- Current sensitive configuration (large Cd, long duration signal) tp = 50 ns
  - $ENI^2 = \propto \frac{e_n^{\ 2} C_d^{\ 2}}{t_p^{\ 3}(\Delta)} + \beta \frac{i_n^{\ 2}}{t_{p(\Delta)}} \text{ where } \Delta \text{ is a triangle}$
  - 0T50 400pF: ENI@50ns=55nA, 0T25 1.5nF: ENI@50ns=150nA
  - Spec : < 120 nA for 50 Ω and ENI < 300 nA for 25 Ω (pileup dominating at HL LHC)



- Dynamic range:
  - Front 50 Ω : from 50 nA noise up to 2 mA = 40 000 or 15.5 bits
  - Middle and back 25 Ω : from up 200 mA to 10 mA = 50 000 or 16 bits

- Radiation resistance : ~ 1 Mrad

→ "Universal" preamplifier with selectable dynamic range and input impedance (25/50 Ohm)

LAUROC0 overview

- Integrates 8 channels with variants of preamp: PA 25 and 50 Ohms as well as a preamp 25-50 for which Zin can be selected by SC

$$Z_{in}\,PA = \frac{R_0 + Zin(SCB)}{1 + |G|}$$

- Preamp Input impedance
  - Super Common Gate: low input impedance
  - Fine tuning of Zin (±5%) possible with C2

- Noise :

- Amplifier = low noise voltage sensitive

- “Electronically cooled” resistor

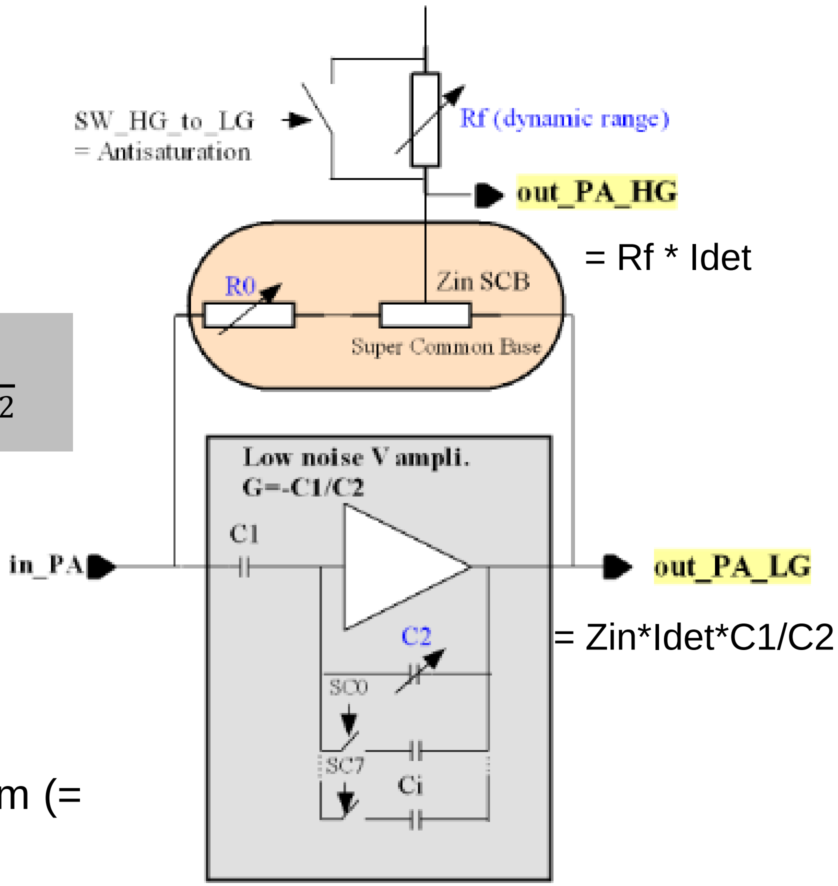
$$\frac{4kTR_0}{(1 + |G|)^2}$$

- HG and LG outputs available :

Discriminator at the output of the LG PA used to short R_f and to avoid saturation of the HG

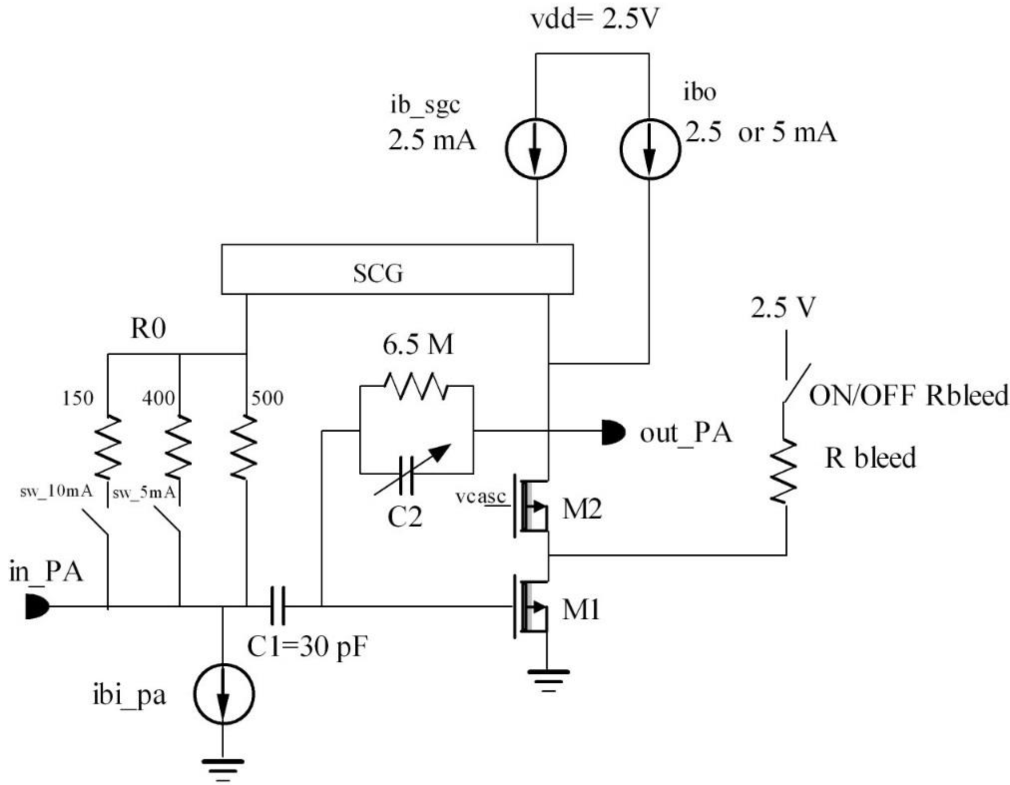
⇒ This system generates some non linearity

⇒ Lauroc1 built around this preamp “PA_25_50” but wo the discri system (= wo the HG output)

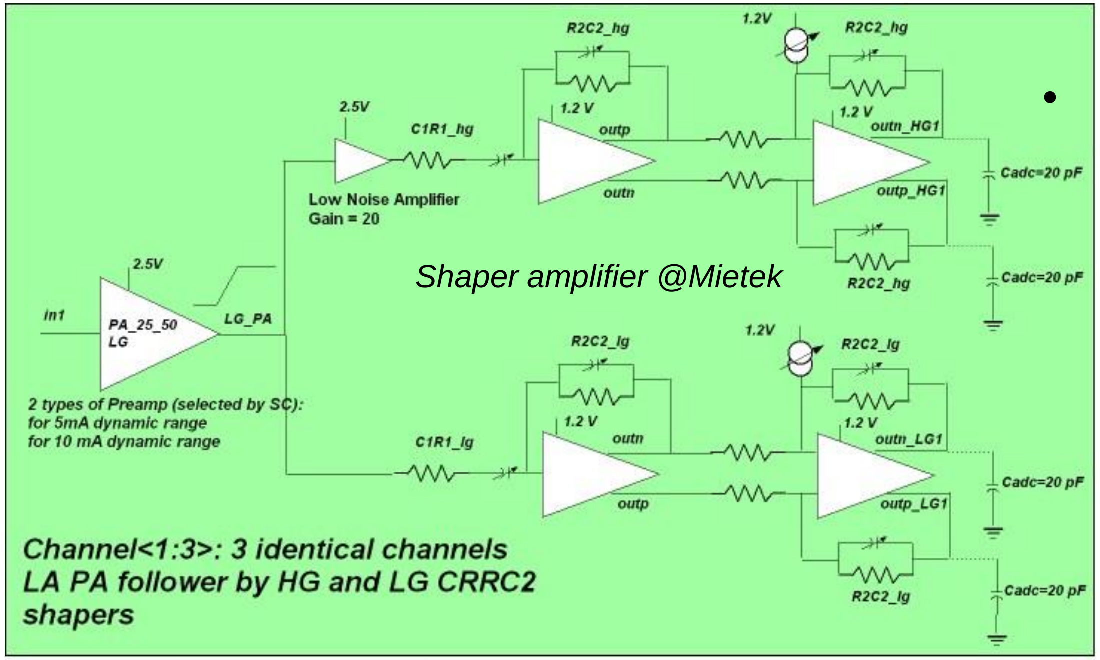


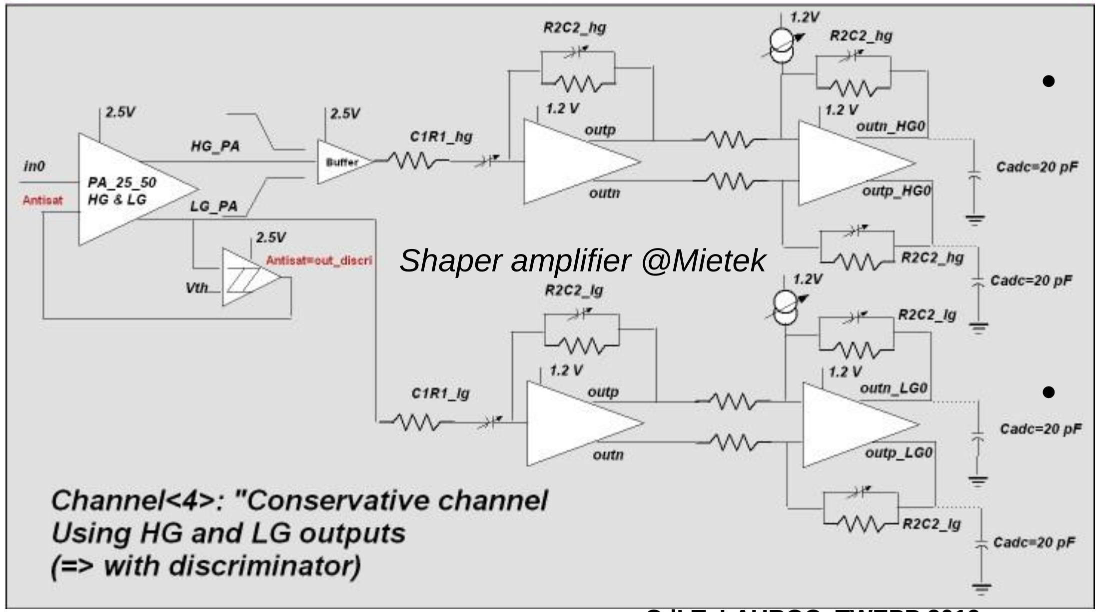
R0, C2 tunable to set absolute value of Zin
Ci: 8-bit fine adjustement of Zin (±5%)
using Slow Control parameters

- Input transistor = 1V NMOS transistor, 3000 µm/ 0.25 µm
- Cascode trans: 2.5V NMOS transistor
- Dynamic range adjustable by R0
- Input impedance adjustment by Cf (8 bits)
- Possibilty to tune the current that flows in the input preamp
  - ibo_pa can be set to 2.5 mA or 5 mA using SC parameter
  - R_bleed: can add 6 mA using SC parameter



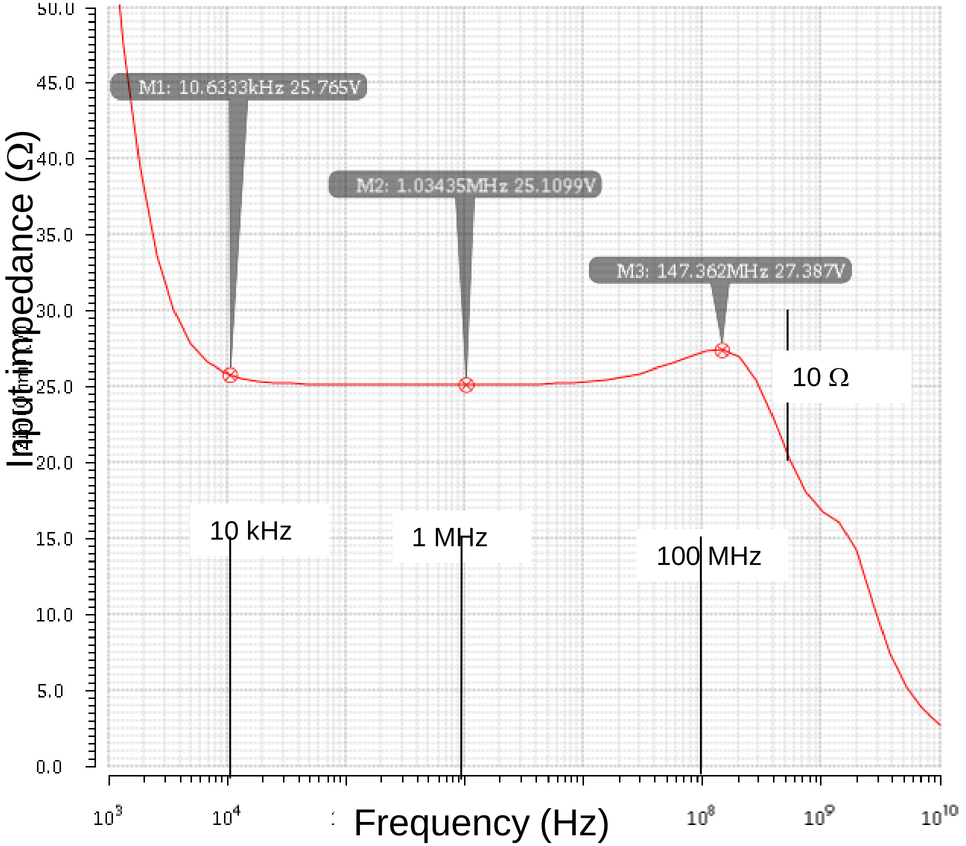
LAUROC1 overview





- **4 channels using the preamp_25_50 of Lauroc0 (**Zin tuneable by SC)
  - Channel 1, 2 and 3: LG preamp followed by one CRRC2 HG shaper and one CRRC2 LG shaper
  - Channel 4: conservative channel using the discriminator and HG and LG PA for comparison
- Preamps followed by CRRC2 shapers built around an amplifier: designed by Mietek Dabrowski @BNL
- τ tuneable between 1.25 ns and 20 ns

LAUROC0 25 Ω preamp: Simulations of Zin



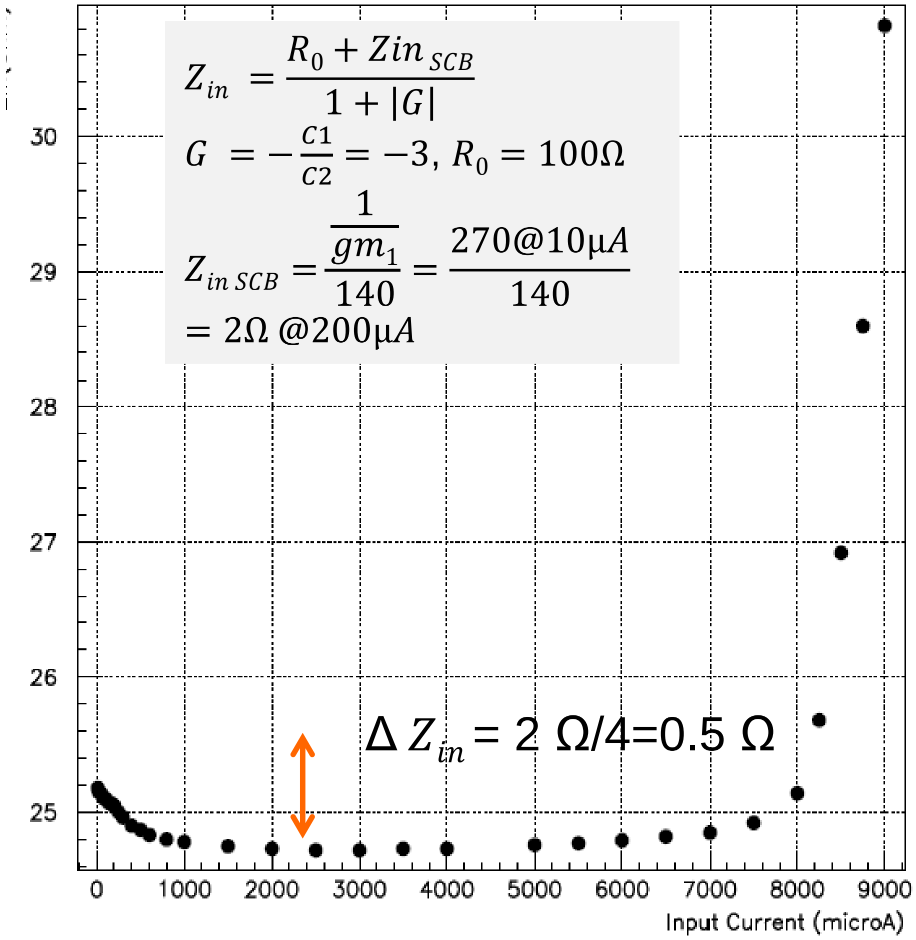
Impedance flat from 10 kHz to 100 MHz
< 1 Ω variation versus current due to
Super Common base Zin variation

Zin simulation

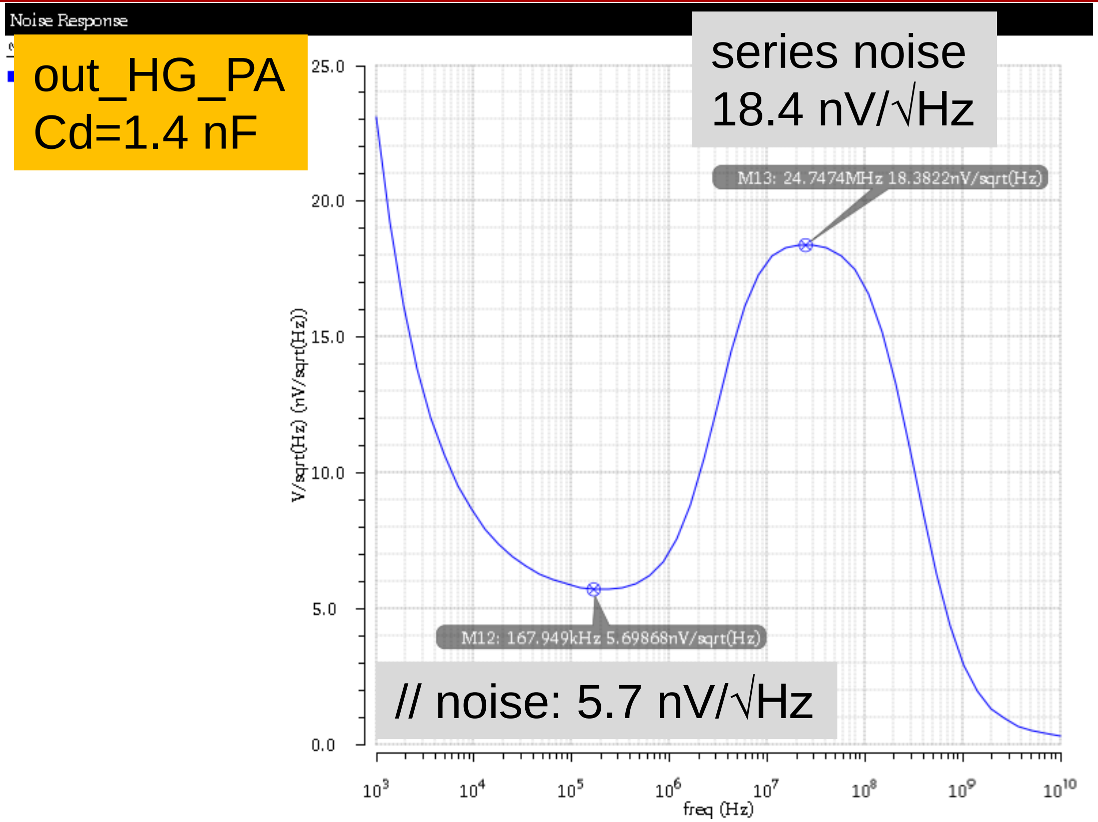
$$Z_{in} = \frac{R_0 + Zin_{SCB}}{1+|G|}$$

$$G = -\frac{C1}{C2} = -3,\ R_0 = 100\Omega$$

$$Z_{in\ SCB} = \frac{\frac{1}{gm_1}}{140} = \frac{270@10\mu A}{140} = 2\Omega\ @200\mu A$$

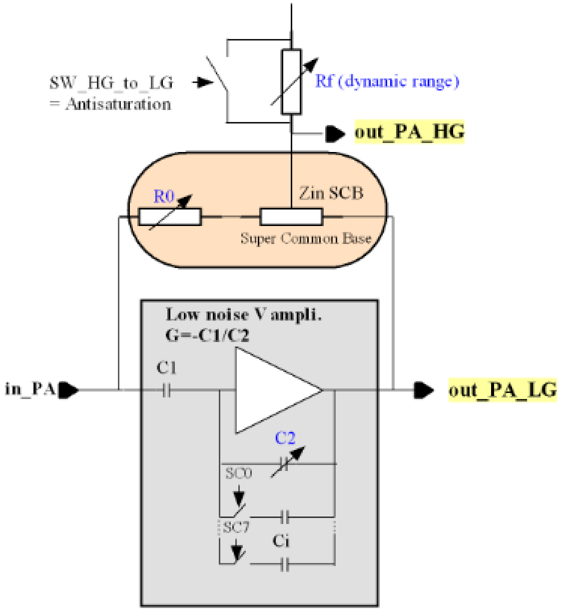


HG 25 Ω PA: Equivalent Output Noise



$$\frac{4kTR_0}{(1+|G|)^2}$$ with G=-3

R_0=100 Ω =>
Equ. Noise: 0.32 nV/√Hz or 6.25Ω



R0, C2 tunable to set absolute value of Zin
Ci: 8-bit fine adjustement of Zin (±5%)
using Slow Control parameters

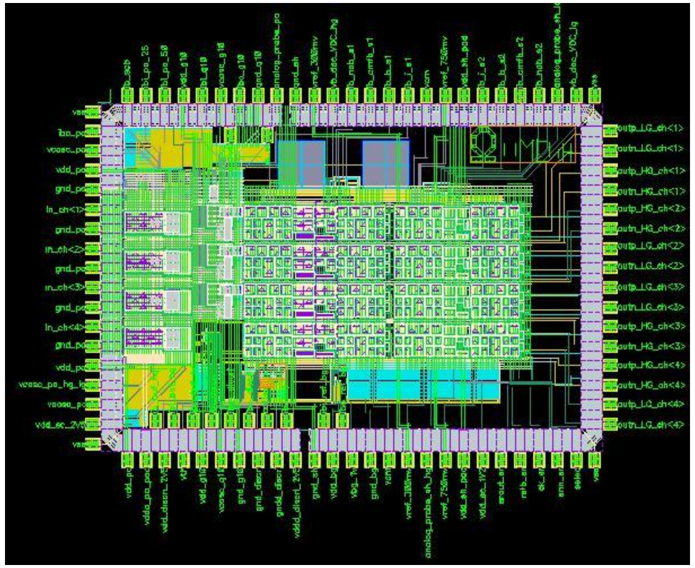
// noise dominated by
R_f=1K (51%)
R_{deg} =15K (26%)

Series noise:
R_0=100 (43%)
NMOS ampli (24%)
NMOS SCB amp (8%)

⇒ Gain at the output of the preamp = 1K/25=40
⇒ Input Noise:
18.4 nV/40=0.46 nV/√Hz or 13 Ω

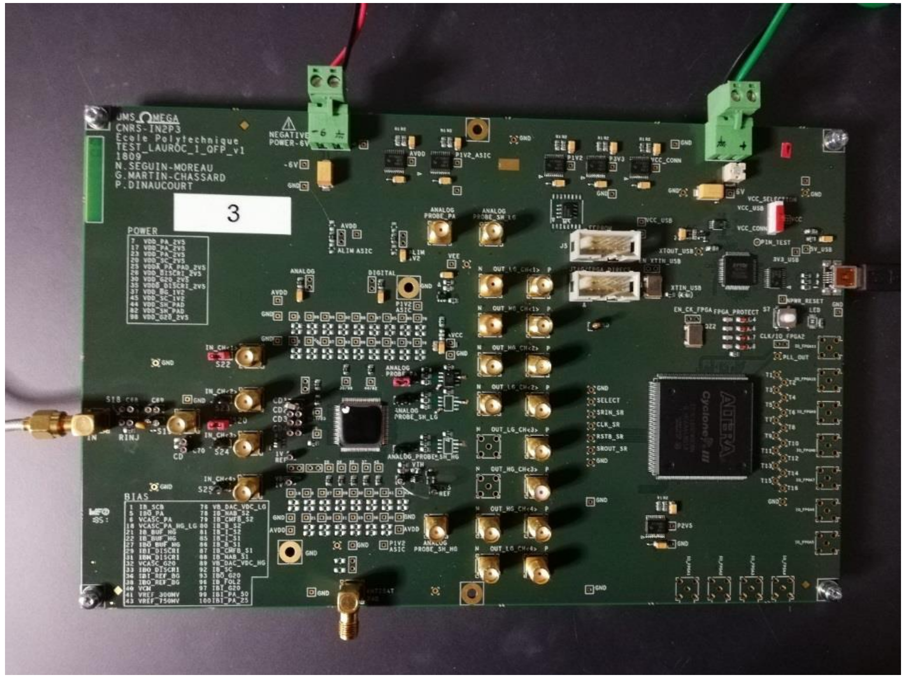
2 setups:
Omega testboard (characterization)
LAL/BNL setup= Injection board (Toy cal. board)+ external Pulser (Larg Pulse) + DUT + ADC

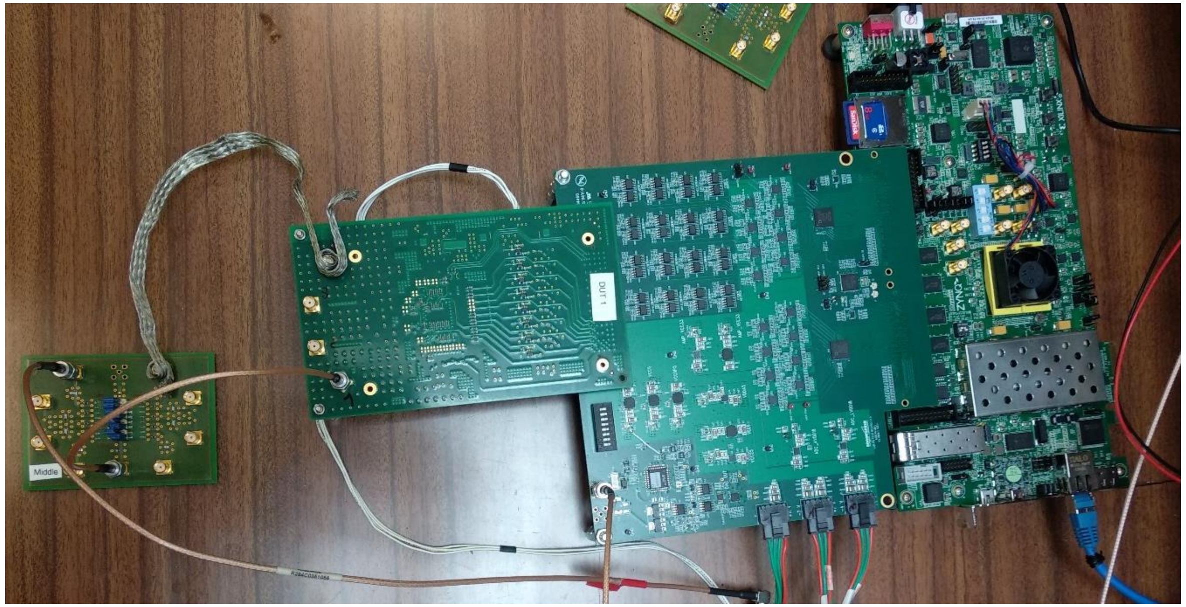
Measurements performed on scope and using the full chain (with ADC)



The chip size is 2.8 mm x 2.5 mm.

Packaged in a LQFP 100 14*14 package.

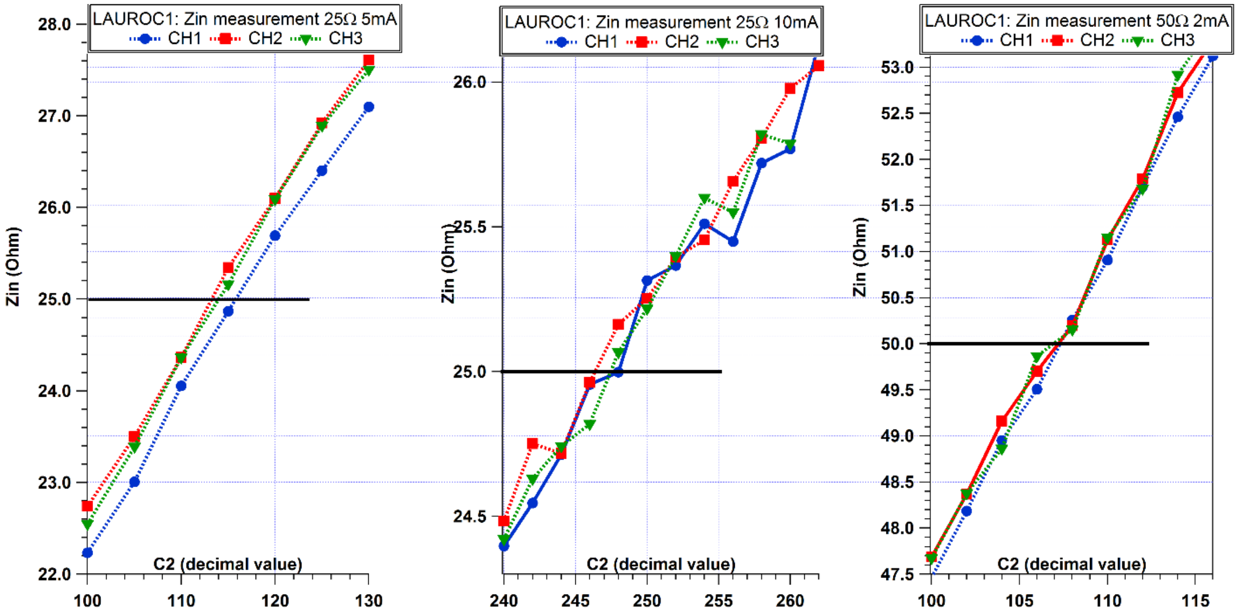




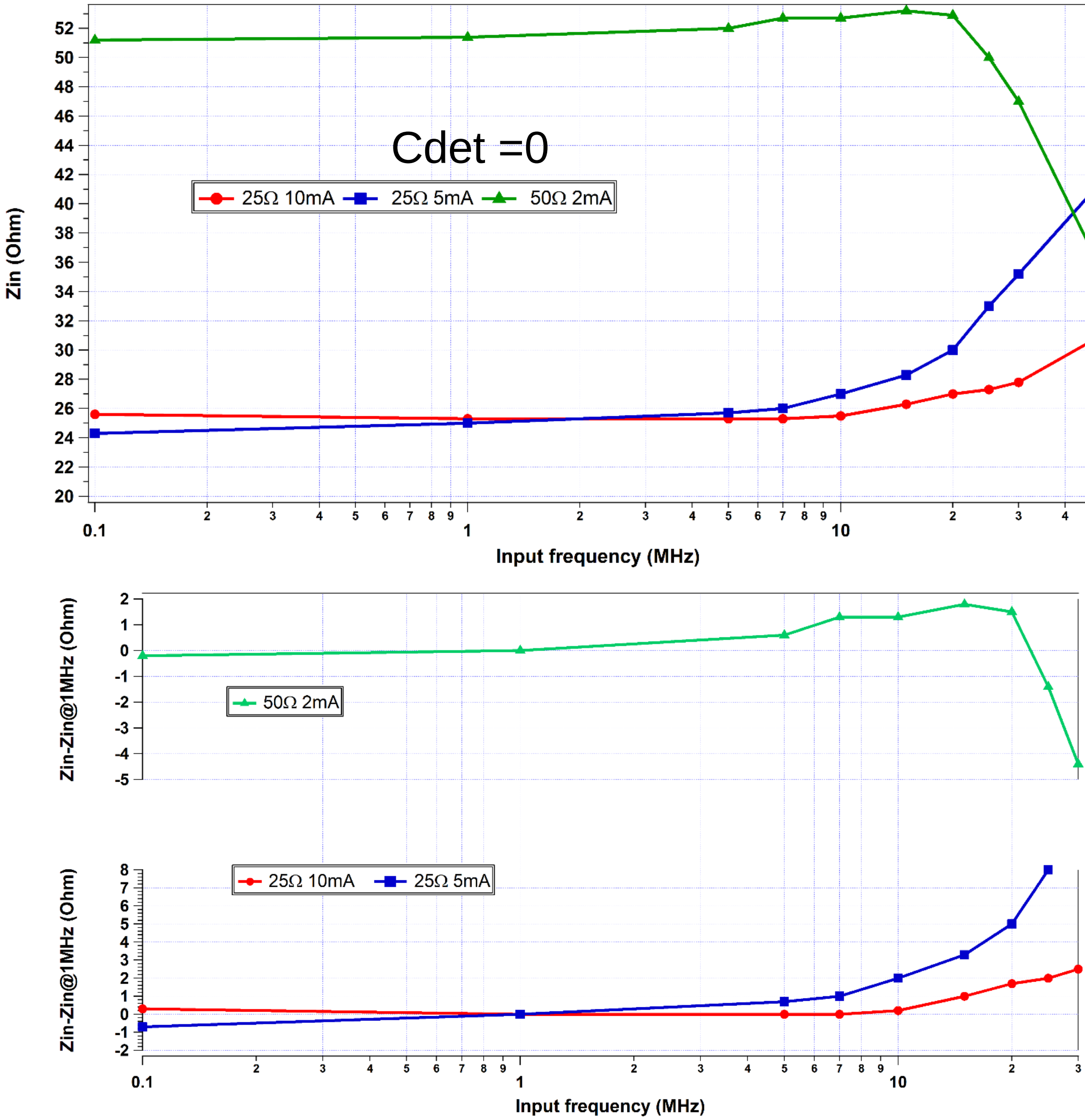
LAUROC1 measurements: Zin vs C2 uniformity and vs freq.

Ωmega

Specification: Zin tunable, 25 ± 2.5 Ω and 50 Ω ± 5 Ω up to 20 MHz



Zin vs C2 (9 bits, LSB = 31.6 fF) for 3 channels

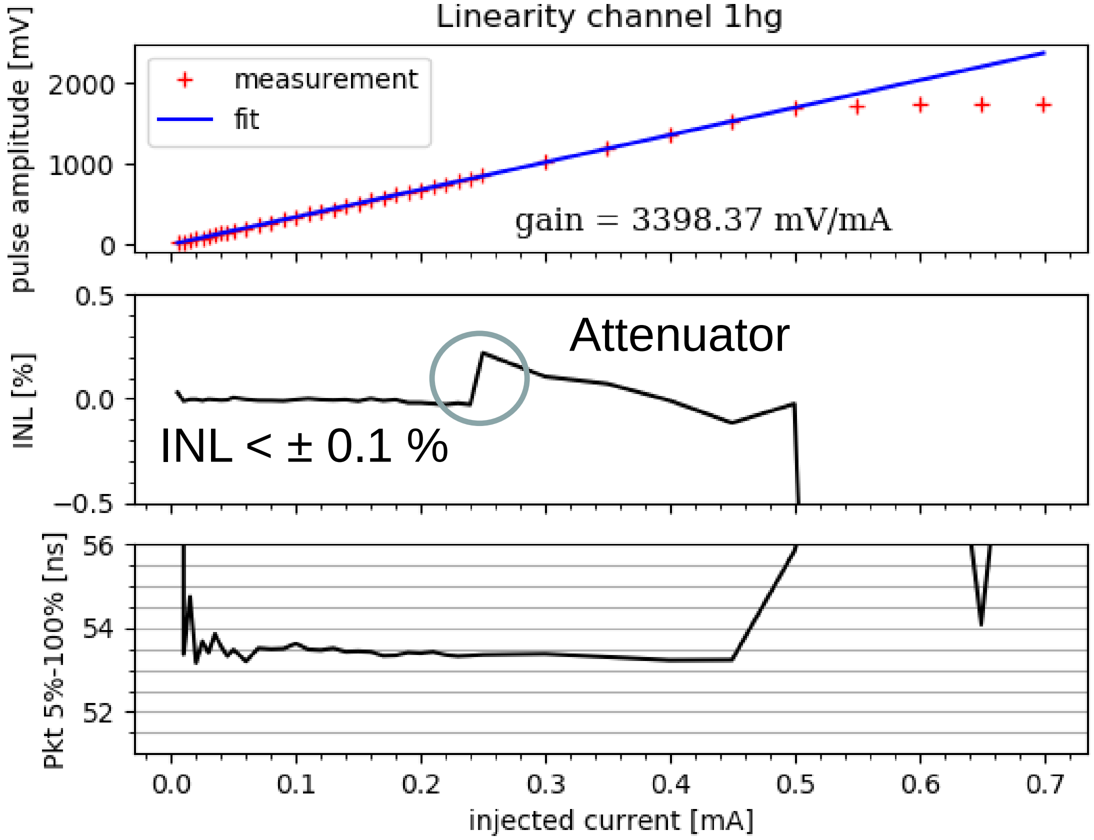


LAUROC1 25 Ω 10 mA config: Linearity measurements

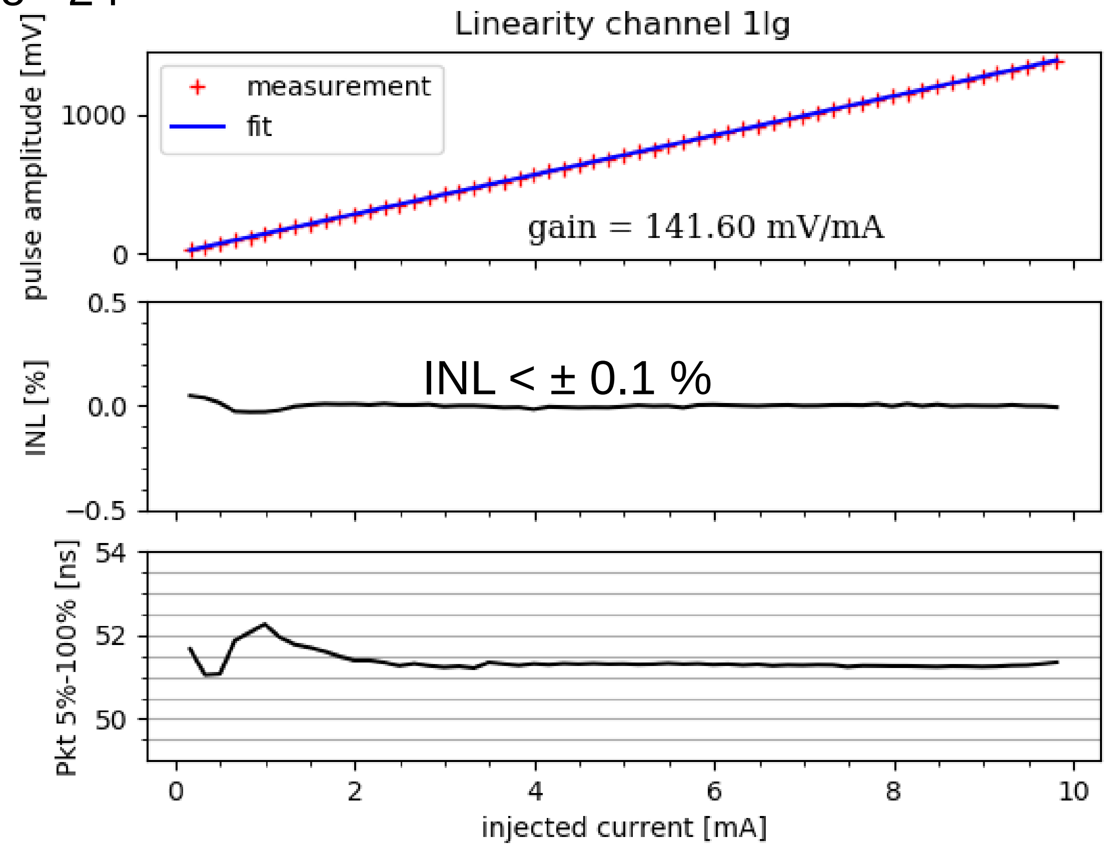
Specifications	
Linearity	INL < ±0.2% on High Gain output
	INL < ±0.5% on 80% of Low Gain dynamic range
	INL < ±3% on the full dynamic range

HG/LG ratio= 24

HG



LG

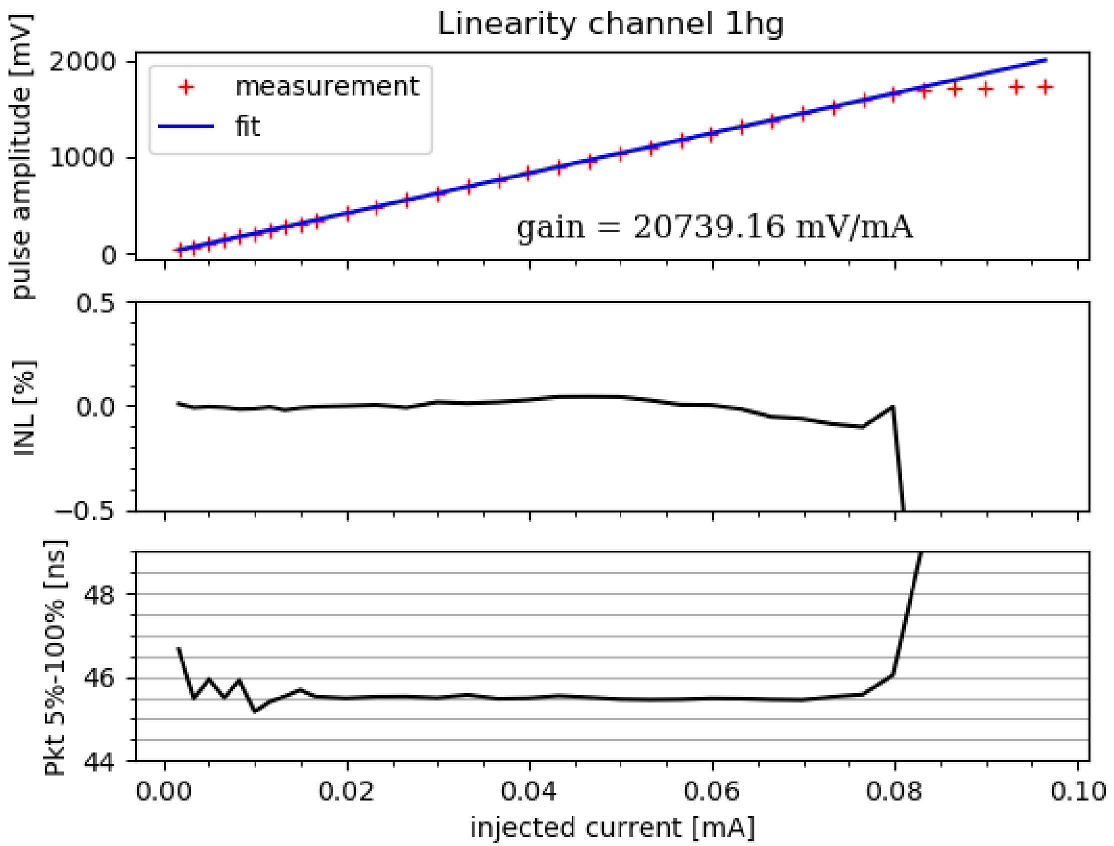


LAUROC1 50 Ω 2 mA config: Linearity measurements

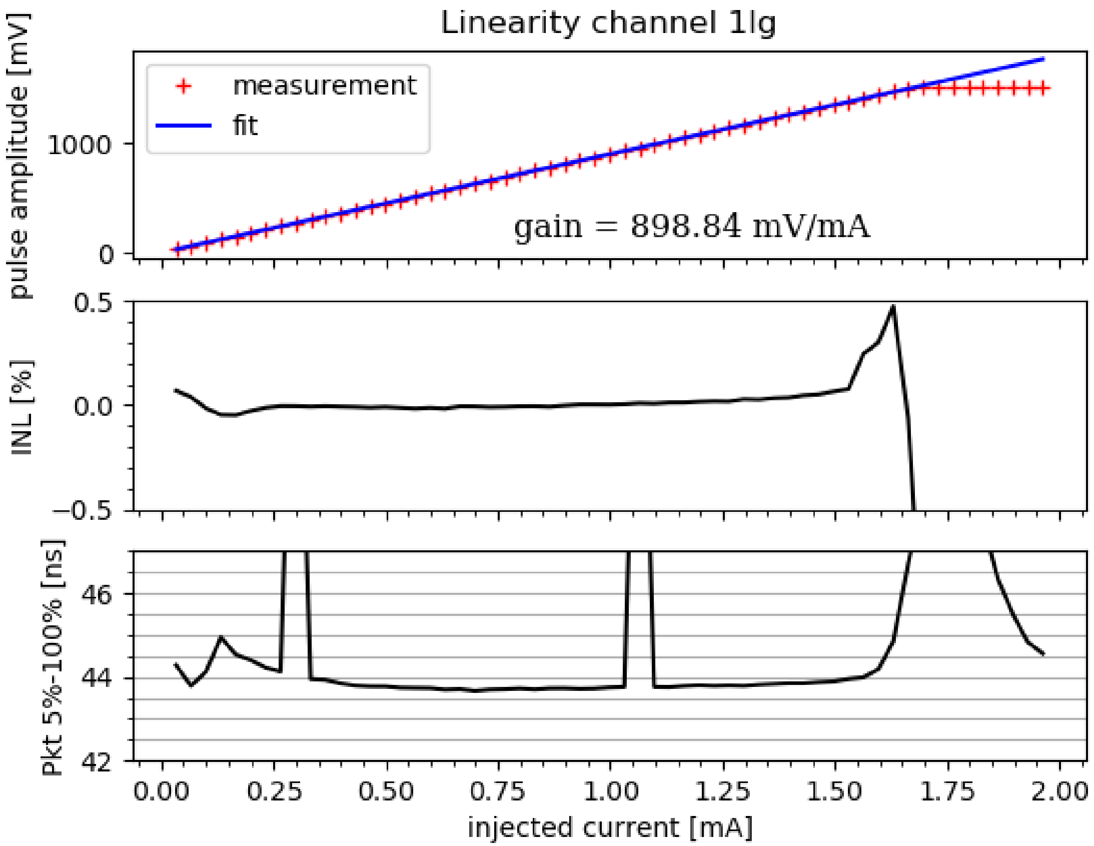
Specifications Linearity	INL < ±0.2% on High Gain output INL < ±0.5% on 80% of Low Gain dynamic range INL < ±3% on the full dynamic range

HG/LG ratio= 23

HG

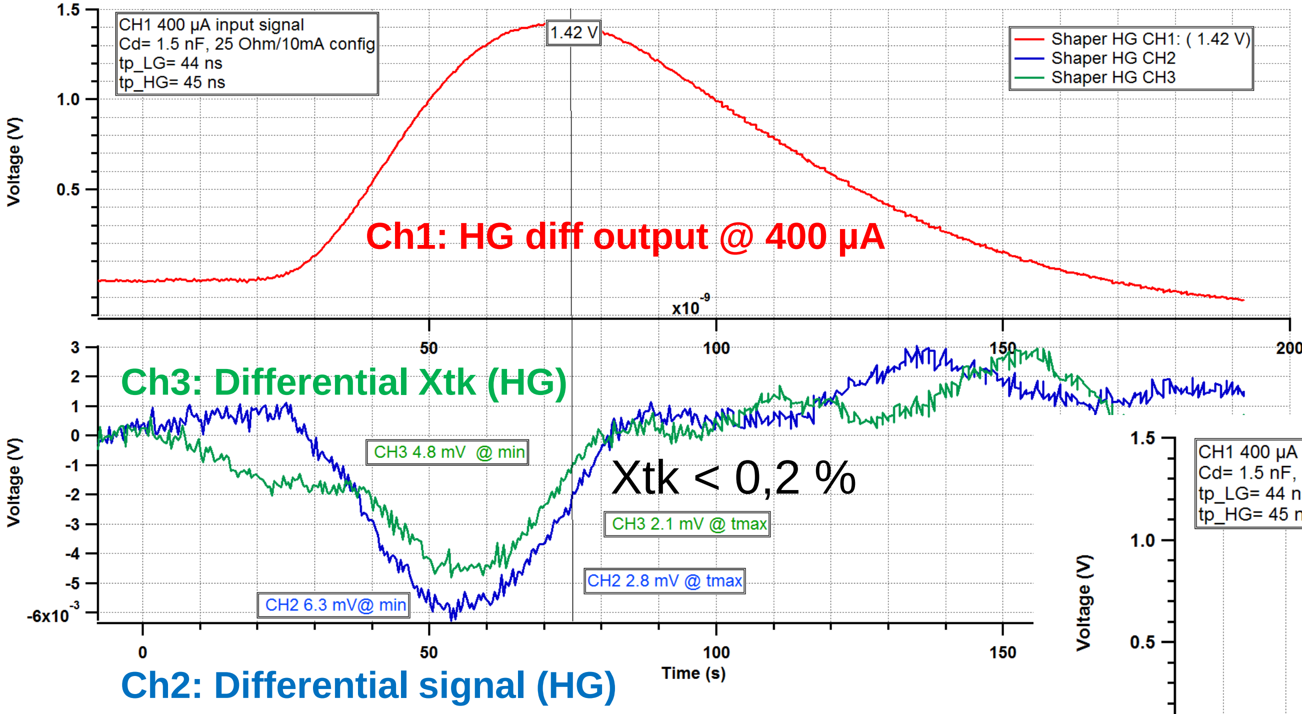


LG



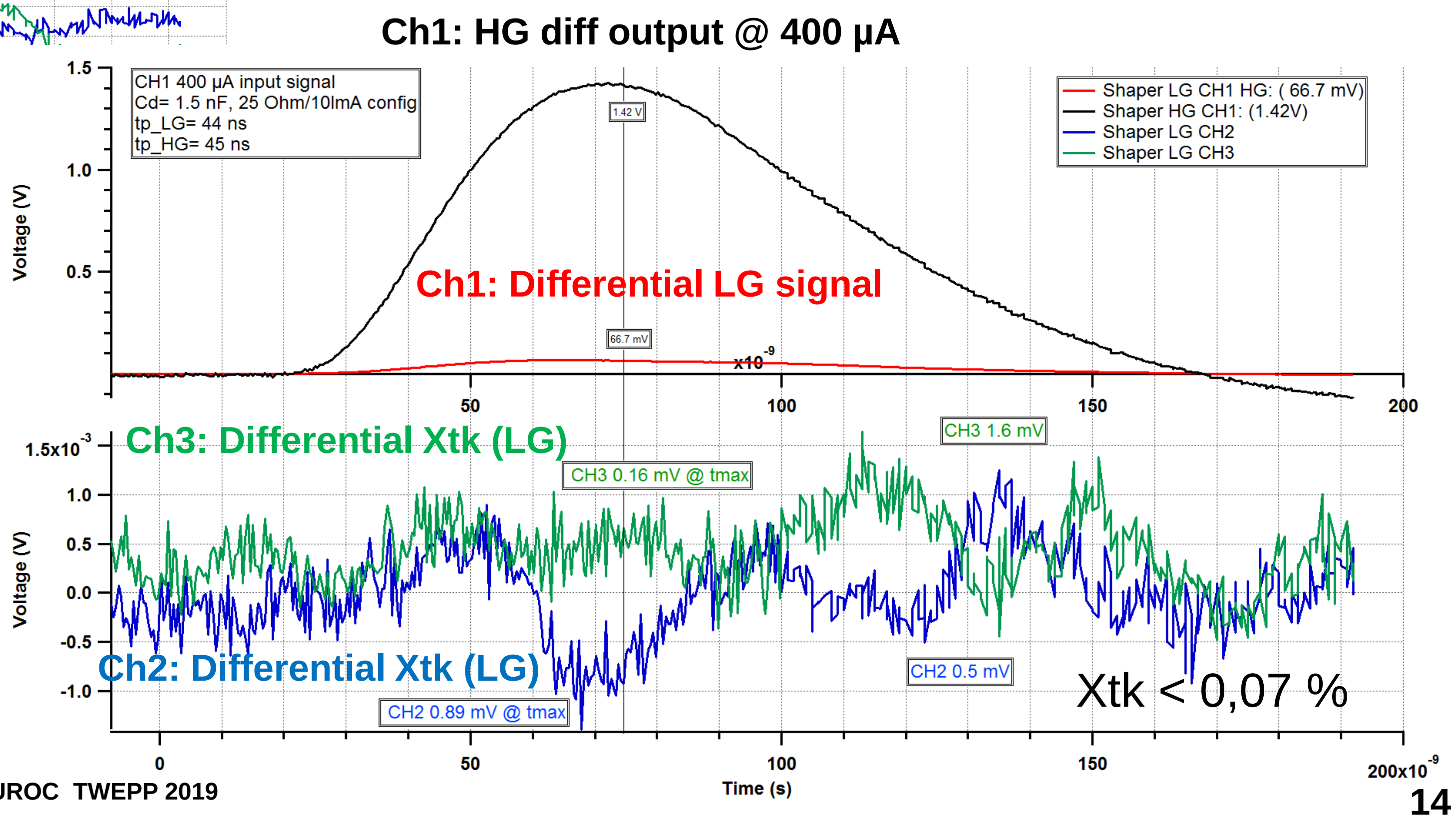
XTk (differential) between channels : 25 Ω 10 mA config

Injection of 400 µA in ch1, Xt in Ch 2 and Ch3. Cd= 1.5 nF on all channels

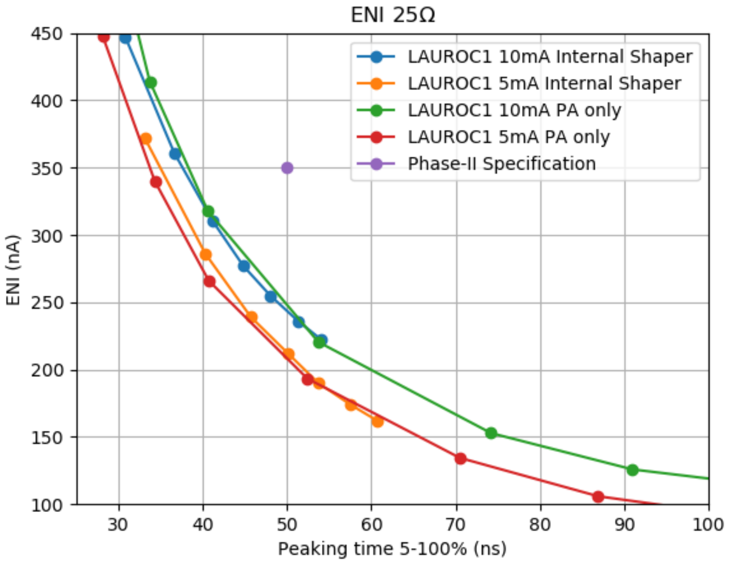


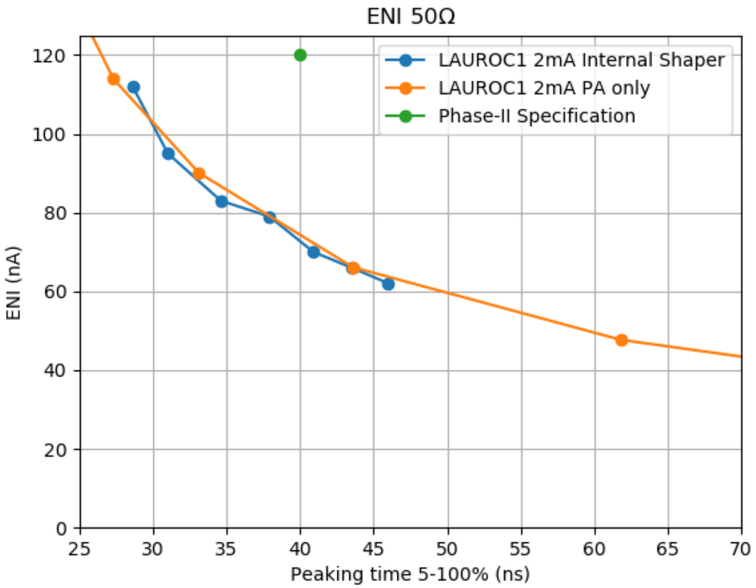
Specification:

Cross-talk	<0.5%



ENI vs tp 5-100% (injection of LArg pulses)





Specification:
< 300 nA @ tp $_{5\text{-}100\%}$ = 50 ns, Cd=1.5 nF for 25 Ω config
< 120 nA @ tp $_{5\text{-}100\%}$ = 50 ns, Cd= 330 pF for 50 Ω config

LAUROC1 noise: below specification but larger than expected by 20%
Series noise as expected : e_n = 0.45 nV/√Hz Ctot=36 pF and parallel noise negligible, even with leakage current

But large 1/f noise (400 e-)

Attributed to dielectric noise in input C1=30 pF MIM capacitor (goes as 4kTωCtanδ): tanδ of SiO2= 0,002 => 278 e-

Special channel added in LAuroc2 with external capacitor for C1 to prove it definitively

Series noise input transistor

3000/0.25 µm transistor at I_D=4 mA

Measurement = 2 * theory

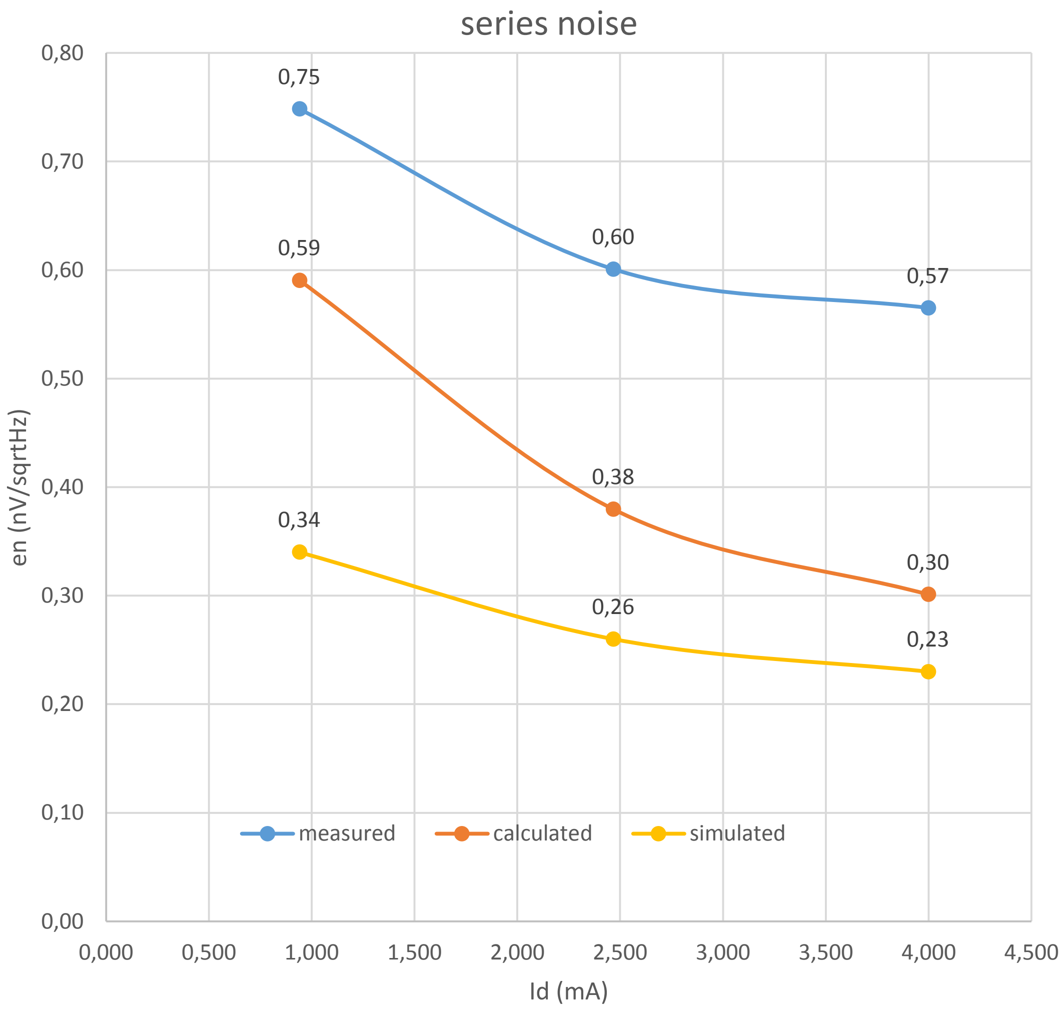
Simulation < theory !

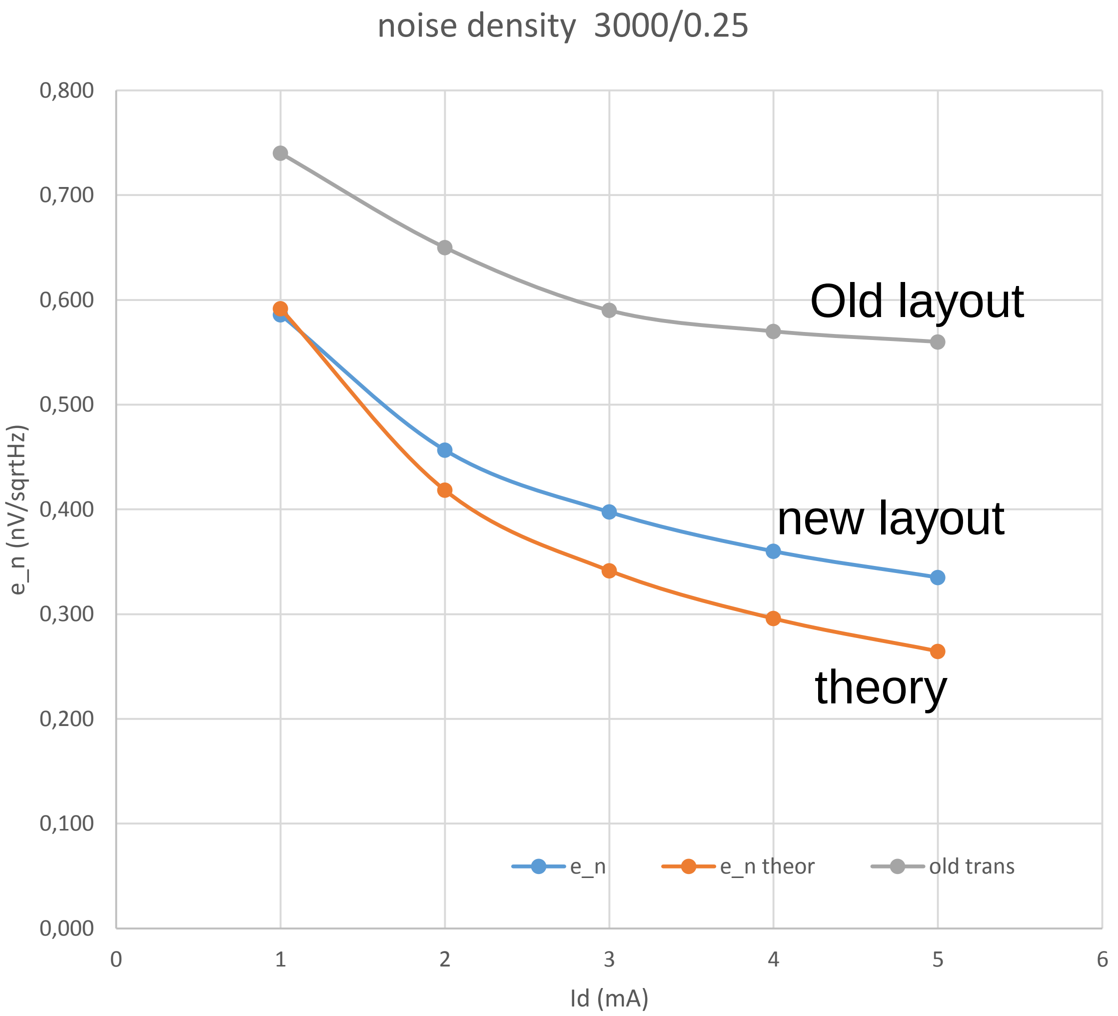
New layout with minimized bulk contribution

Measured noise now at 0.36 nV/√Hz

close to calculations = 0.3nV (0.56nV before)

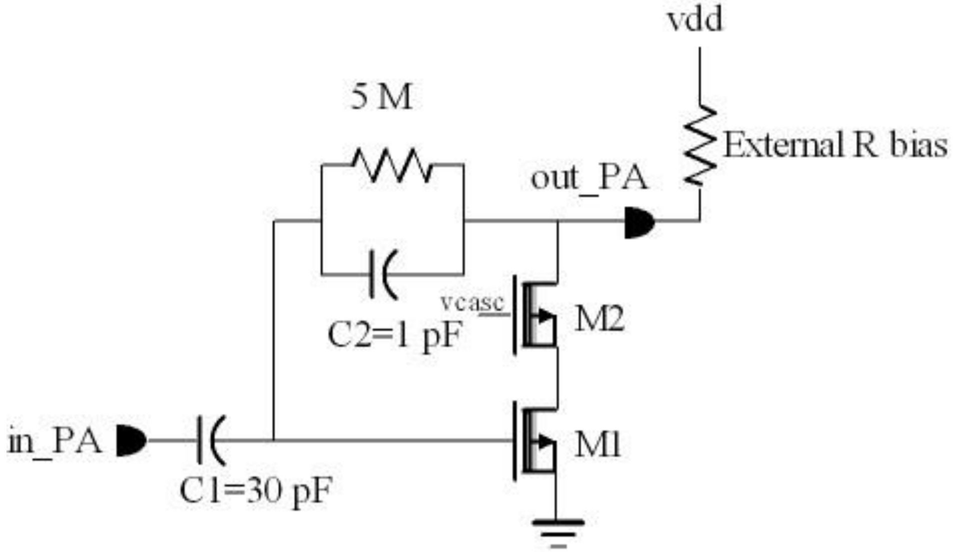
Difference corresponds to 0.2 nV/√Hz ~ 2 Ω





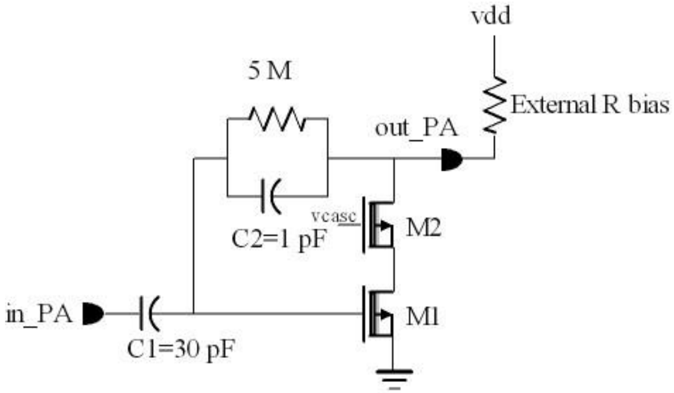
Input preamp measurement

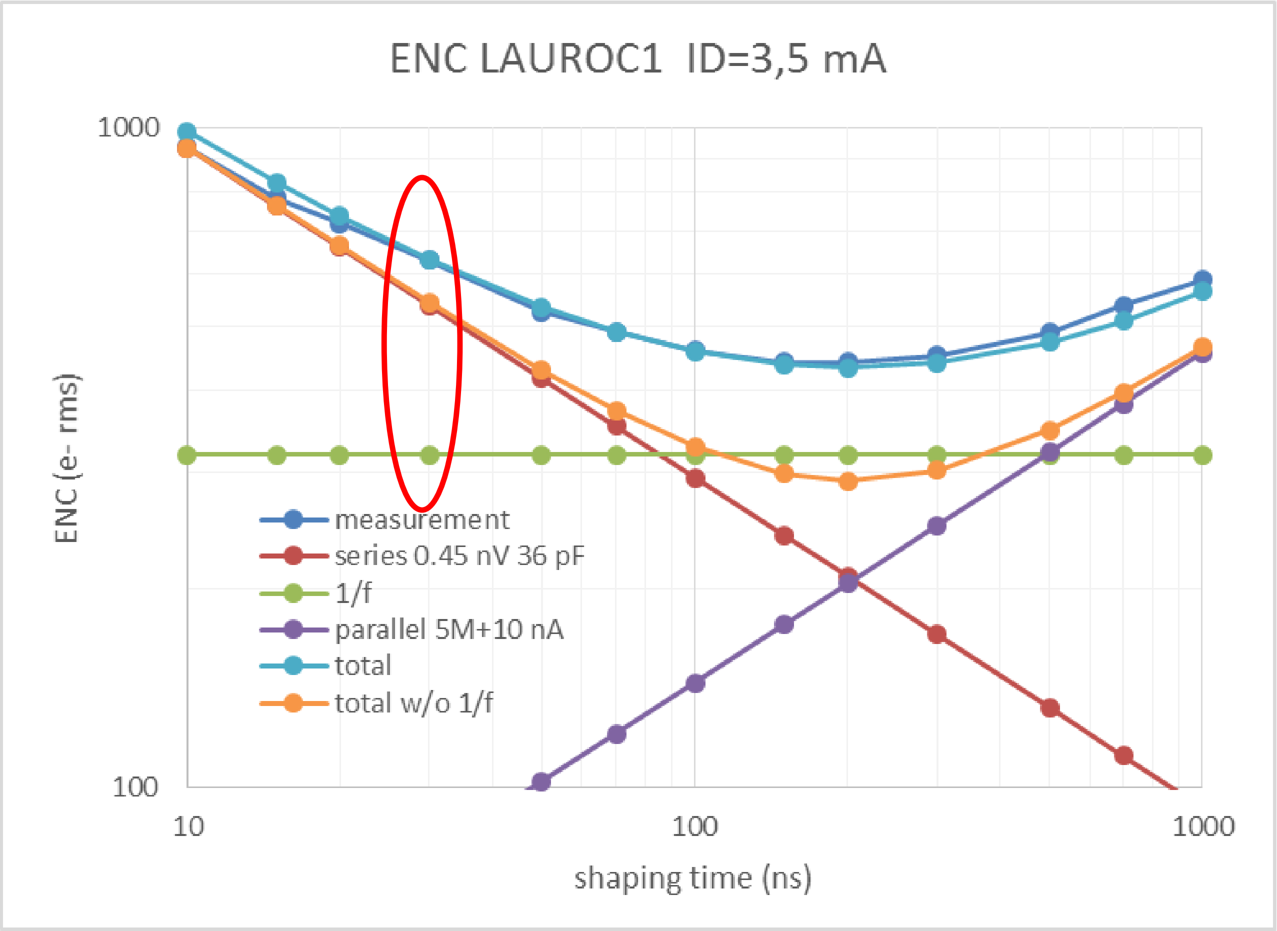
- LAUROC1: Low noise input preamp measured alone as charge preamp followed by external variable CRRC² shaper. Cf = 1 pF
  - All current sources switched off : preamp biased externally by external RL
  - Noise expected : ENC = 174 $e_n C_{tot}/\sqrt{t_p}\,(\delta) \oplus 166\, i_n \sqrt{t_p}\,(\delta)$
  - Parallel noise due to Rf = 5 M and leakage current, measured I_G=10 nA



PAC ENC measurement @ Id=4mA

- Good agreement for series noise : e_n = 0.45 nV/√Hz Ctot=36 pF
- Parallel noise negligible, even with leakage current
- But large unexpected 1/f noise (400 e-)
- At ATLAS shaping (tp = 30 ns) 1/f increases noise by ~20%



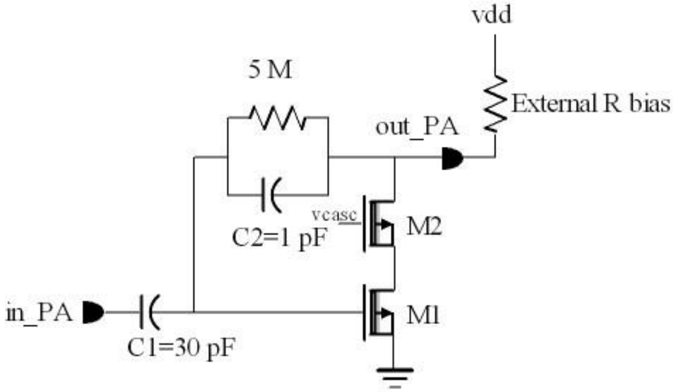


$$ENC = 174\, e_n C_{tot}/\sqrt{t_p}\,(\delta) \oplus 166\, i_n \sqrt{t_p}\,(\delta)$$

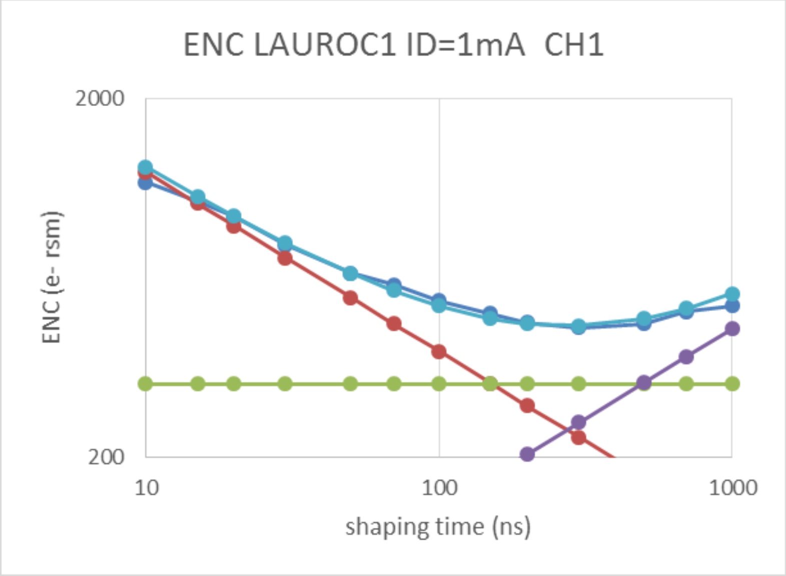
1/f noise origin

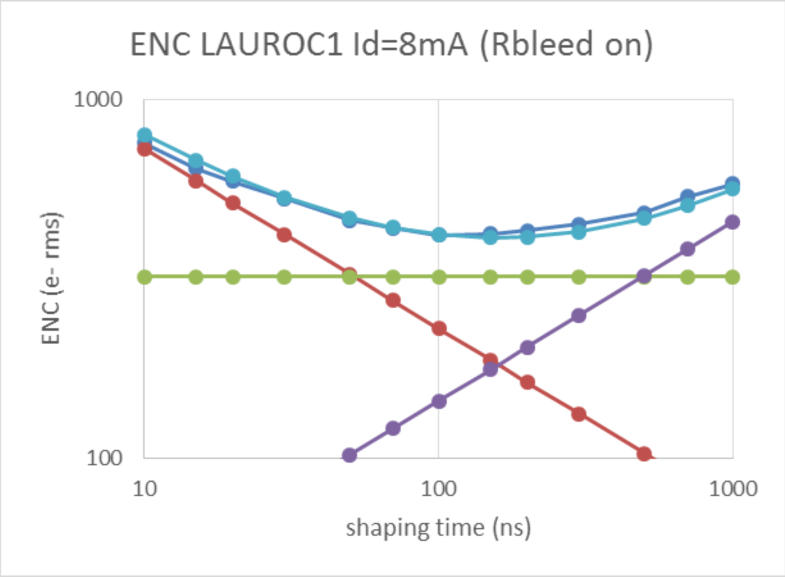
- 1/f can originate from the 2 transistors or the MIM cap
- Negligible 1/f measured on input transistor
- 1/f at the same level on CH4 which does not have 2.5V cascode

⇒ remains dielectric noise in the MIM input capacitor



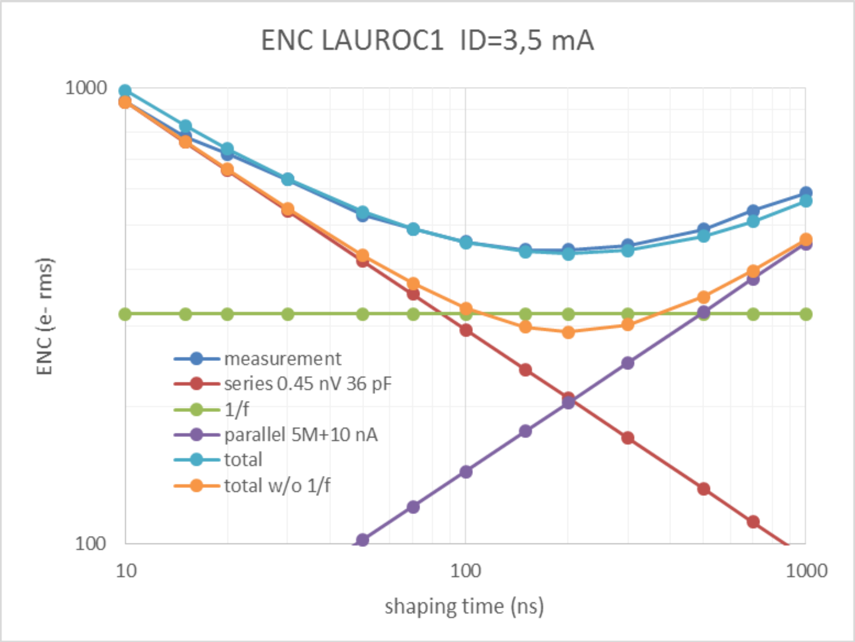
- Confirmed by measurement at small and large currents which shows 1/f unchanged
  - At 1 mA series noise plotted e_n = 0.6 nV/√Hz
  - At 8 mA e_n = 0.35 nV/√Hz

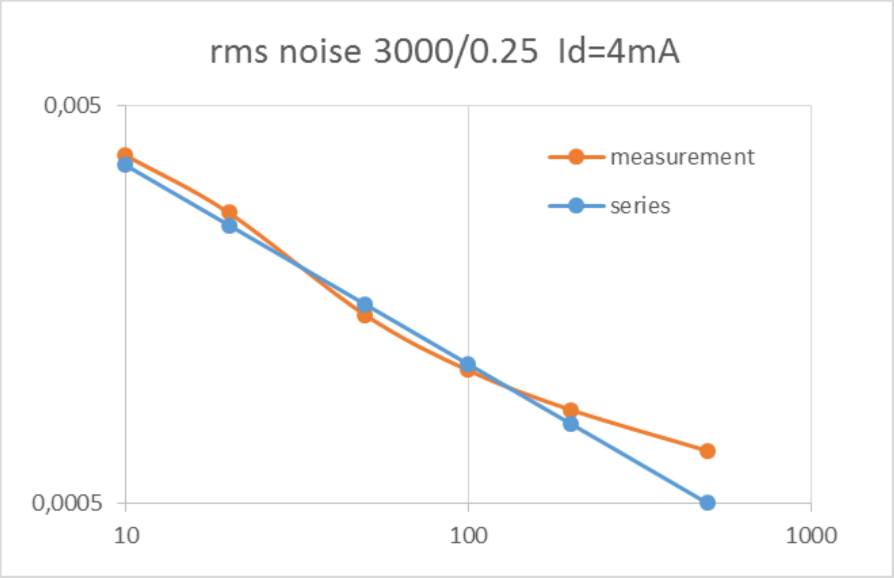




1/f input transistor alone

- ENC CH4 (1 V cascode)
- Input transistor alone (from previous run)
- Dielectric noise is parallel noise going as 4kTωCtanδ
- tanδ of SiO2= 0,002 => 278 e-, not far from the 320 e- given by the fit





Noise summary

- Noise measurements on preamp alone show good agreement with theoretical noise
- Series noise :
  - e_n = 0.6 nV/√Hz @ 1 mA
  - e_n = 0.45 nV/√Hz @ Id = 4 mA
  - e_n = 0.35 nV/√Hz @ Id = 8 mA
  - Total capacitance 36 pF : 10% parasitics in MIM + input transistor
- Parallel noise :
  - i_n = 0.09 pA/√Hz due to Rf=5M and 10 nA gate leakage current
  - Larger than expected but still negligible
- But large 1/f contribution
  - Independant of drain current or cascode type
  - Not seen on input transistor alone
  - Attributed to dielectric noise in input 30 pF MIM capacitor (goes as 4kTωCtanδ): tanδ of SiO2= 0,002 => 278 e-, not far from the 320 e- given by the fit
  - Increases series noise by ~20%
  - Would need a special channel with external capacitor to prove it definitively

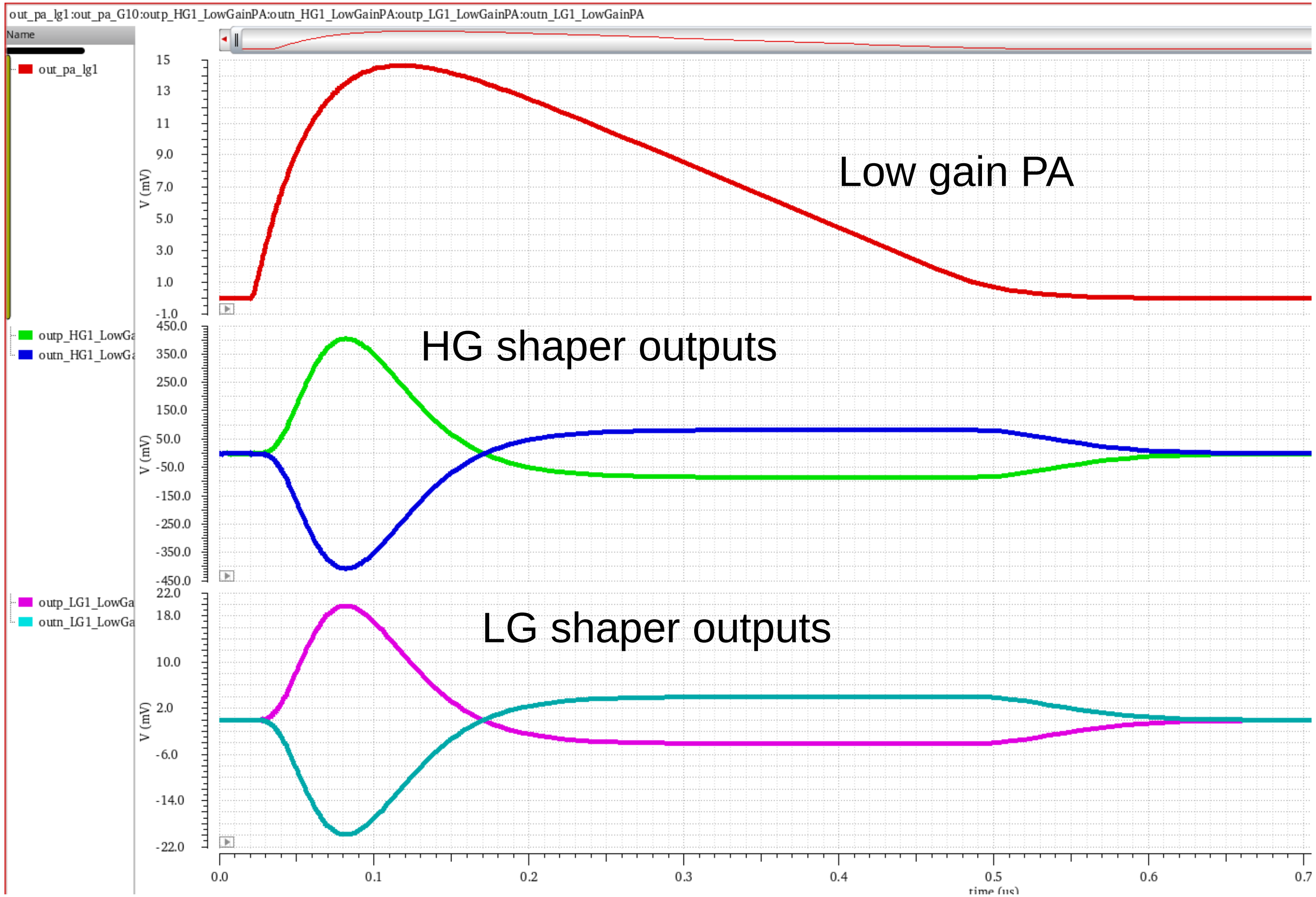
LAUROC conclusion

- Good performance for impedance matching and linearity
- Noise models were wrong for large transistors and large current : go back to BSIM3 model [J. Kaplon]
- Non negligible 1/f noise attributed to MIM caps
- Interesting design lower noise at BNL with fully differential amplifier [ALFE M. Dabrovski et al.]
- Final versions of LAUROC and ALFE submitted in sept.

- ATLAS at USC :

ATLAS EXPERIMENT

Waveforms


out_pa_lg1:out_pa_G10:outp_HG1_LowGainPA:outn_HG1_LowGainPA:outp_LG1_LowGainPA:outn_LG1_LowGainPA
Name
out_pa_lg1
outp_HG1_LowGa
outn_HG1_LowGa
outp_LG1_LowGa
outn_LG1_LowGa
Low gain PA
HG shaper outputs
LG shaper outputs
V (mV)
time (us)

SIMULATIONS: Channel <1:3>

LG_Preamp_25_50, followed by a low noise amplifier with a gain=20 for the HG path
=> Shaper noise negligible

Dynamic range of the 25 Ω preamp tuneable by SC: 5 mA or 10 mA

Cload ADC= 20 pF

Simulations @ τ=15 ns

Ratio HG/LG ≈ 25

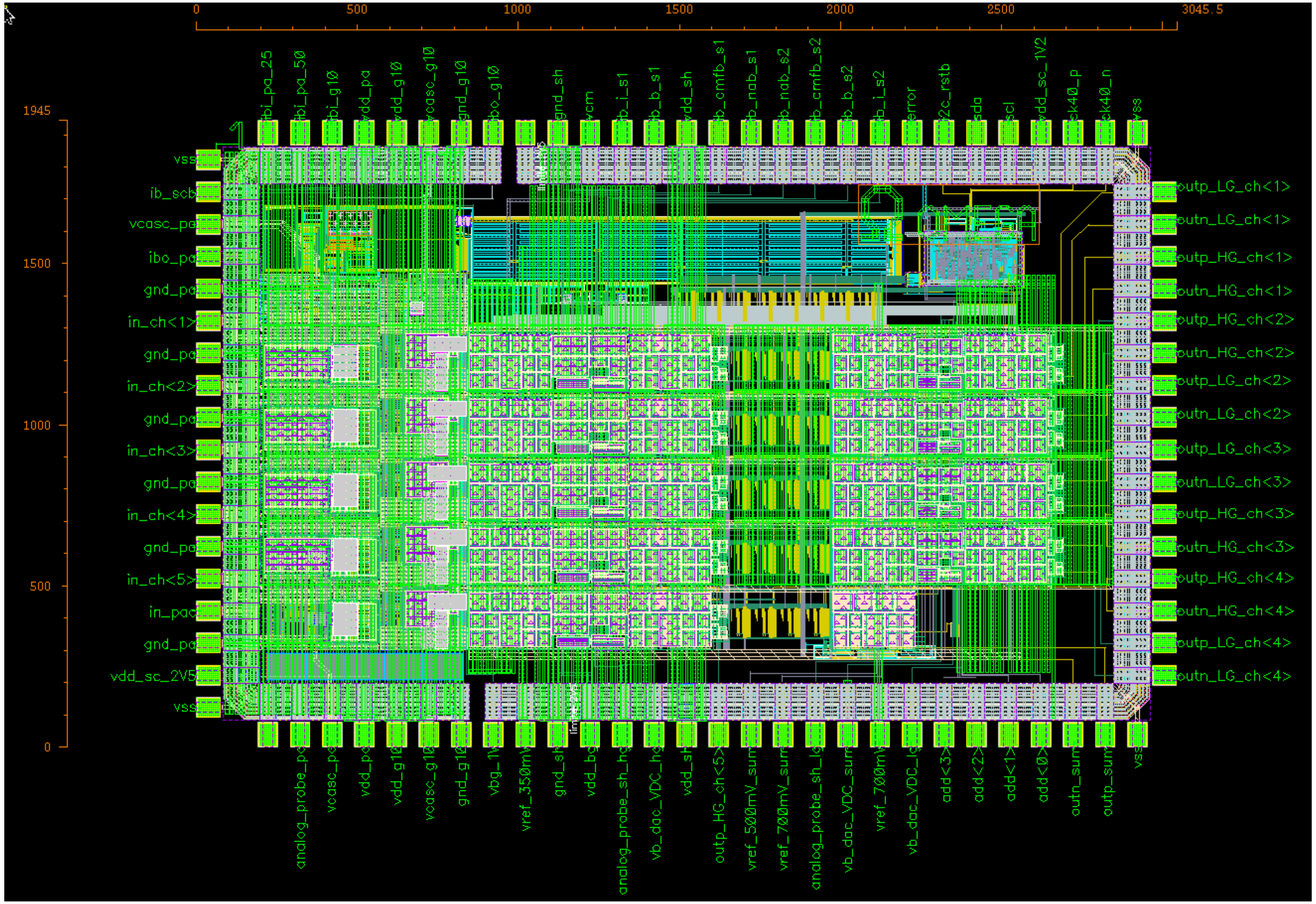
- **LG_preamp 25 Ω with a dynamic range of 5 mA (tuned by SC), Cd=1.5 nF**
  - HG path: 250 µA give ± 983 mV, tp= 46.5 ns and **ENI= 167 nA**
  - LG path: 5 mA give ± 988 mV, tp=46 ns

- **LG_preamp 25 Ω with a dynamic range of 10 mA (tuned by SC), Cd=1.5 nF**
  - HG path: 500 µA give ± 930 mV, tp= 46 ns and **ENI= 220 nA**
  - LG path: 10 mA give ± 920 mV, tp= 46 ns

- **LG_preamp 50 Ω with a dynamic range of 2 mA, Cd=400 pF**
  - HG path: 75 µA give ± 945 mV, tp= 48 ns and **ENI= 53 nA**
  - LG path: 2 mA give ± 923 mV , tp= 46 ns

LAUROC2 LAYOUT (July 8): 3 mm x 2 mm

2 power domains well separated : vdd_pa= 2.5V (total= 100 mA) and vdd_sh= 1.2V (total=125 mA)

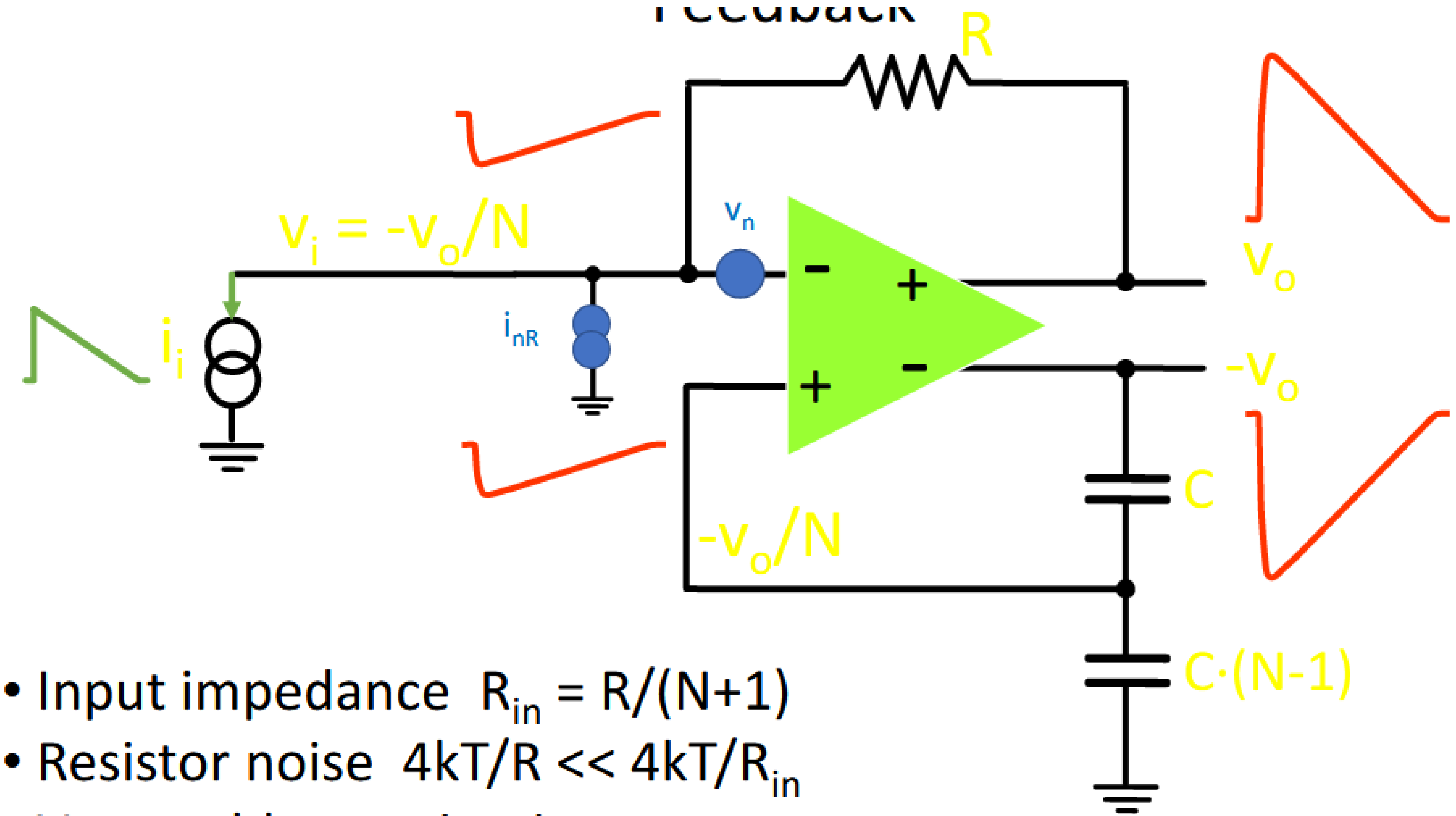


QFN or QFP 128 pins

Same pinout for HEC, ALFE and LAUROC ASICs

Pad ring of Lauroc avalable on LARg SOS server

Final ASIC: should be in BGA package



- Input impedance $R_{in} = R/(N+1)$
- Resistor noise $4kT/R << 4kT/R_{in}$
- Very stable termination (R, N indep. of signal current and active components)
- Fully-differential output