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Performance of LAUROC1, ATLAS Liquid Argon Upgrade ReadOut Chip

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The analog front-end readout electronics of the ATLAS Liquid Argon (LAr) Calorimeter will be replaced by a single chip as part of the upgrades for the High-Luminosity Large Hadron Collider (HL-LHC) program. The cornerstone of the circuit is the very demanding preamplifier, which must have low noise (0.4 nV/√Hz), large dynamic range (up to 10 mA, 16 bits) and precise input impedance (25 or 50 Ohms) to terminate the cables from the detector. LAUROC1 is a prototype that integrates an innovative electronically cooled resistor architecture to fulfil these requirements.

The design of the ASIC and testbench measurements will be presented.

Summary

The readout electronics of the ATLAS LAr Calorimeter must be upgraded for the HL-LHC phase, due to ageing, and to cope with the demanding radiation tolerance and trigger requirements coming from the very high event rates. The increased integrated luminosity also necessitates a larger dynamic range for the readout chain.

LAUROC1 is an ASIC designed in CMOS 130 nm that integrates four analog front-end channels. Each channel consists of a preamplifier followed by a High-Gain (HG) and a Low-Gain (LG) CRRC2 fully differential shaper. The two-gain shaper accommodates the large dynamic range of the LAr signals to the external 14-bit ADC. Their bipolar waveform optimizes the signal to noise ratio in the presence of the anticipated pileup and acts as anti-aliasing for the following 14 bits 40 MHz ADC.

The cornerstone of the analog Front-End is the preamplifier, which is current sensitive due to the long signal duration (600 ns) of the liquid argon pulse. The input impedance has to be precisely matched to the cable impedance bringing the signals out of the cryostat (25 and 50 Ohm). As always in calorimetry, the dynamic range is very large, with detector current reaching up to 10 mA, and the detector capacitance ranges from 400 pF to 2.2 nF. The dynamic range is split in two 14 bits ranges, with a gain ratio of 20 and a linearity better than 0.3 % on both ranges. The most stringent requirement is actually the very low noise, where the Equivalent Noise Current (ENI) must be smaller than 200 nA for a detector capacitance of 1.5 nF and a central frequency of around 10 MHz. This corresponds to a noise spectral density of 0.4 nV/√Hz, equivalent to a 10 Ohm resistor, hence the denomination of "electronically cooled resistor".

The ASIC incorporates 4 channels with tunable input impedance from 15 to 70 Ohms, with an accuracy of 1 Ohm. The maximum input current is also selectable, from 2 mA to 10 mA, depending on the detector sampling depth. The peaking time is adjustable by slow control, from 30 to 60 ns.

LAUROC1 was received in February 2019. While the linearity measurements over the whole dynamic range for both 25 and 50 Ohm configurations as well as input impedance tunings give good results, the measured noise is larger than simulations by 20% due to extra 1/f noise. As the input transistor has been measured separately with good 1/f performance, the extra noise seems to be due to the dielectric noise of the MIM capacitors, where a tan delta of 1E-3, compatible with data in literature, can explain the discrepancy. This noise source is rarely encountered and highlights the low noise levels reached.

LAUROC1 extensive performance obtained on test bench will be detailed in this presentation.

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