The analog readout channel for the Si(Li) tracker of the GAPS experiment

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Outline

- Motivations
- The GAPS experiment
- The Front-End electronics for the GAPS tracker
- Design architecture choices
- Experimental setup and measurements
- Conclusions

General AntiParticle Spectrometer

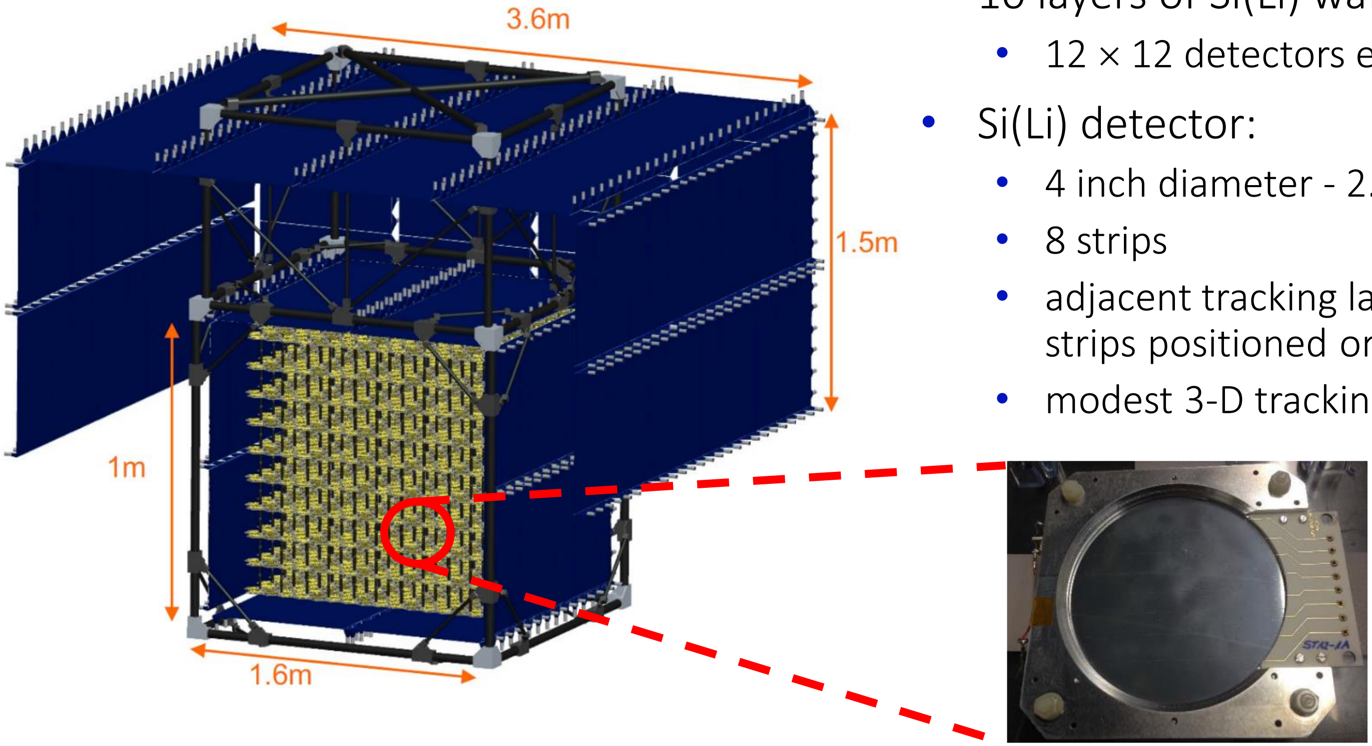
- Two towering problems of early 21st century physics:
  - Dark Matter (DM)
  - Dark Energy (DE)
- Dark Matter is the 85% of matter in the known universe

- Balloon experiments under development will have the potential to detect antideuterons, which may be produced in CDM annihilations
- GAPS: experiment aiming to detect low energy antideuterons (<3GeV/n) produced in the annihilation of CDM particles in the Galactic halo
- Prototype flight (pGAPS) in 2012 @ Taiki, JAXA balloon facility in Japan
- Balloon flight from McMurdo station Antarctica in 2021 (launch approved by NASA)
- The project is funded by NASA, JAXA, INFN, ASI

The Instrument

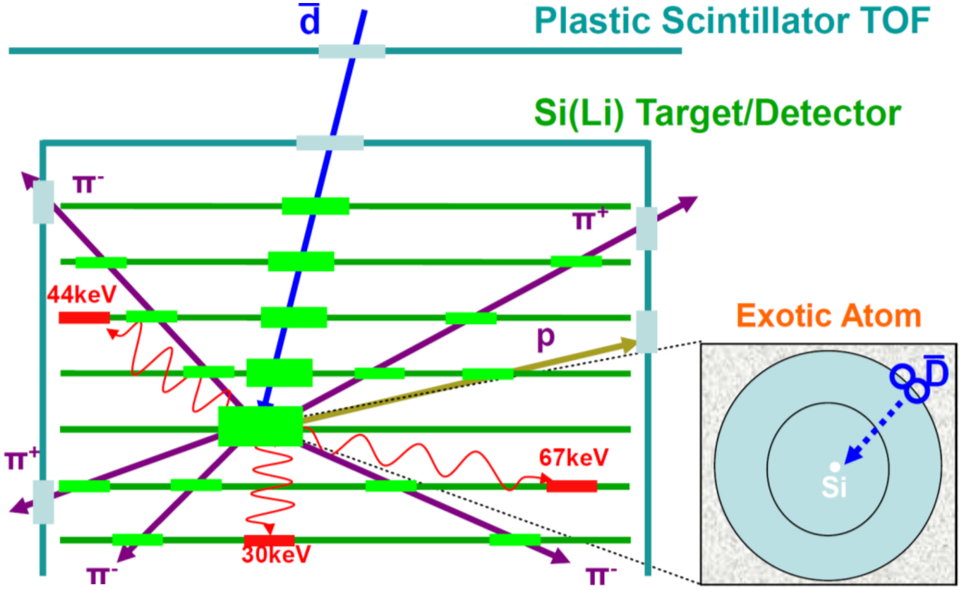
- GAPS relies on 3 techniques to uniquely identify antideuterons:
  - depth sensing and dE/dx loss
  - simultaneous detection of X-rays
  - multiplicity of pions, protons and other particles emitted from the nuclear annihilation

- 10 layers of Si(Li) wafers:
  - 12 × 12 detectors each
- Si(Li) detector:
  - 4 inch diameter - 2.5 mm thick
  - 8 strips
  - adjacent tracking layers have their strips positioned orthogonally
  - modest 3-D tracking



Antiparticle identification with GAPS

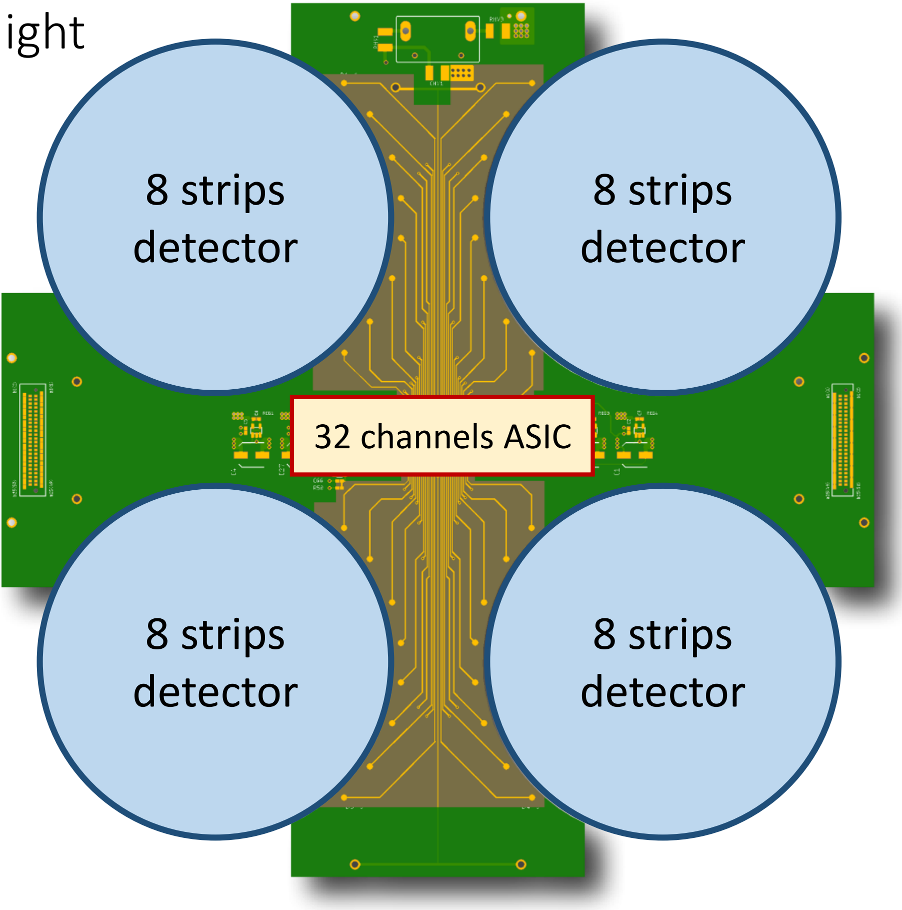
- Time-Of-Flight system measures velocity of the incoming particle (trigger)
- Loses energy in layers of semiconducting Silicon targets/detectors
- Stops, forming exotic excited atom
- Atom de-excites, emitting X-rays
- Remaining nucleus annihilates, emitting pions and protons



- Expected Energy range: 10 keV – 100 MeV
- Required energy resolution in low energy range 4 keV
- Operating temperature -40°C → low power consumption needed

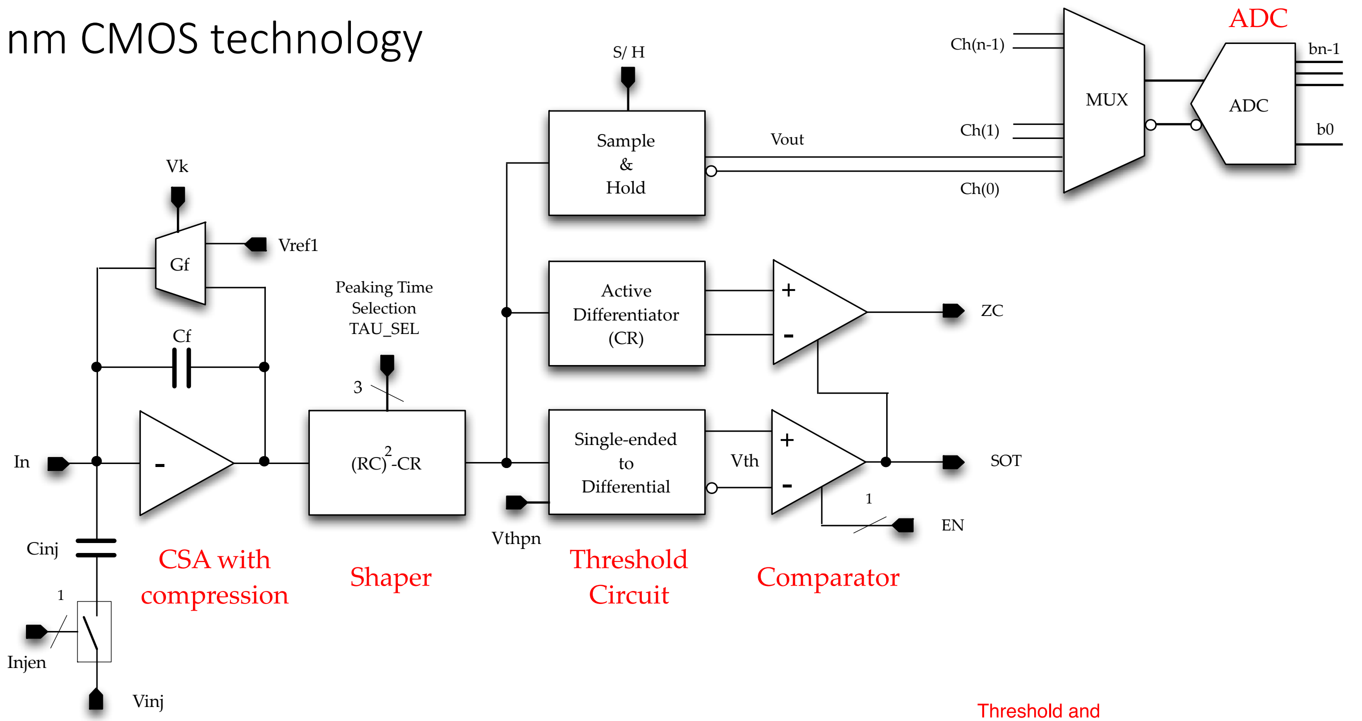
Main requirements for the front-end electronics

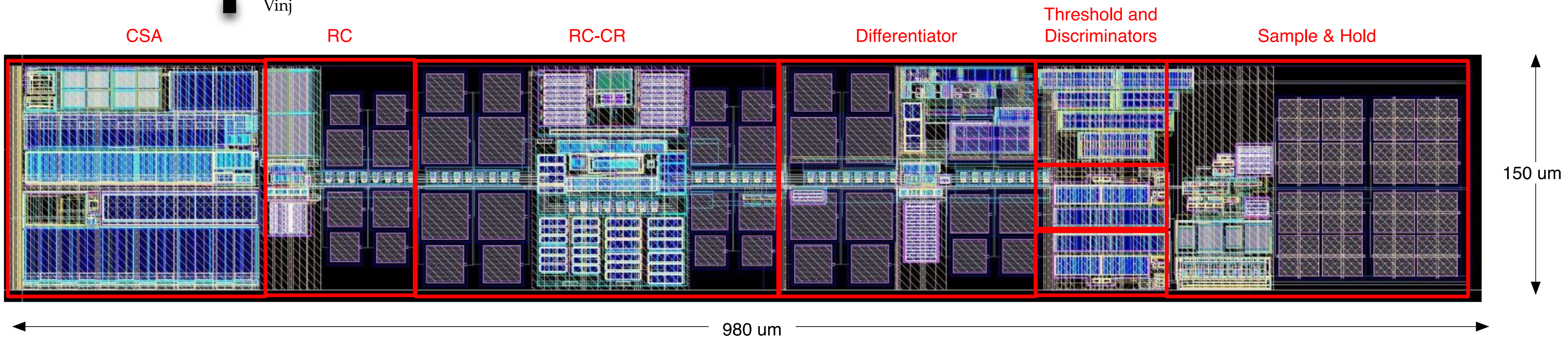
- pGAPS used a discrete amplifier for detector readout
- **Goal:** ASIC design for the final 2021 flight
- Modular structure:
  - 4 sensors per module
  - 1 ASIC per module
  - Channels per ASIC: 32
  - Operating temperature: -40 °C
  - Power dissipation: <10 mW/channel
  - Signal polarity: electrons
  - Dynamic range: 10 keV-100 MeV
  - Analog Resolution: 4 keV (FWHM)
  - Threshold: 10 keV
  - Detector leakage current: 5-10 nA (50 nA for tests at higher temperature)



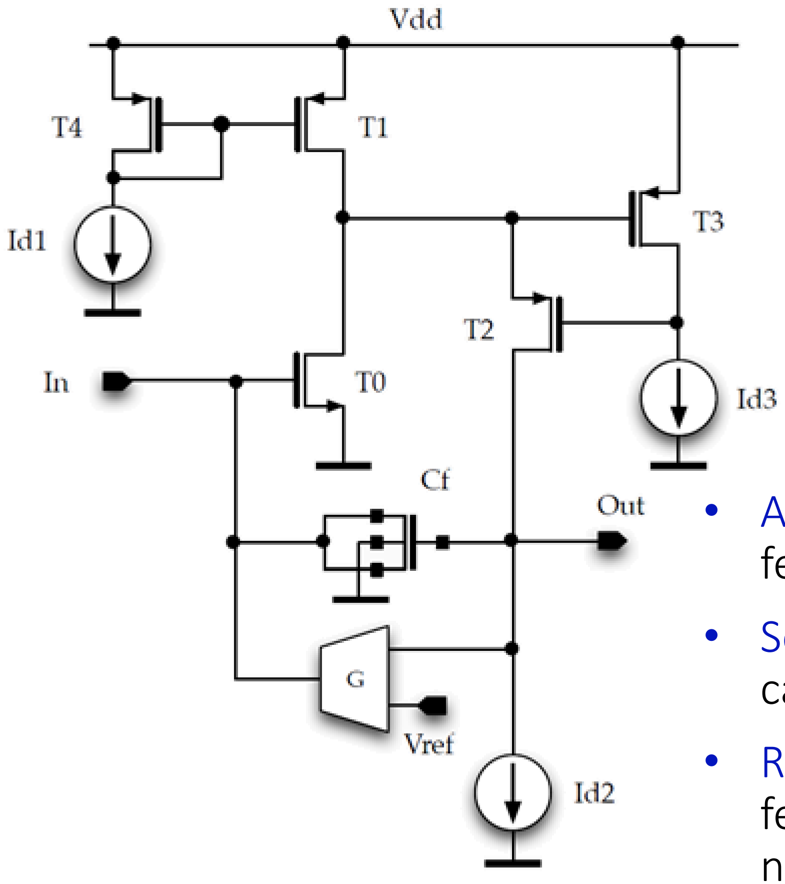
Analog readout channel

- 180 nm CMOS technology





Charge Sensitive Amplifier

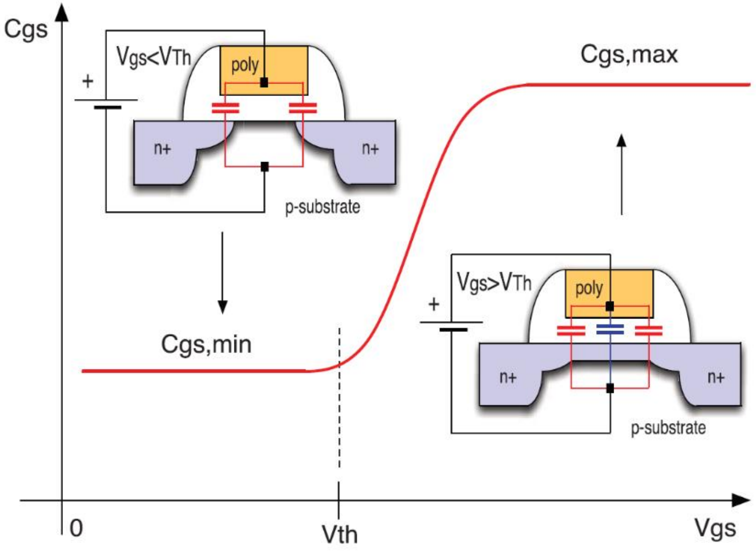


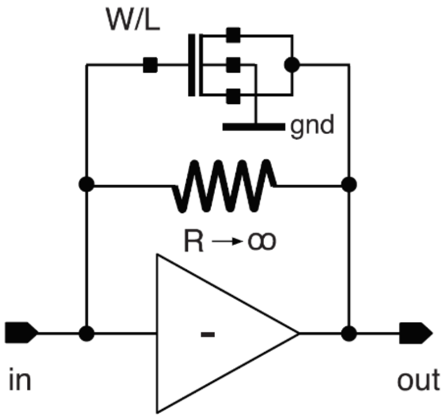
Main design features	
Bias Voltage	1.8 V
Input device W/L	2000/0.5
Input Device Drain Current	1.6 mA
Power Consumption	4.5 mW
Feedback device	240/60

- Architecture: active folded cascode (with local feedback) loaded by an active cascoded load
- Sensitivity: dynamic compression with MOS capacitor
- Reset: performed by a continuous time feedback implemented with a Krummenacher network

Dynamic Signal Compression

- It is based on the nonlinear behavior of a MOSFET capacitor operating in the inversion mode
- Suitable choice of W and L to set the gain in the low and high energy regime





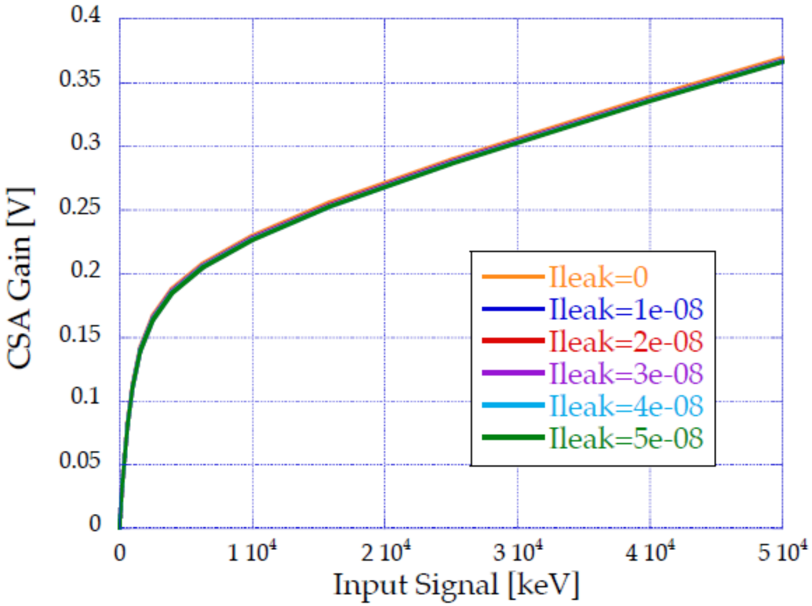
$$\begin{cases} C_{gs,min} \approx C_{ov} = \varepsilon \dfrac{2W\Delta L}{t_{ox}}, & V_{gs} < V_{th} \\ C_{gs,max} = \varepsilon \dfrac{WL}{t_{ox}}, & V_{gs} > V_{th} \end{cases}$$

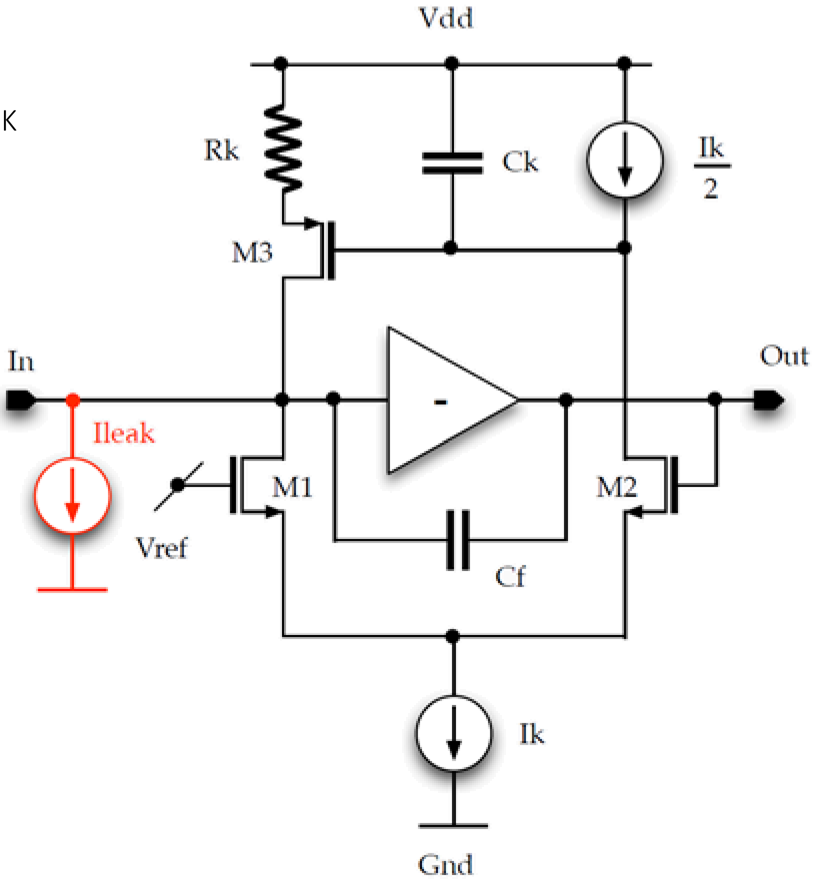
$$Gain \propto \frac{1}{C_f}$$

(*) M. Manghisoni et al., ”Dynamic compression of the signal in a charge sensitive amplifier: from concept to design”, IEEE TNS

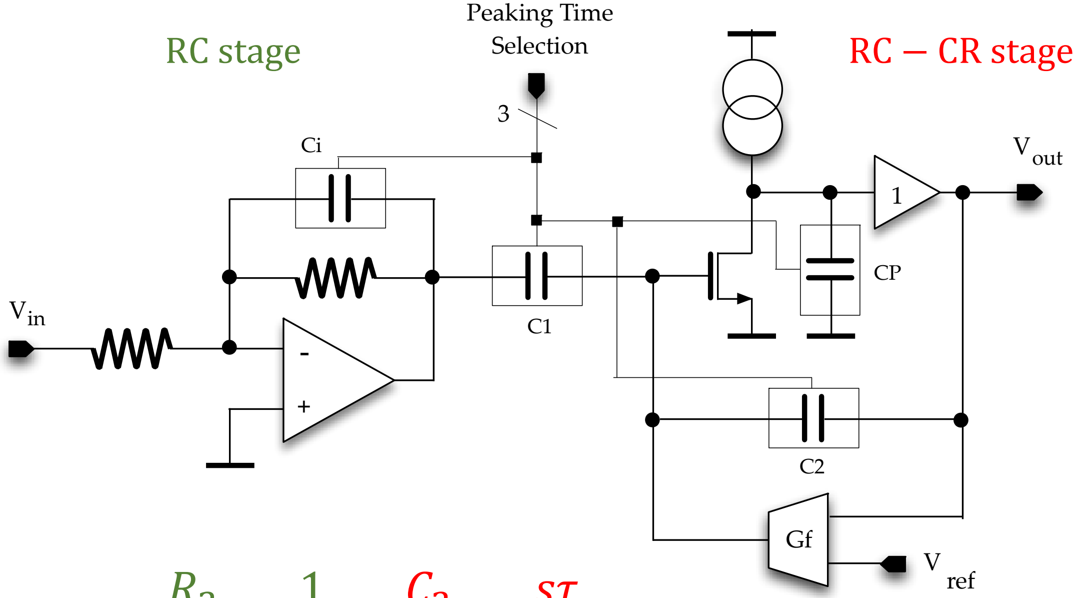
Improved charge restoration network

- Krummenacher network to comply with the high detector leakage current
  - I_{leak} = 5-10 nA (detection at T= -40°C)
  - I_{leak} = 50 nA (test at higher T)
- Additional degeneration resistance R_K





Time invariant filter



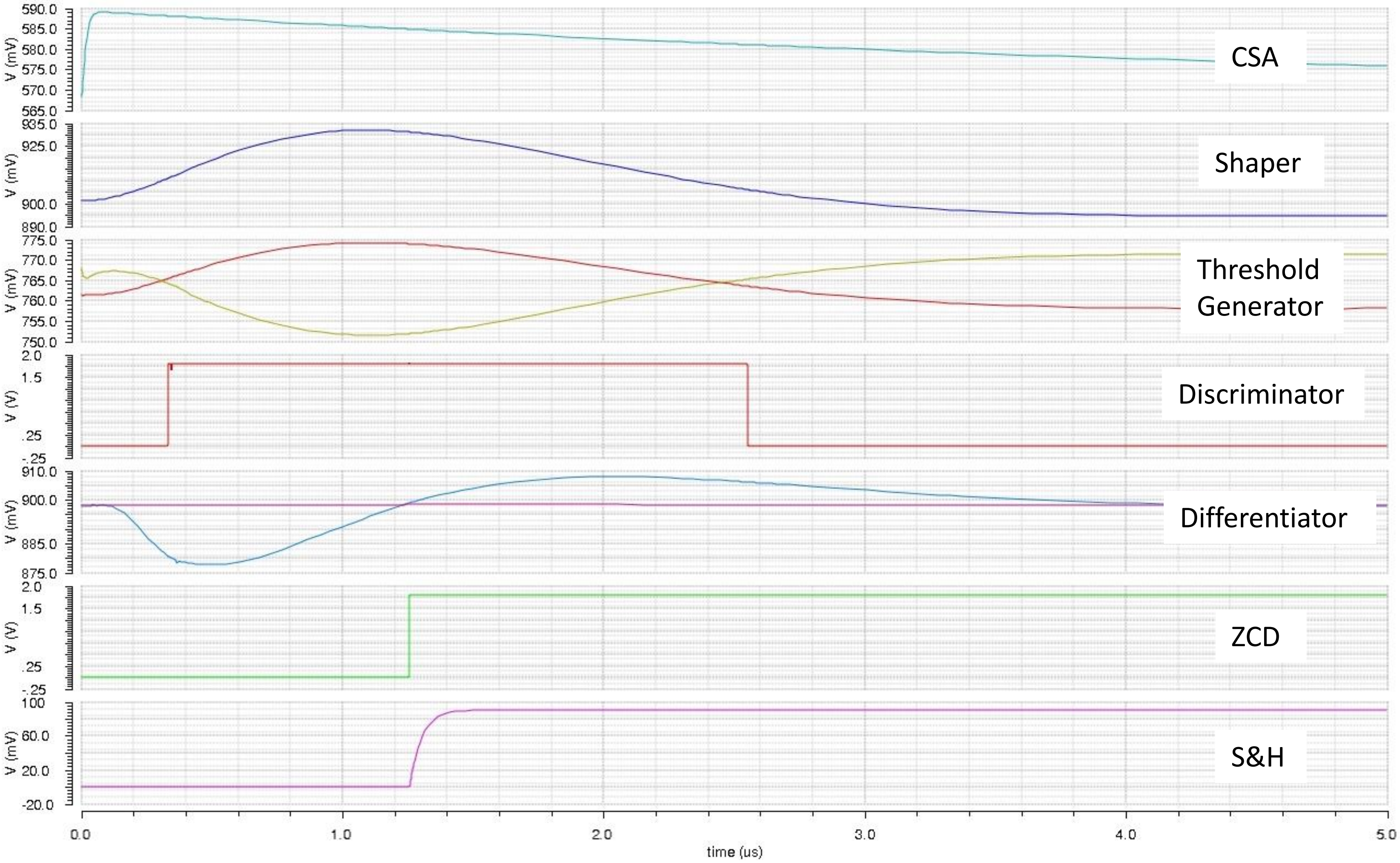
#	Peaking Time (µs)
000	0.30
001	0.50
010	0.65
011	0.85
100	1.00
101	1.30
110	1.50
111	1.80

$$H(s) = \frac{R_2}{R_1}\frac{1}{(1+s\tau)}\frac{C_2}{C_1}\frac{s\tau}{(1+s\tau)^2}$$

- Unipolar semi-Gaussian ($\mathrm{RC}^2 - \mathrm{CR}$) shaping function $t_p = 2\tau$
- Peking time selection (3 bit): obtained by switching capacitances C_1, C_2, C_p and C_i in order to keep constant the ratios:

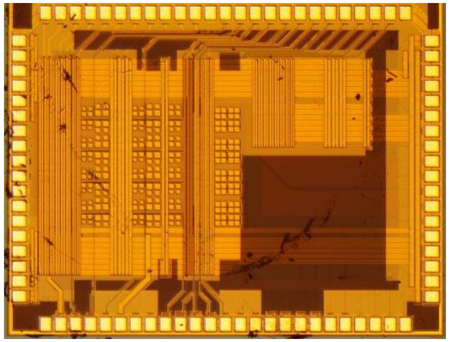
$$\frac{C_2}{C_1} \quad \text{and} \quad G_f = \frac{C_2}{t_p}$$

Analog Channel Time Response

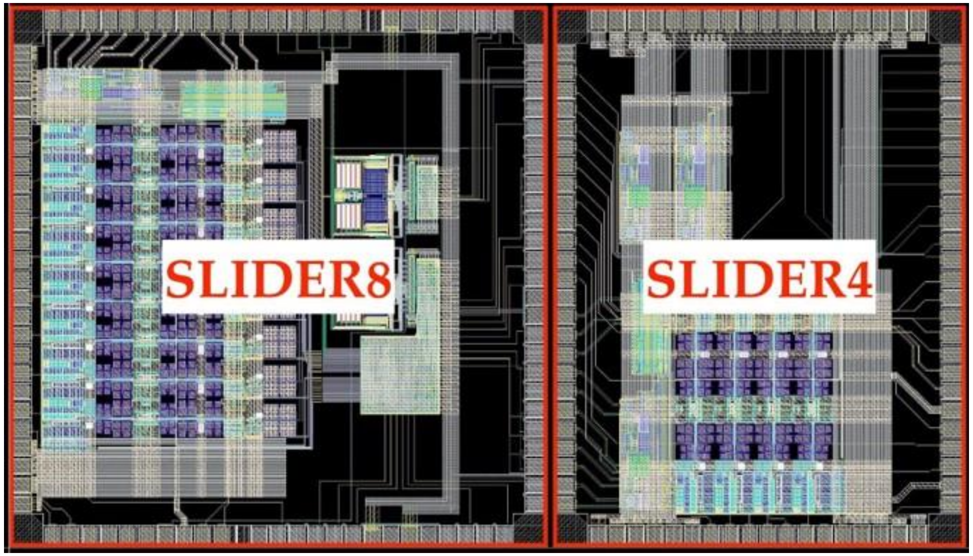


Si(LI) DEtector Readout

- Prototypes for the final 32 channel ASICs
- Submitted and fabricated in late 2018



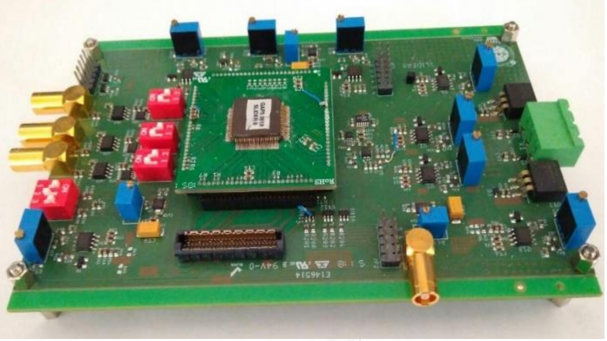
  - SLIDER 4:
    - 4 analog channels
    - No digital backend
    - 2 channels with all analog block output accessible
  - SLIDER 8:
    - 8 analog channels
    - digital backend
    - 11 bit ADC
    - no access to the analog blocks

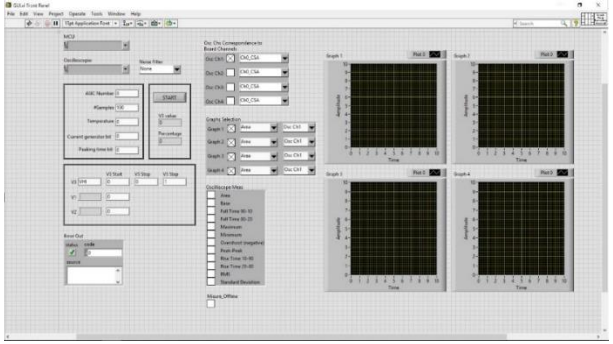


Experimental setup and LabView interface

- Experimental setup
    - Two different motherboard
    - Oscilloscope LeCroy Wavesurfer 454
    - LabView Interface

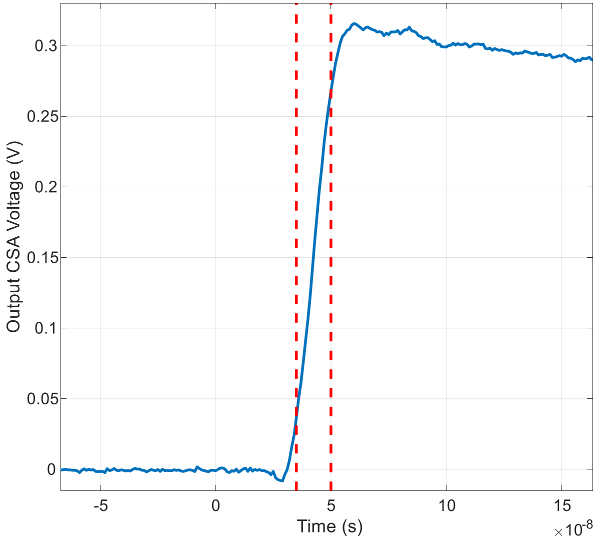
- LabView Interface
    - Slider4 and Slider8 control setup
    - Voltage threshold and calibration setting
    - Oscilloscope measurements setting
    - Automatic measurements with voltage reference sweeps fixing initial, final and step values

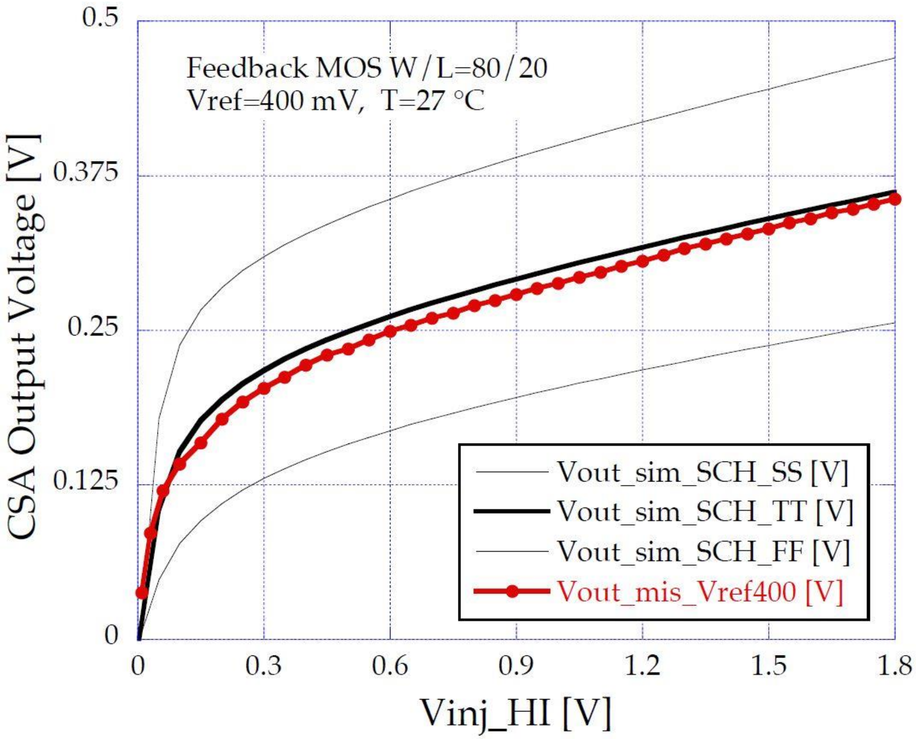




SLIDER4: CSA - Simulation vs Measurements

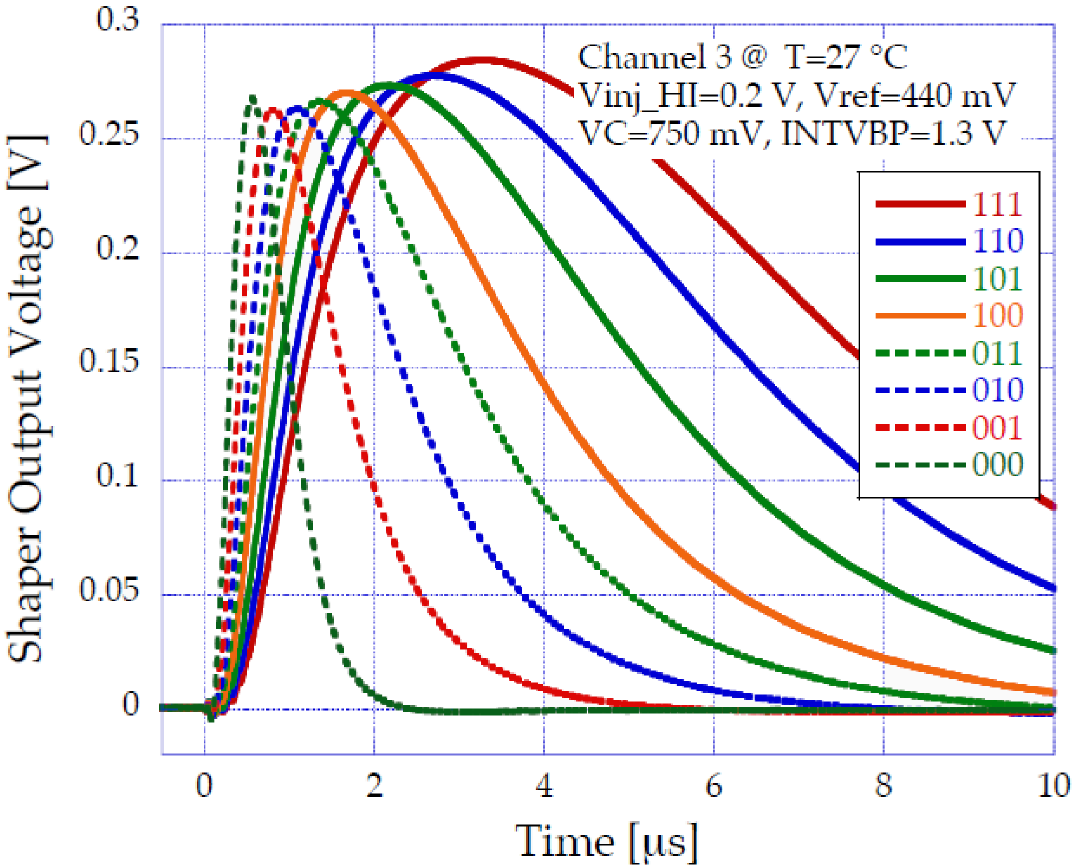
- Charge sensitivity:
  - High gain region: 140 µV/keV ($C_f = 190\ \mathrm{fF}$)
  - Low gain region: 4.5 µV/keV ($C_f = 14.5\ \mathrm{pF}$)
- Dynamic range: the CSA covers the full dynamic range of 100 MeV
- Rise time: $t_r \approx 15\ \mathrm{ns}$
- Very promising correlation between simulation and measurements





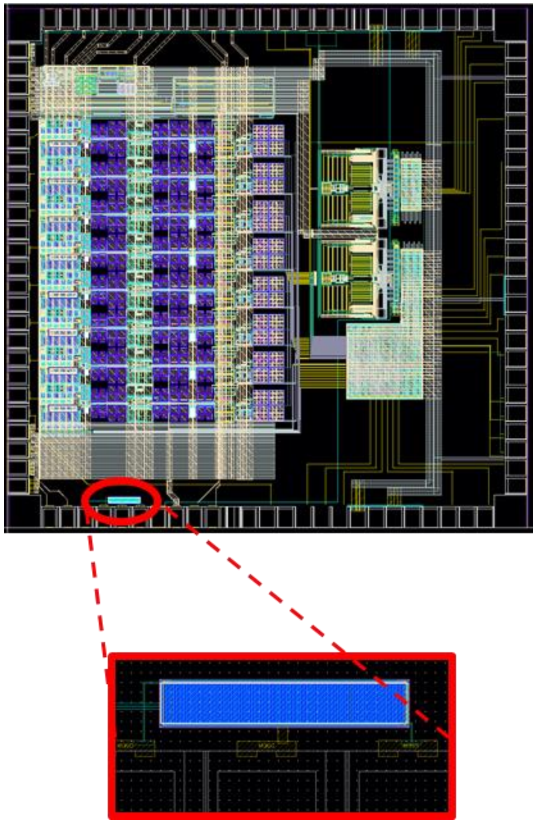
SLIDER4: Shaper Measurements

- Calibration Voltage V_{HI} = 0.2 V
- Amplitude coherent with the selected calibration voltage

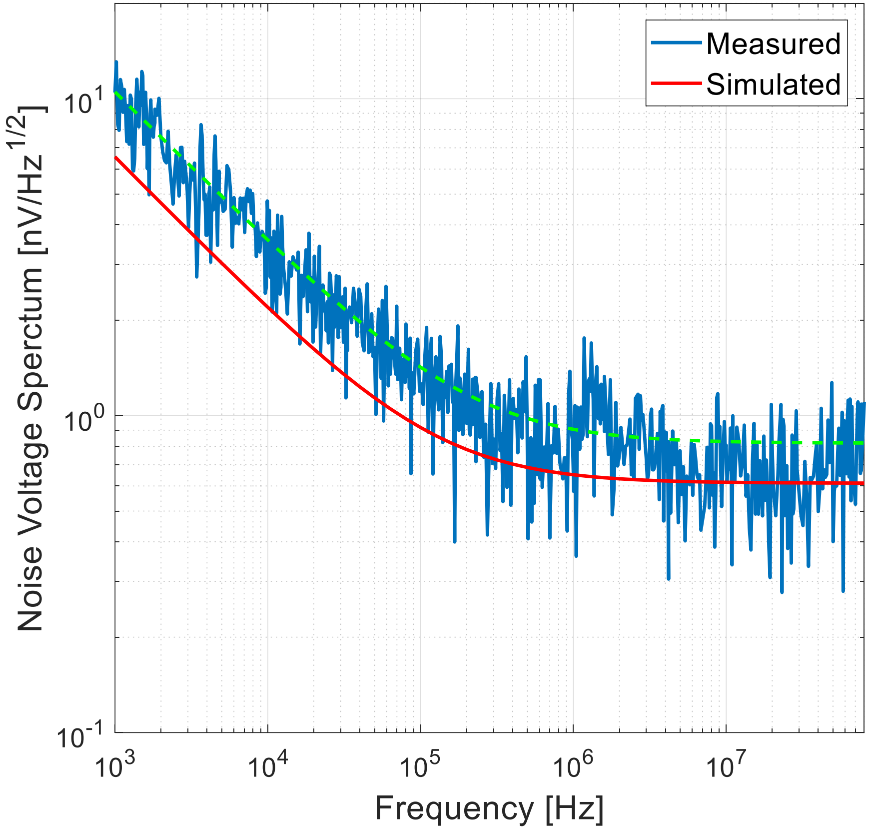


SLIDER8: NMOSFET characterization

- Single device with the same geometry of the CSA input device
- Characterization of the CSA Input device at the expected DC working point:
  - V_{DS} = 1.29 V
  - V_{GS} = 294 mV
  - I_D = 1.62 mA
  - @ 27°C
- Static Measurements:
  - performed by means of a Semiconductor Parameter Analyzer
  - I_D-V_{GS} at fixed V_{DS}
- Noise Voltage Spectrum Measurement:
  - performed by means of a purposely developed wide-band interface circuit, which allows for noise measurements in the 1 kHz-100 MHz range and a Network/Spectrum Impedence Analyzer



SLIDER8: noise voltage spectrum



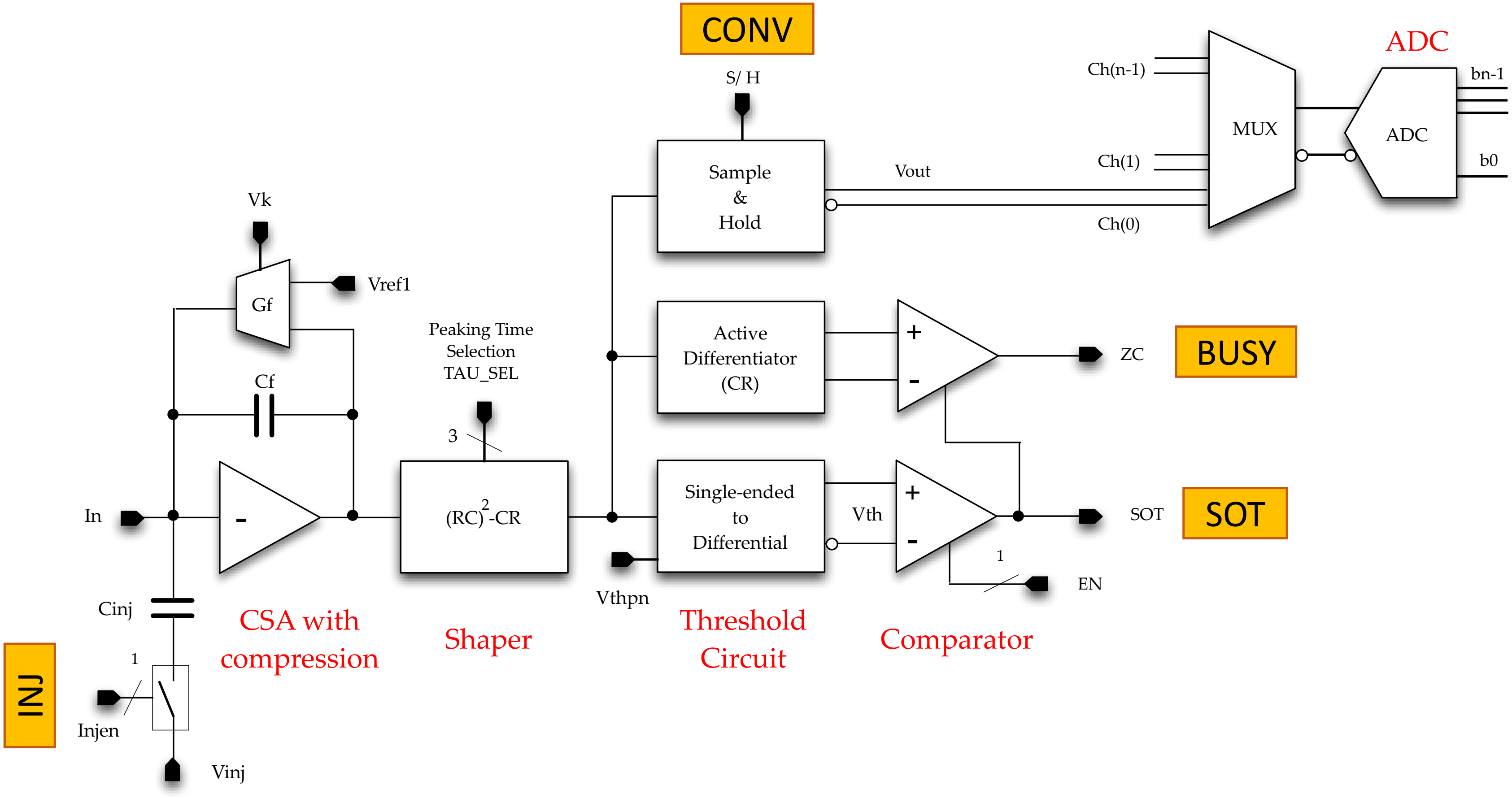
$$Noise\ PSD = A_f \frac{1}{f^{\alpha}} + S_w^2$$

	α	$A_f\ (V^2)$	$S_w \left(\frac{nV}{\sqrt{Hz}}\right)$
Simulation	0.98	$3.7 \cdot 10^{-14}$	0.62
Measurement	0.95	$8.0 \cdot 10^{-14}$	0.73

$$S_w^2 = 4k_B T \frac{\Gamma}{g_m}$$

- $\Gamma = 0.96$ with measured $g_m = 30.5\ mS$

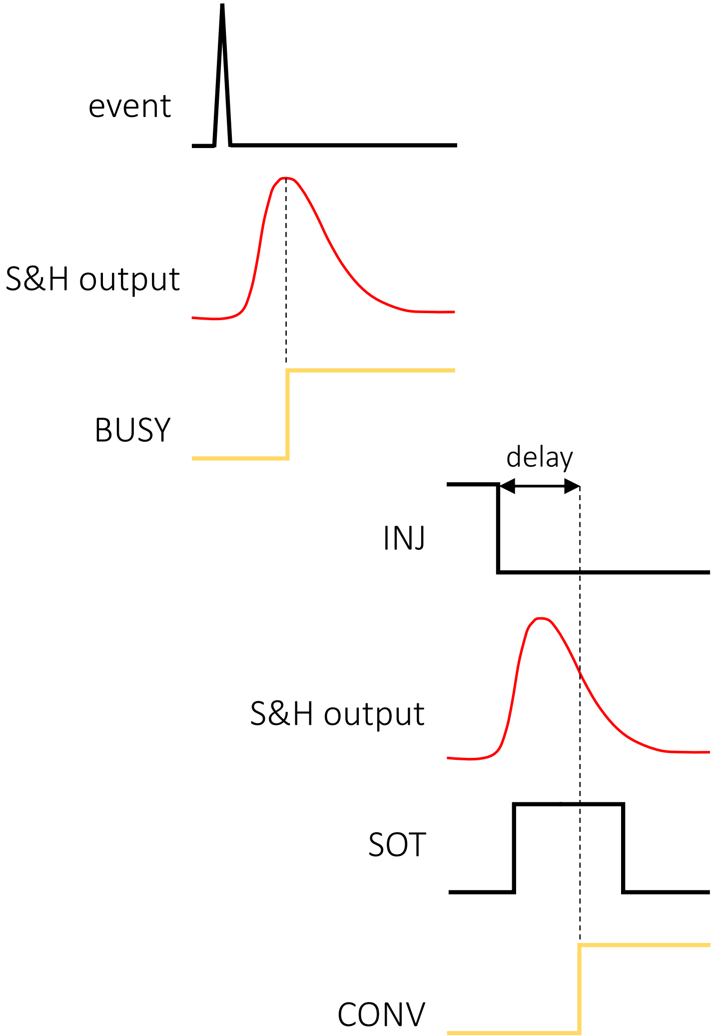
SLIDER8: Channel



SLIDER8: Data acquisition

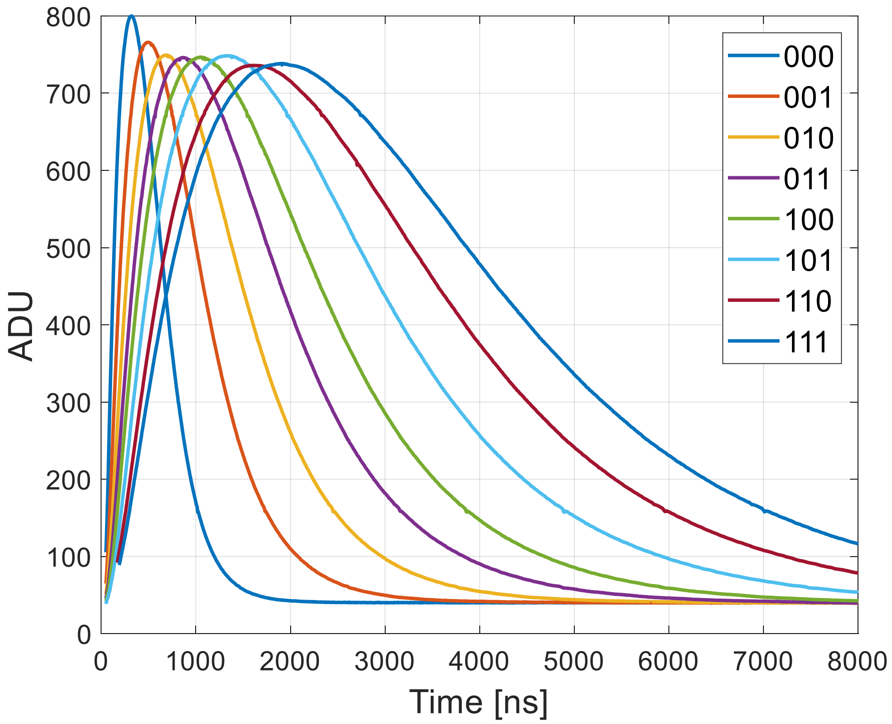
The ASIC can operate in two modes:

- Self-trigger mode (calibration):
  - if an event/injection occurs
  - ZCD (busy signal) triggers the readout of the Sample&Hold
- Acquisition mode:
  - if the channel fires (SOT=high)
  - the S&H output is sampled at the CONV signal
- By varying the delay between INJ and CONV signal it is possible to reconstruct the channel time response



SLIDER8: Shaper output

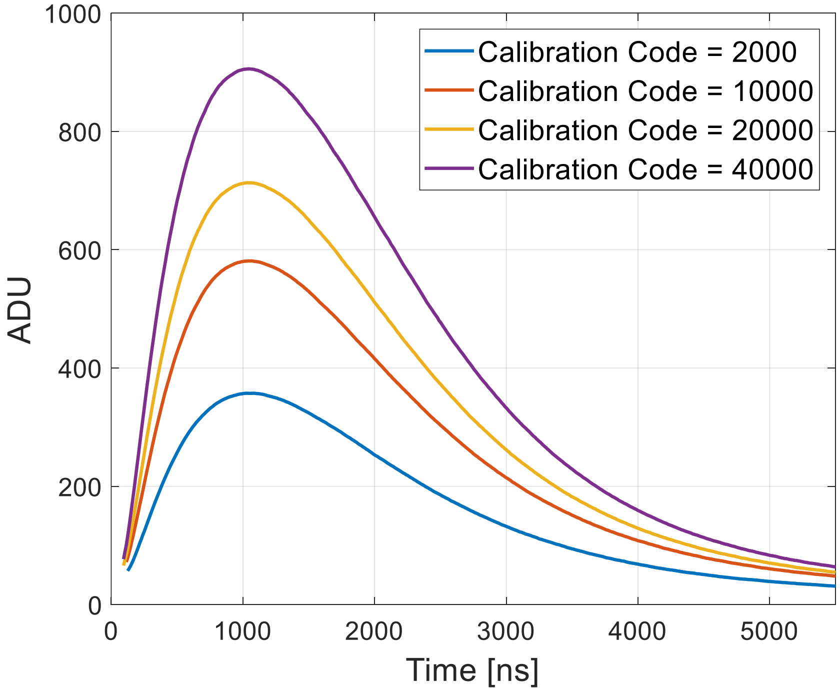
Channel 3 – Calibration Code 20000 DAC (15.6 MeV)

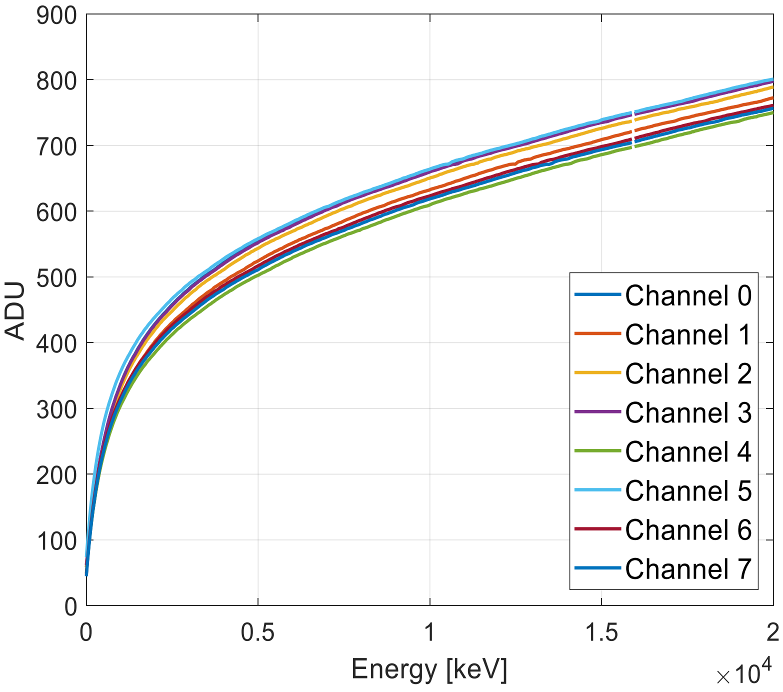


#	τ_p Sim [µs]	τ_p Meas [µs]
1	0.30	0.31
2	0.50	0.50
3	0.65	0.68
4	0.85	0.85
5	1.00	1.02
6	1.30	1.26
7	1.50	1.49
8	1.80	1.73

- Good agreement between simulated and measured peaking times
- Amplitude decreases with t_p due to the zero in the CSA feedback network

SLIDER8: Channel transfer function


Channel 0 – Peaking time 011


Peaking time 011

SLIDER8: Threshold scan

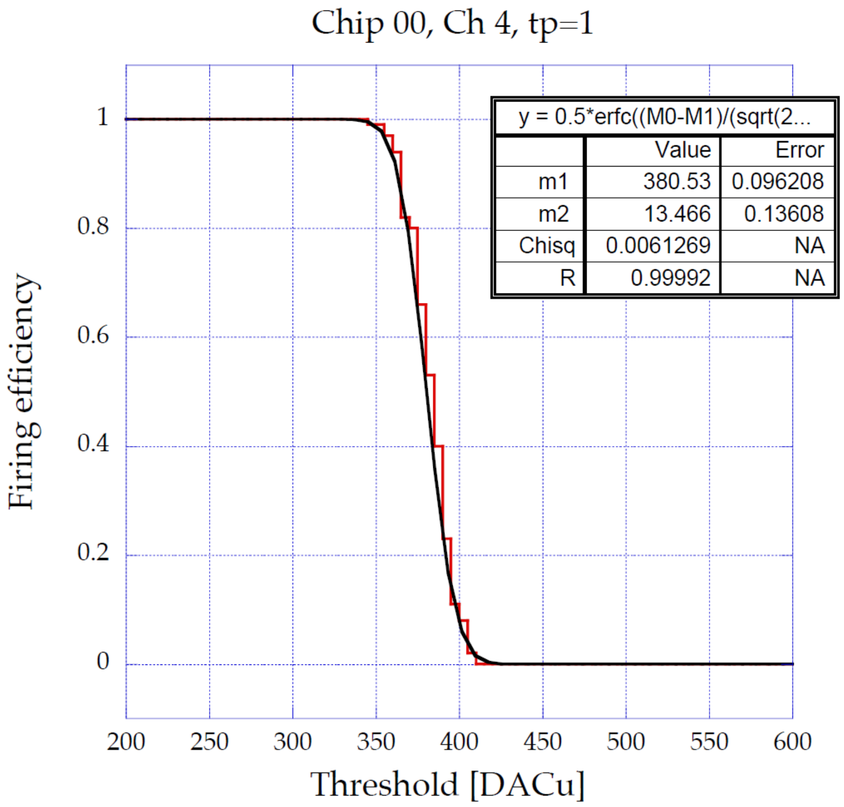
- Interpolating function:

$$F(x) = \frac{1}{2} \cdot \mathrm{erfc}\left(\frac{x - V_{th}}{\sqrt{2}\sigma_q}\right)$$

- where
  - σ_q is the rms value of the shaper output voltage
  - V_{Th} is the offset of the SOT discriminator

- if the charge sensitivity G is known

$$ENC = \frac{\sigma_q}{G}$$



y = 0.5*erfc((M0-M1)/(sqrt(2...

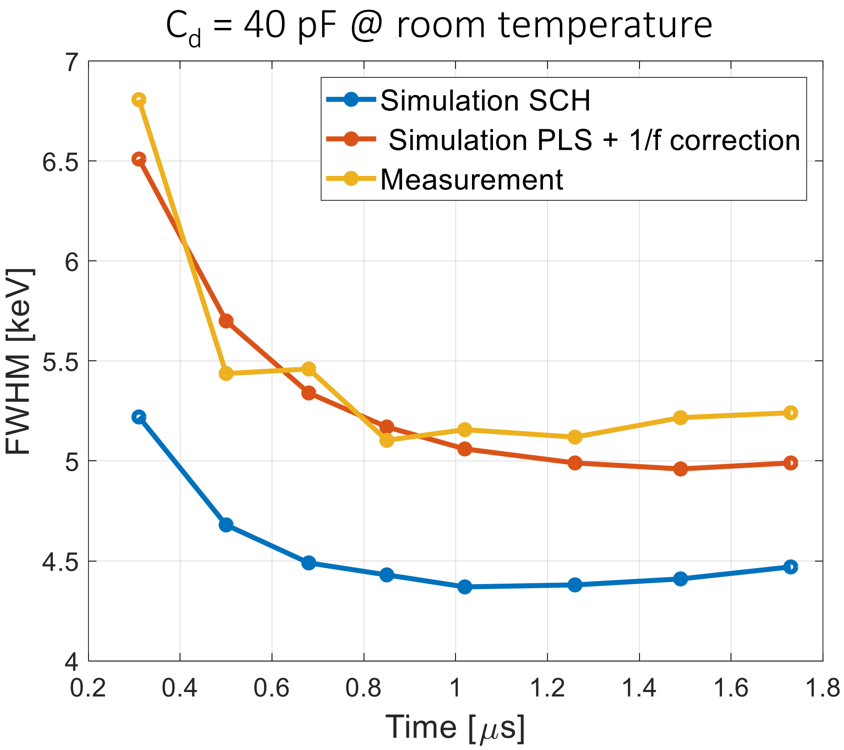
	Value	Error
m1	380.53	0.096208
m2	13.466	0.13608
Chisq	0.0061269	NA
R	0.99992	NA

SLIDER8: FWHM

- Noise at room temperature higher than expected because of:
  - a higher parasitic resistance in series to the CSA input (can be eliminated with a new layout)
  - according to measurement performed on the single MOS device, flicker noise coefficient is larger with respect to model
- Knowing that the Full Width at Half Maximum is:

$$FWHM = 2.35 \cdot \varepsilon \frac{ENC}{q}$$

- Considering the measured A_f coefficient and an higher parasitic resistance, FWHM is in agreement with simulation results
- At peaking times exceeding 0.8µs simulations predict a 30% reduction of the noise going from room temperature down to -40°C
- At 0.8µs and a C_d = 40pF, a 3.6keV FWHM can be expected at the GAPS operating conditions (to be verified with measurements)



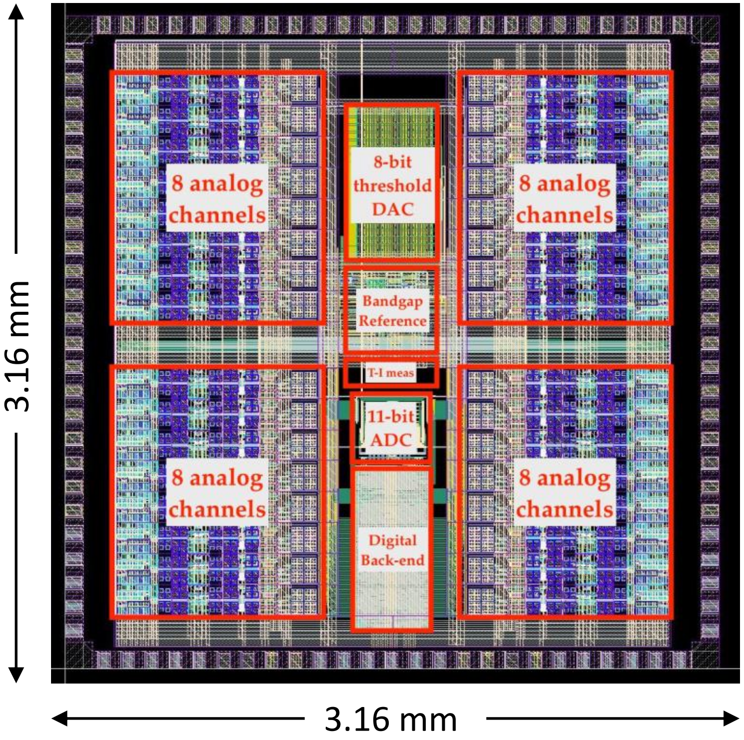
C_d = 40 pF @ room temperature

Conclusions and next steps

- Characterization of the first prototype of SLIDER4 and SLIDER8 ASIC
- Good correlation between simulated data and measurements:
  - CSA output transfer function
  - Shaper behavior @ different peaking times
  - Resolution
- Useful information for the design of pSLIDER32, a prototype with 32 analog channels

Next Steps:

- Test with detector in order to validate Krummenacher performance
- Improving the statistics with more samples
- Defining the most useful tests enabling the differentiation between good and bad ASICs (mass production)



pSLIDER32 submitted in July 2019 expecetd delivery in second half of September

The GAPS collaboration

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agenzia spaziale italiana

INFN

UNIVERSITÀ DI PAVIA

UC San Diego

JAXA

NASA

SLAC NATIONAL ACCELERATOR LABORATORY

MIT

UNIVERSITY OF HAWAI'I

AOYAMA GAKUIN UNIVERSITY

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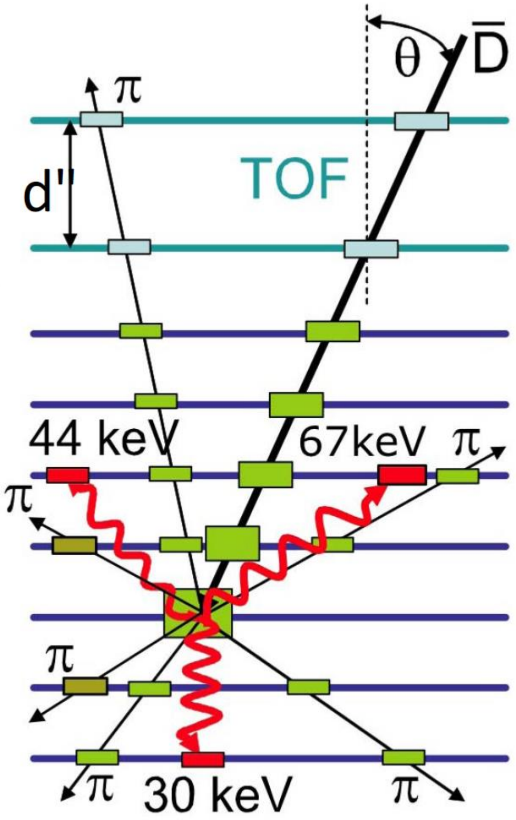
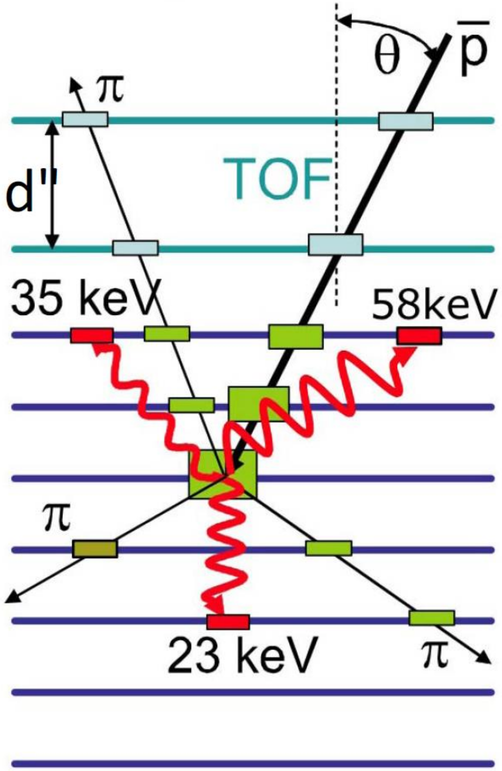
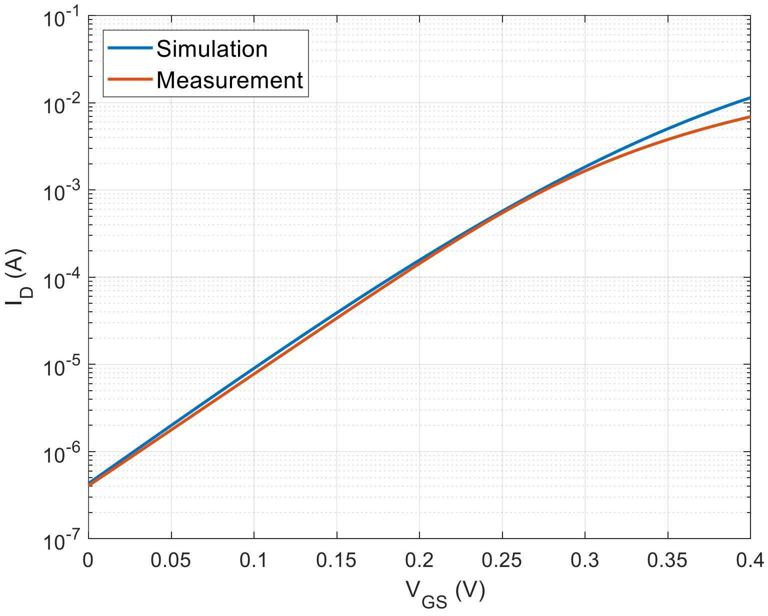
Spare Slides

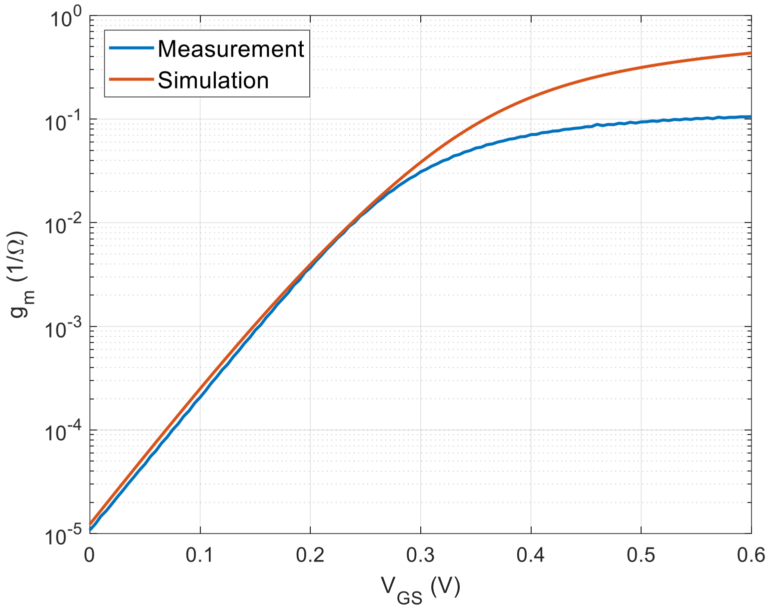
GAPS Background rejection





SLIDER8: drain current and transconductance





- Simulation and measurement show a discrepancy with $\mathrm{V_{GS}} > 300\ \mathrm{mV}$

@ I_D = 1.62 mA	**Simulation**	**Measurement**
g_m	34.5 mS	30.5 mS