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Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration

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A prototype chip named RD50-MPW2 in the 150 nm High-Voltage CMOS (HV-CMOS) technology from LFoundry has been designed and submitted for fabrication within the CERN-RD50 collaboration. The chip contains a matrix of depleted CMOS pixels with monolithically integrated readout electronics. The focuses of the chip are on improving the readout speed that is achieved by designing high-speed, low-noise readout electronics, and minimising the leakage current and increasing the breakdown voltage of the sensor by optimising the chip layout. The design and initial measured results of RD50-MPW2 will be presented in this contribution.

Summary

The industry standard High-Voltage CMOS (HV-CMOS) technology is a promising candidate for future particle physics experiments that require sensors with small pixel size, good timing resolution, excellent radiation tolerance and low material budget, such as the Mu3e experiment, future upgrades of the Large Hadron Collider (LHC) and the Circular Electron Positron Collider (C EPC).

As opposed to traditional hybrid silicon sensors that require bump-bonding to assemble the sensing element and the readout chip together, depleted CMOS sensors allow integrating all parts onto one single piece of silicon, thus making this technology efficient in material, production time and cost. A high voltage used to bias the sensor substrate brings the benefits of fast charge collection by drift and high radiation tolerance up to a few 1015 1 MeV neq/cm2.

The CERN-RD50 collaboration is developing depleted CMOS sensors to further improve their performance to meet the requirements of future particle physics experiments. In this work, we present the design of a new prototype chip in the 150 nm HV-CMOS technology from LFoundry, named RD50-MPW2. The chip contains a matrix of pixels with monolithically integrated readout electronics. The focuses of the chip are on improving the readout speed, minimising the leakage current and increasing the breakdown voltage of the sensor, which are achieved by designing high-speed, low-noise readout electronics and optimised chip layout. The RD50-MPW2 also acts as a necessary step for developing a large demonstrator of depleted CMOS sensors that is foreseen within CERN-RD50.

The depleted CMOS matrix includes two flavours of 60 um x 60 um pixels that use different methods to reset the sensing diode. These methods are named the continuous-reset and the switched-reset. Pixels with continuous-reset use a continuous current to reset the Charge Sensitive Amplifier (CSA) after a particle hit, resulting in a processing time (rise plus fall time) that is proportional to the number of electrons collected by the sensor. With this pixel flavour, it is possible to process a particle hit that generates 10k electrons within 90 ns only. Pixels with switched-reset use the output of the discriminator to switch on and off a larger reset current. The switched current resets the CSA in 15 ns and shortens the processing time to 45 ns, independently of the number of collected electrons. As the larger reset current is active for a very short time only, the power consumption is kept low.

The continuous-reset pixel is able to provide both rising and trailing edge time-stamps to obtain the Time over Threshold (ToT). In contrast, the switched-reset pixel can only provide the time of arrival. Post-layout

simulations show that both pixel flavours have time resolution better than 15 ns, Equivalent Noise Charge (ENC) around 100 e- and pixel power consumption less than 25 μW.

RD50-MPW2 has been submitted for manufacture and the fabricated dies that will be in 10, 100, 1.9k and 3k Ωcm resistivity substrates are expected in July 2019. The design and initial measured results of the chip will be presented in this contribution.

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