Electronics readout for the CGEM - Inner Tracker: TIGER ASIC and electronics chain

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on behalf of the BESIII Italian Collaboration

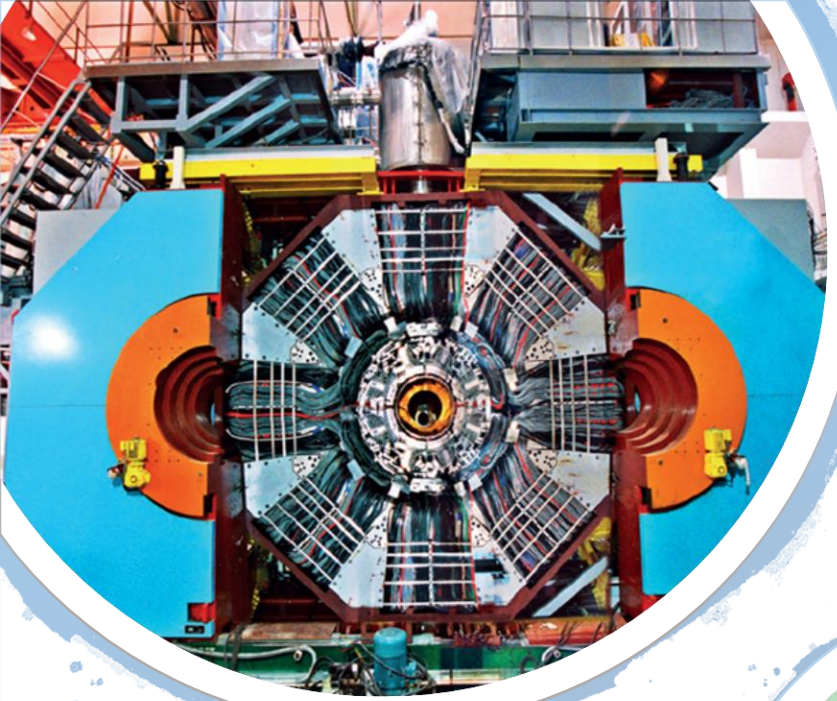
UNIVERSITÀ DEGLI STUDI DI TORINO

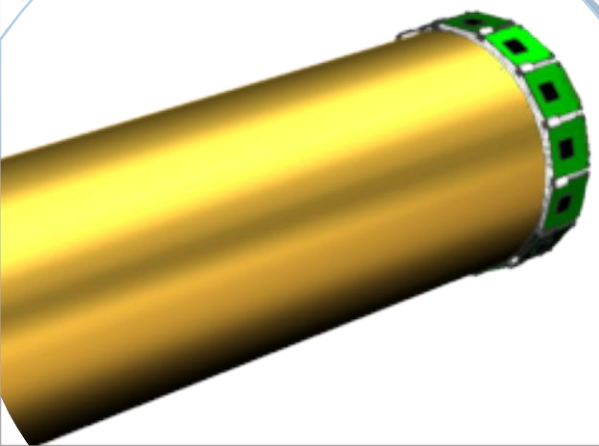
BESIII

INFN
Istituto Nazionale di Fisica Nucleare

Outline

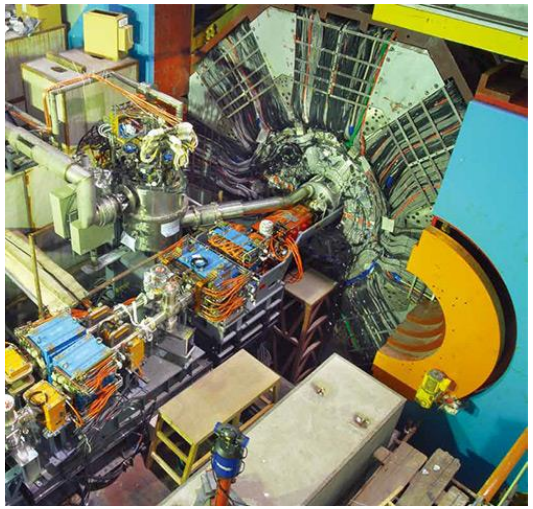
- BESIII and CGEM-IT
- TIGER ASIC
  - Design
  - On silicon characterization
- Off detector electronics
- Detector integration





Introduction:
BESIII and CGEM-IT

BESIII Experiment

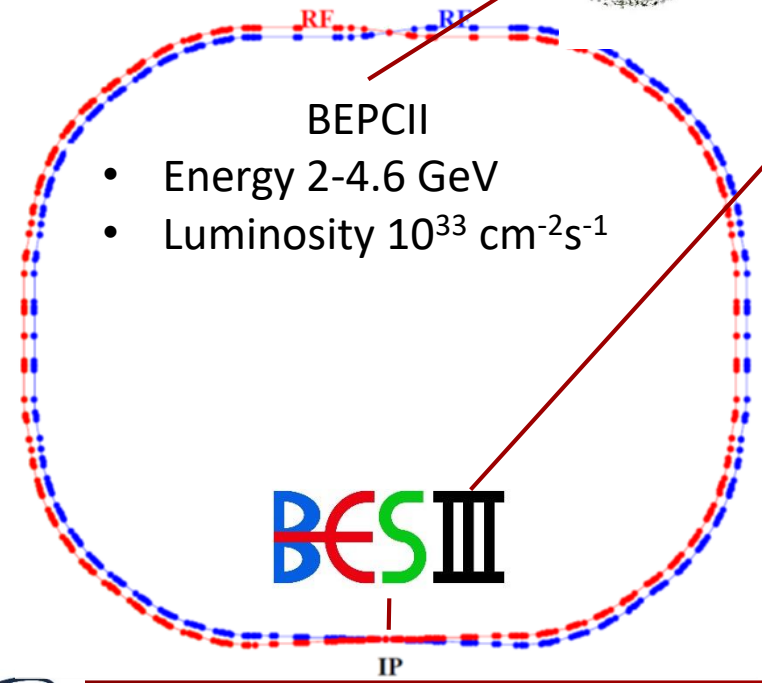


BESIII spectrometer

BESIII main scientific objectives:

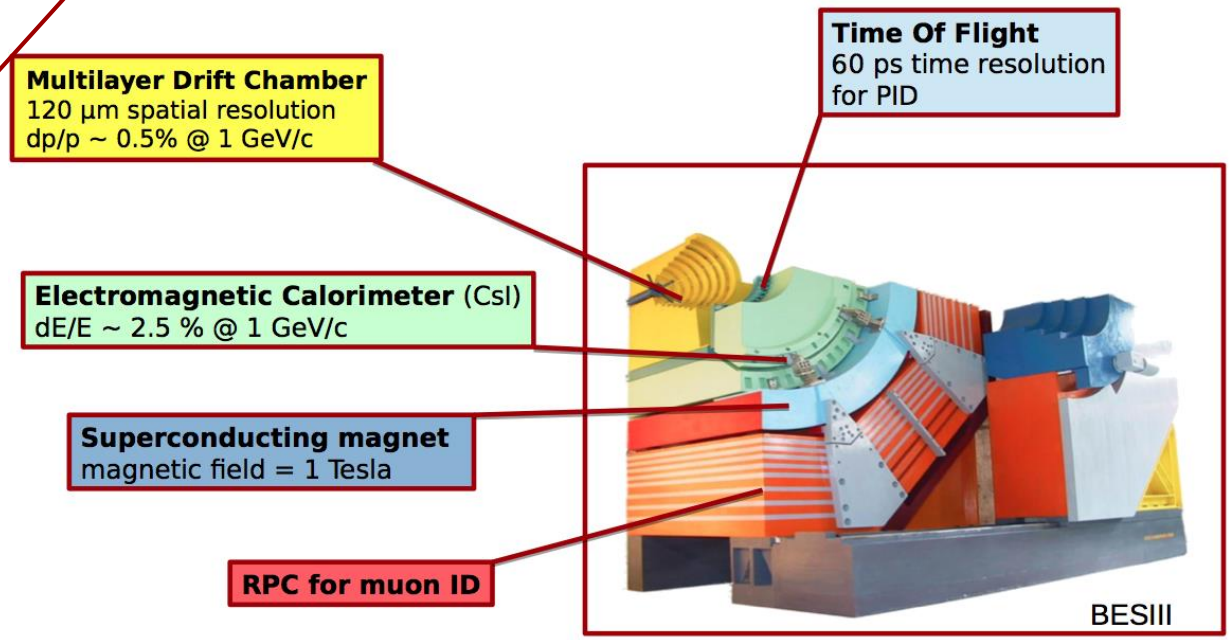
- Charm physics
- Tau physics
- Charmonium decays
- Light hadrons spectroscopy
- New physics

IHEP



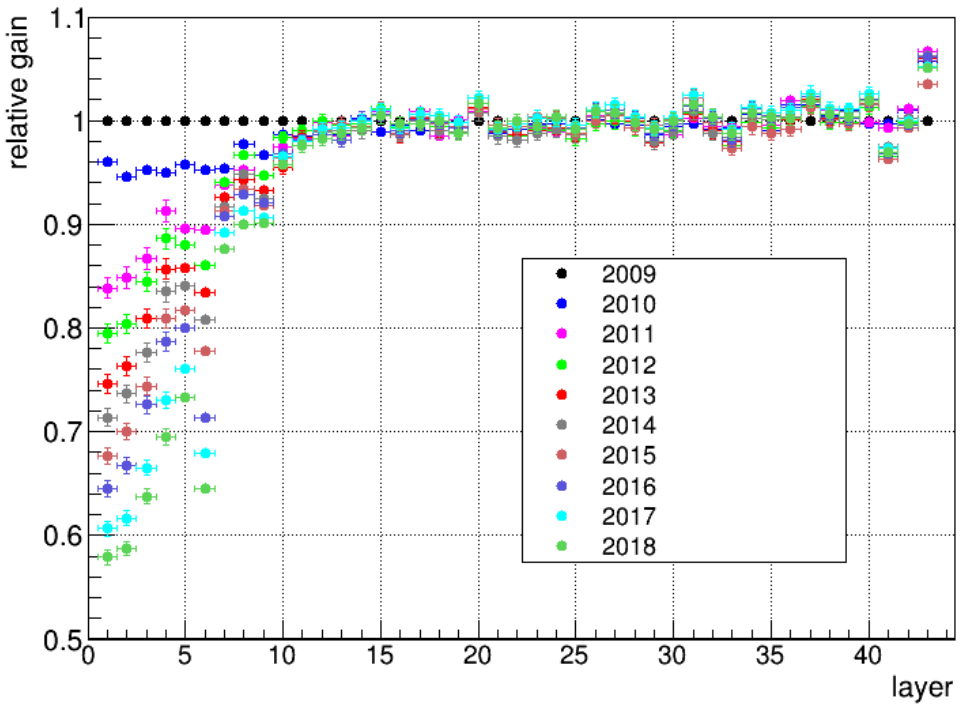
BEPCII

- Energy 2-4.6 GeV
- Luminosity 10^{33} $cm^{-2}s^{-1}$

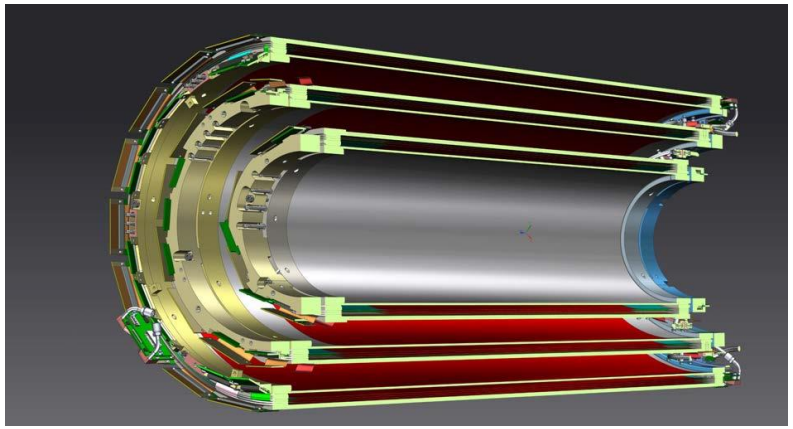


BESIII detectors

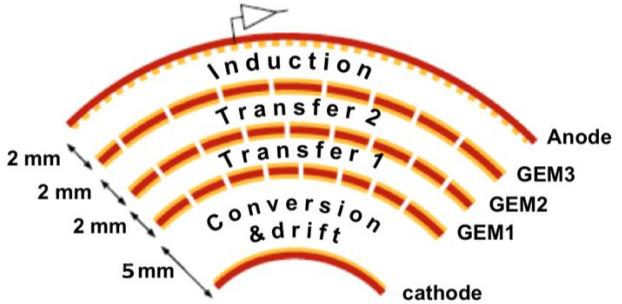
Cylindrical Gas Electron Multiplier Inner Tracker



Loss of gain in current MDC



CGEM CAD model

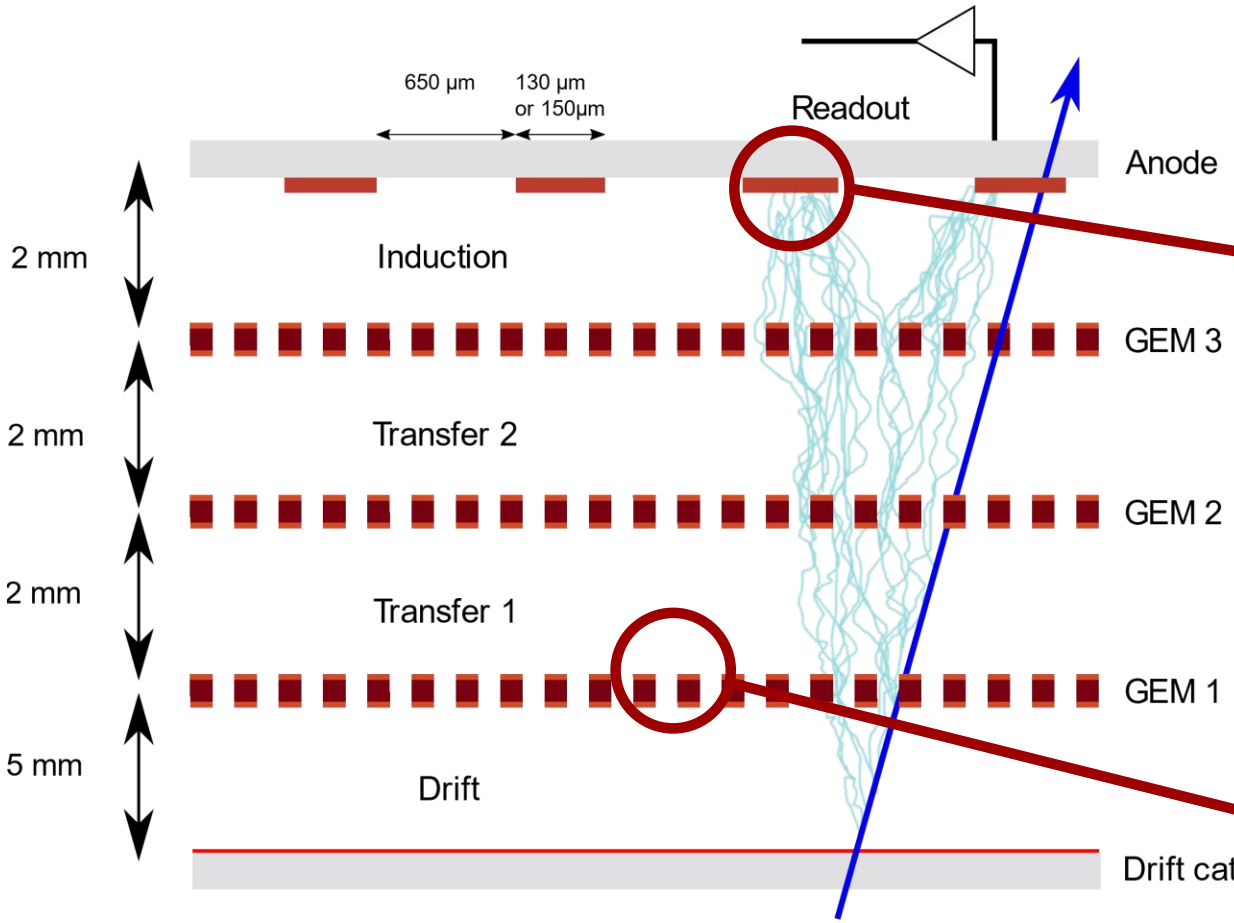


Single layer internal layout

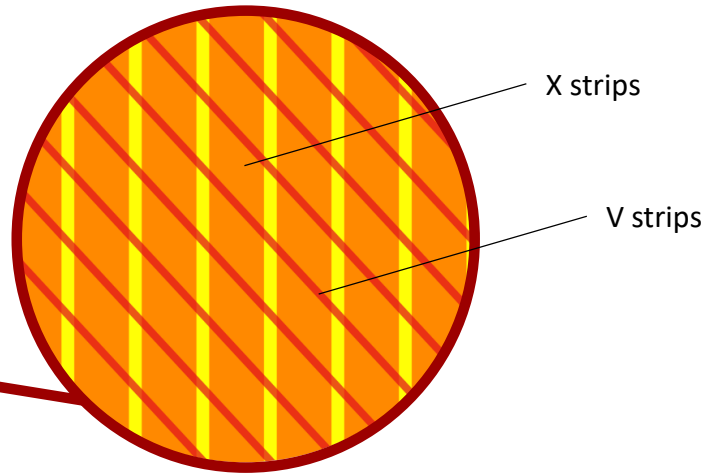
Detector features:

- Radial resolution <130 μm
- Resolution along the beam direction < 500 μm
- Momentum resolution σ_{Pt}/p_t ~0.5%
- Time resolution about 5 ns
- Material budget X_0~ 0.5% for each layer
- High rate capabilities (10kHz/cm^2)

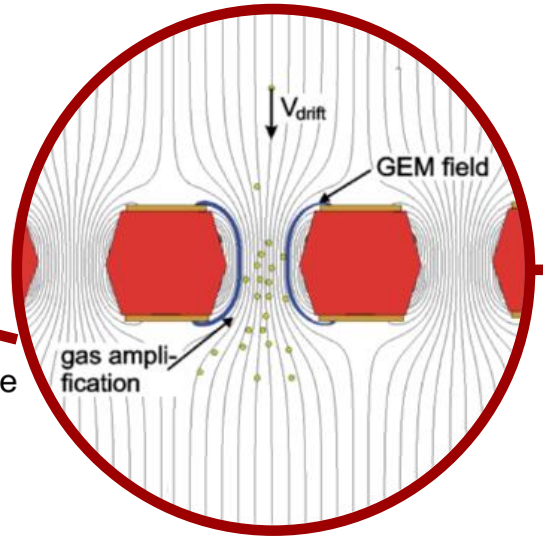
GEM working principles

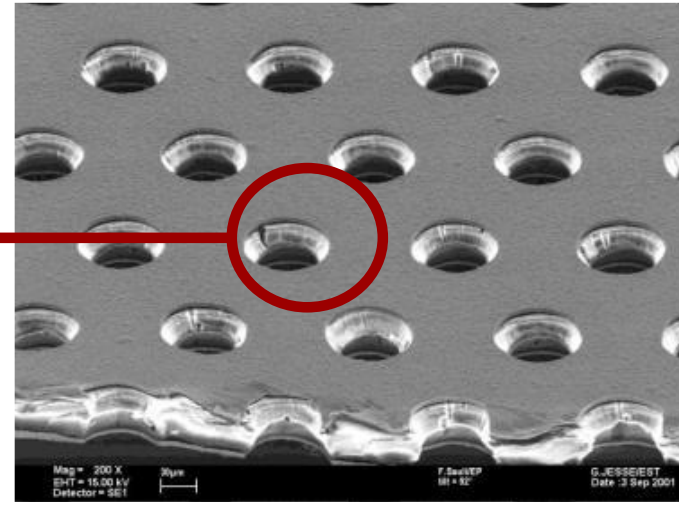


Anode strip structure



Holes structure



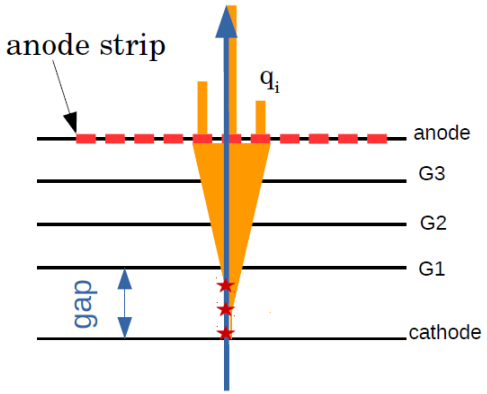


Ref. Fabio Sauli *"The gas electron multiplier (GEM)"* in: Nuclear Inst. and Methods in Physics Research, A 805 (2016), pp. 2–24.

Analog readout

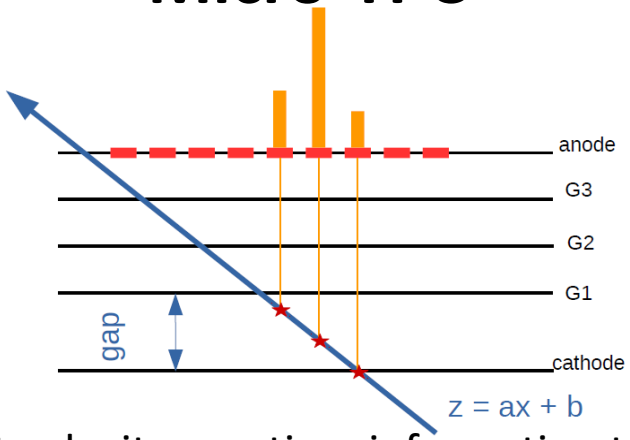
- Charge centroid and µ-TPC algorithms
- 130 µm spatial resolution with strip pitch of 650 µm
- Total number of channels ~ 10 000 (vs 25000 with binary readout to obtain similar resolution)
- Apply threshold on collected charge to cut noise-induced events

Charge centroid



- Weighted average position from fired strips
- Improve spatial resolution vs digital readout (constrained to the strip pitch)

Micro-TPC



- Known the drift velocity, use time information to project the signal origin on the Z axis
- Reconstruct the particle track from these coordinates
- Improve the spatial resolution for tilted tracks and in magnetic fields

Ref. Lia Lavezzi et al. *"The new cylindrical GEM inner tracker of BESIII"* in: Int.J.Mod.Phys.Conf.Ser. 46 (2018), DOI: 10.1142/S2010194518600777

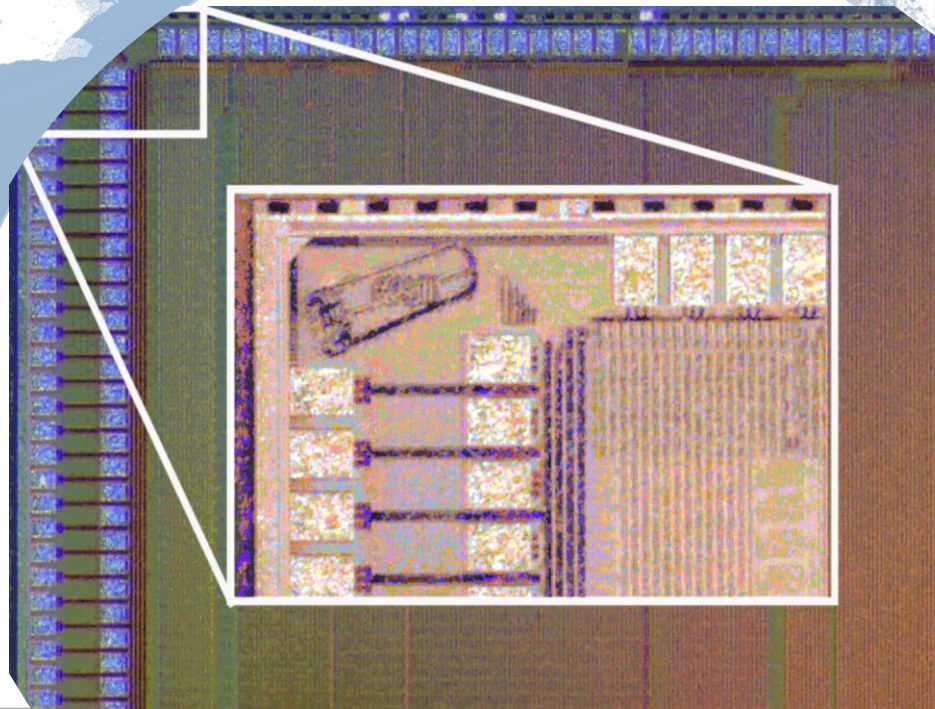
TIGER

Design:

- INFN-Torino
- LIP-Lisboa
- PETSYS-Lisboa
- IHEP Beijing

Test ancillaries:

- INFN-Torino

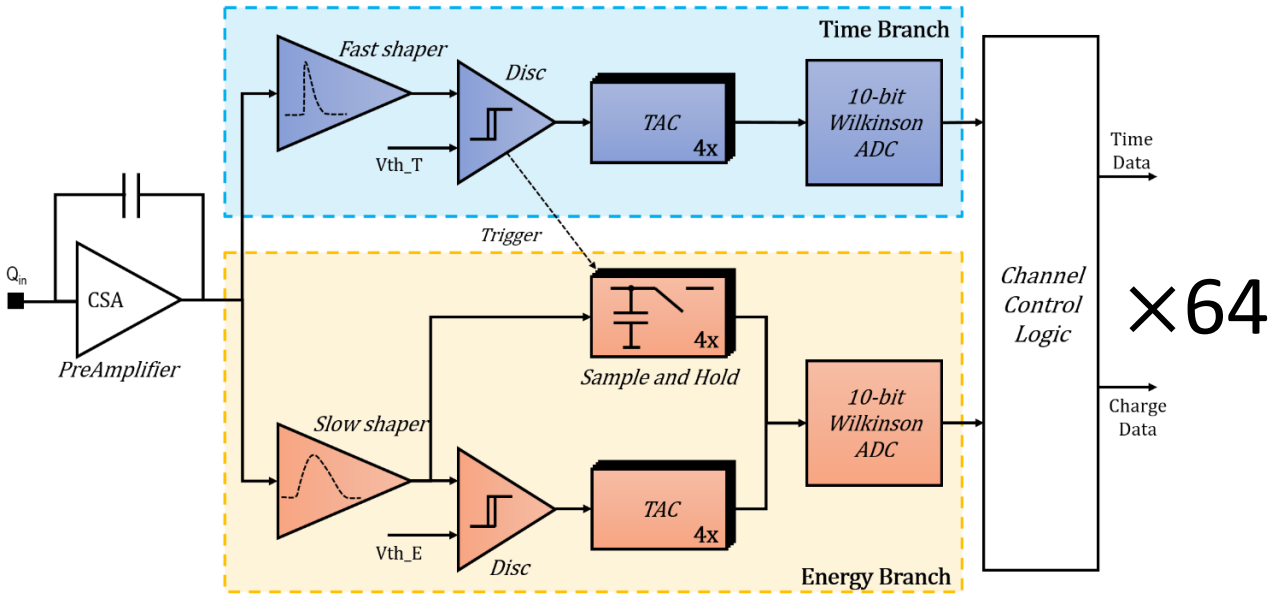


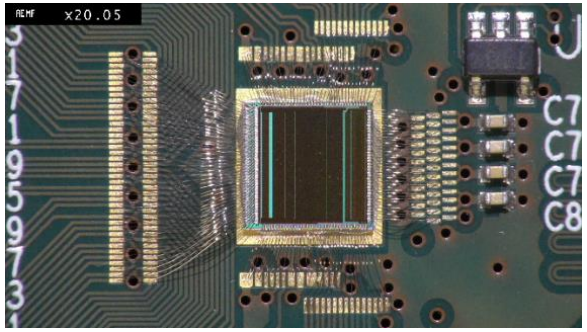
Ref. A. Rivetti et al. *"TIGER: A front-end ASIC for timing and energy measurements with radiation detectors* in: Nuclear Inst. and Methods in Physics Research, A 924 (2019), pp. 181–186.

TIGER ASIC

Torino Integrated Gem Electronics Readout

Font end architecture





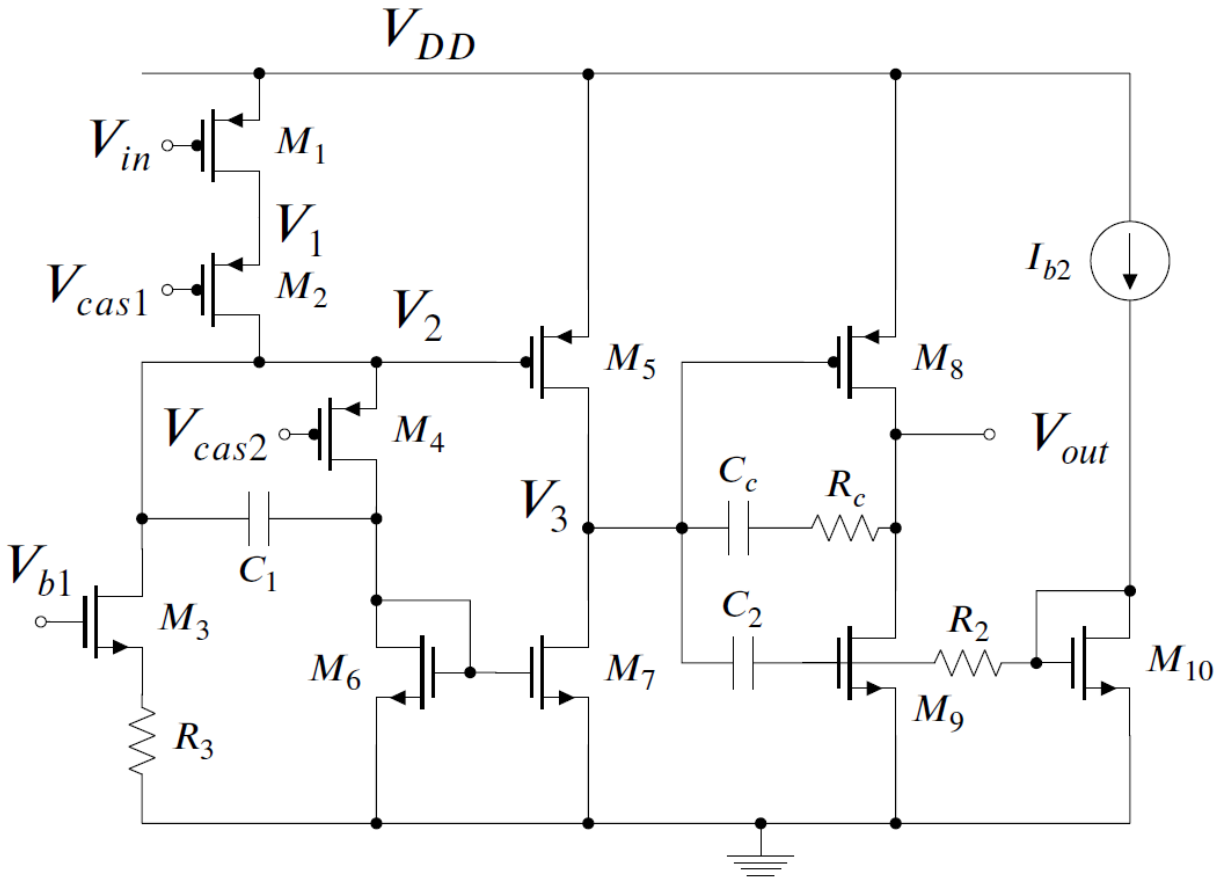
TIGER bonded on PCB

Front end board (FEB)

Chip features:

- 64 channels
- Power consumption < 12 mW/channel
- Sustained event rate 100 kHz
- Input dynamic range up to 50 fC
- Time resolution < 5 ns
- ENC < 2000 e^- rms with 100 pF input capacitance
- Analog read out providing charge and time measurement
- Digital logic protected from single event upset (SEU)
- Tunable internal test pulse generator
- 110 nm technology

Charge Sensitive Amplifier



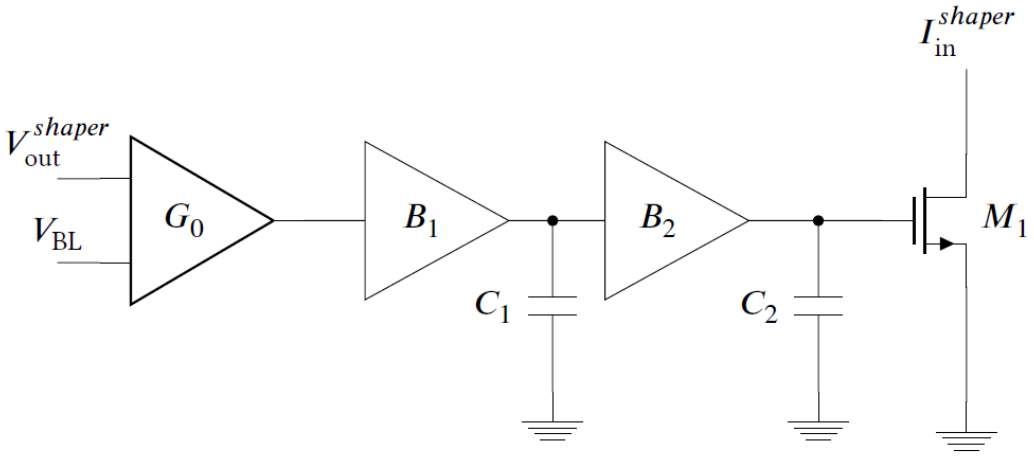
Three stage cascoded common source amplifier

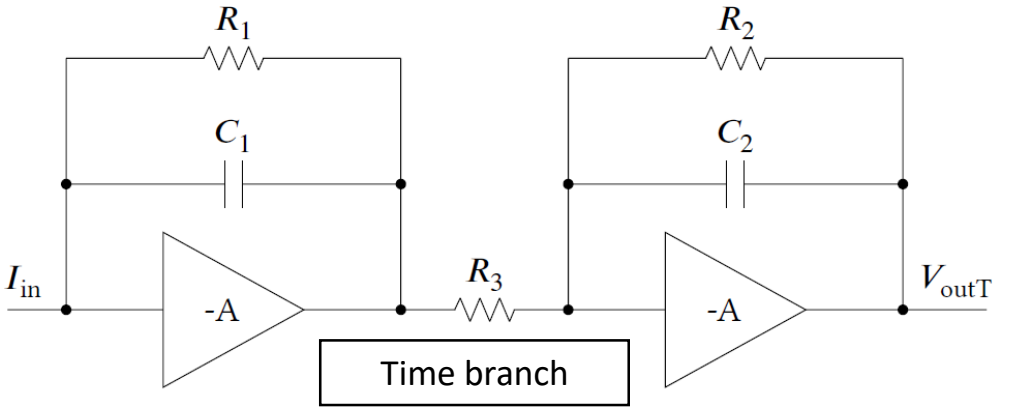
- ENC target < 2000 e^- @ C_{in} = 100 pF
- Q_{in} = 2 - 50 fC
- PMOS input transistor to reduce 1/f noise
- g_{m1} ≈ 80 mS (3.6 mA bias current)

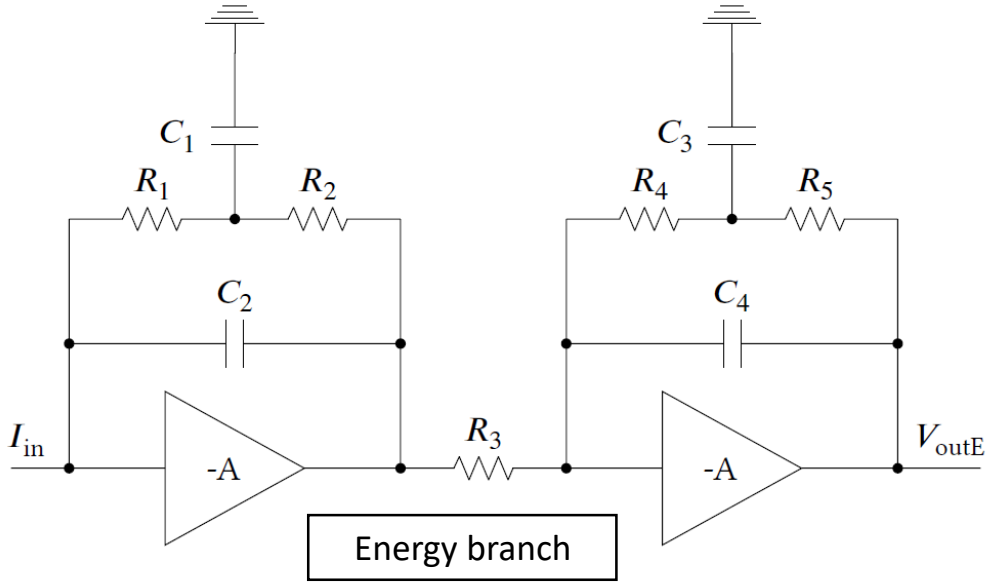
Ref. G. De Geronimo *"An ASIC for micropattern detectors"* in: *IEEE Trans. Nucl. Sci., 60:2314-2321.2013*

Shaping

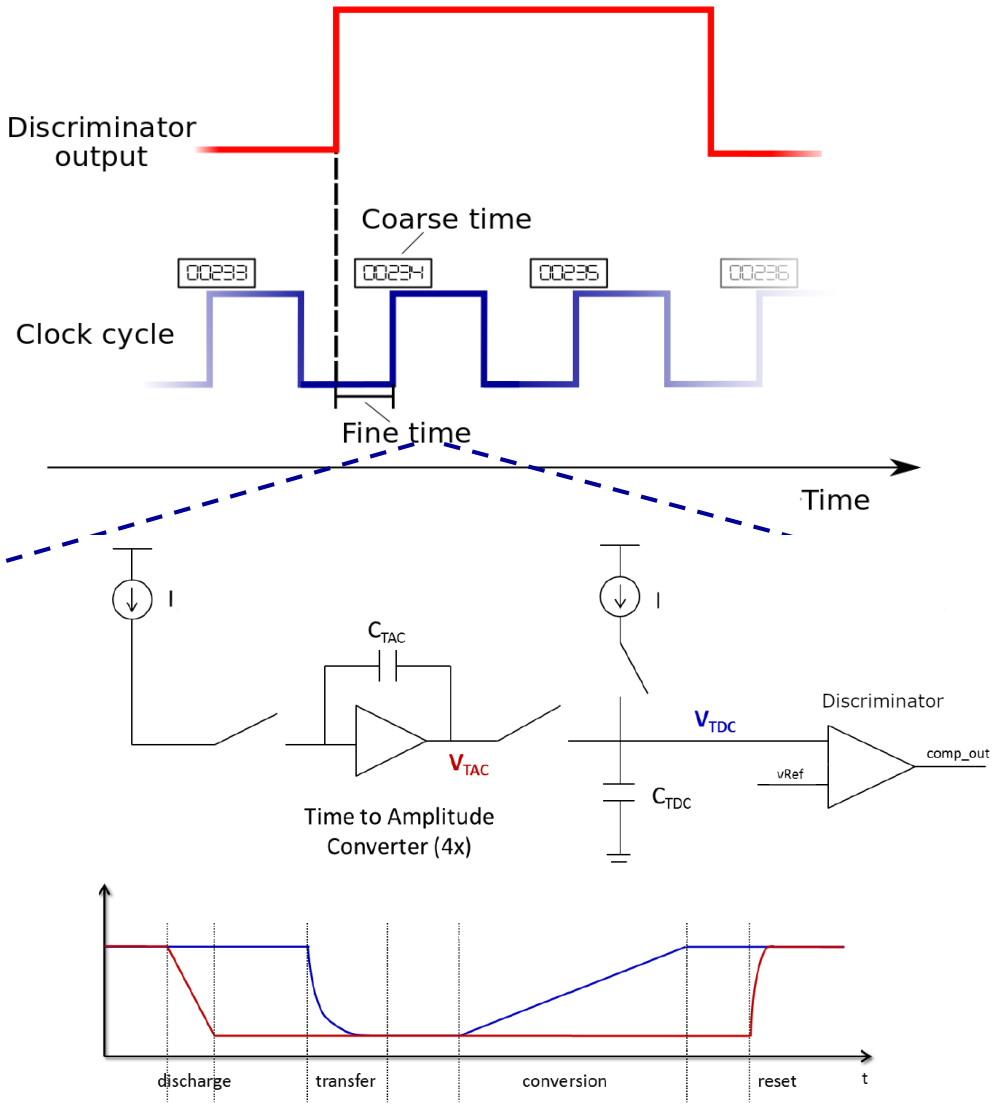
- Peaking time defined by feedback loop RC
  - **Time-branch**: 60 ns peaking time for low-jitter timing measurement
  - **Energy-branch**: 170 ns peaking time for signal-to-noise ratio optimization
- **Baseline holder** to lock the shapers output DC to an external reference value (V_{BL} = 350 mV)







Time measurement



Three accuracy levels (@160 MHz)

Frame-word

Clock counter cycles roll-over

204.8 µs time resolution

Coarse time

Hit clock cycle (16 bit counter)

6.25 ns time resolution

Fine time

Time to the next clock cycle

50 ps binning

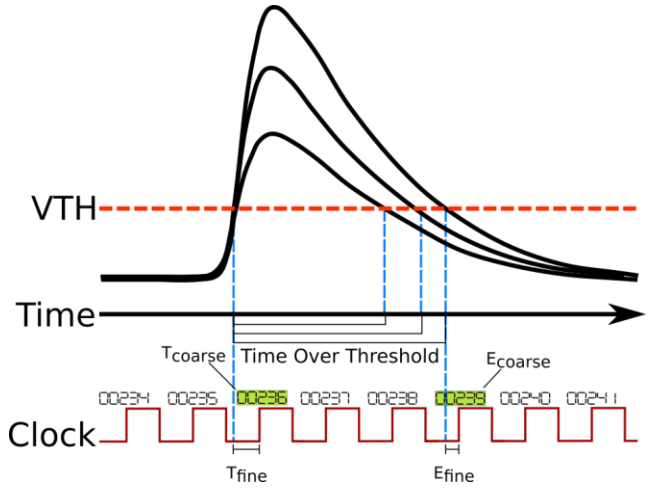
$$T = Coarse \times 6.25\ ns - (Fine\text{-}min) \times binning$$

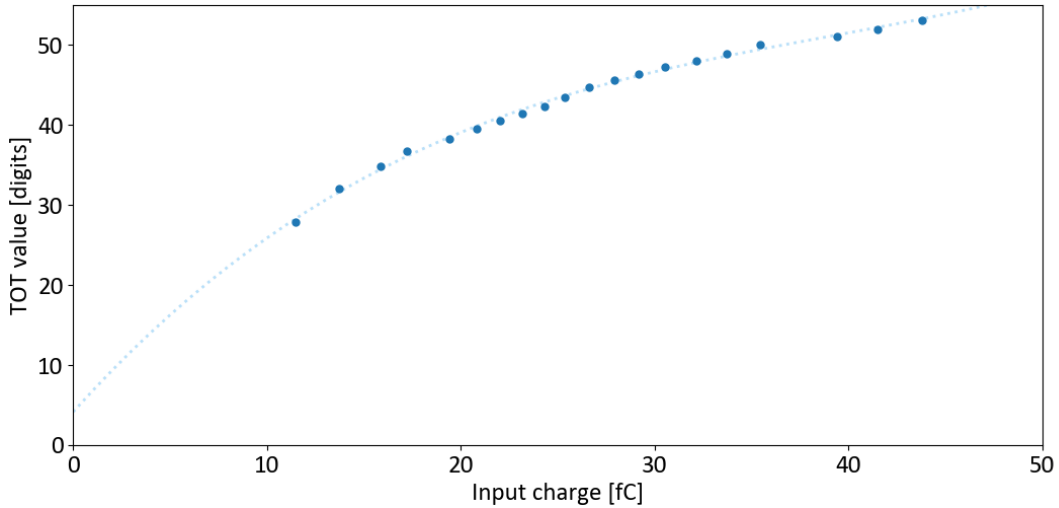
4 TAC per shaper for event de-randomization

1 Wilkinson ADC per branch

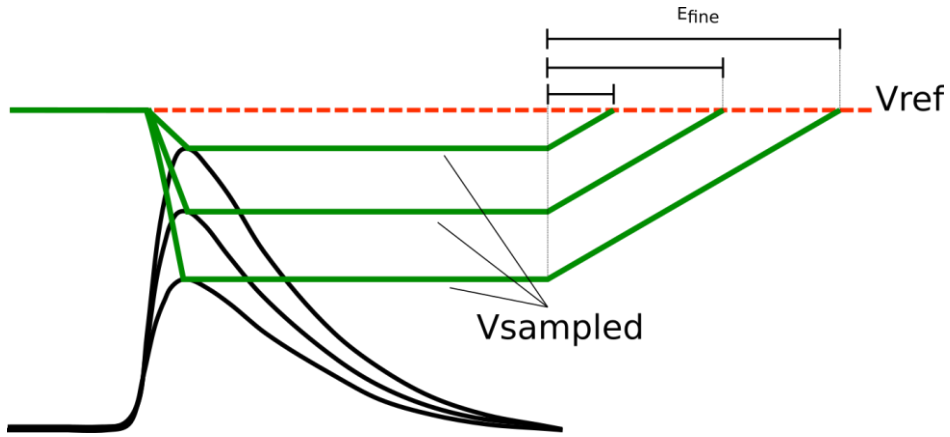
Charge measurement

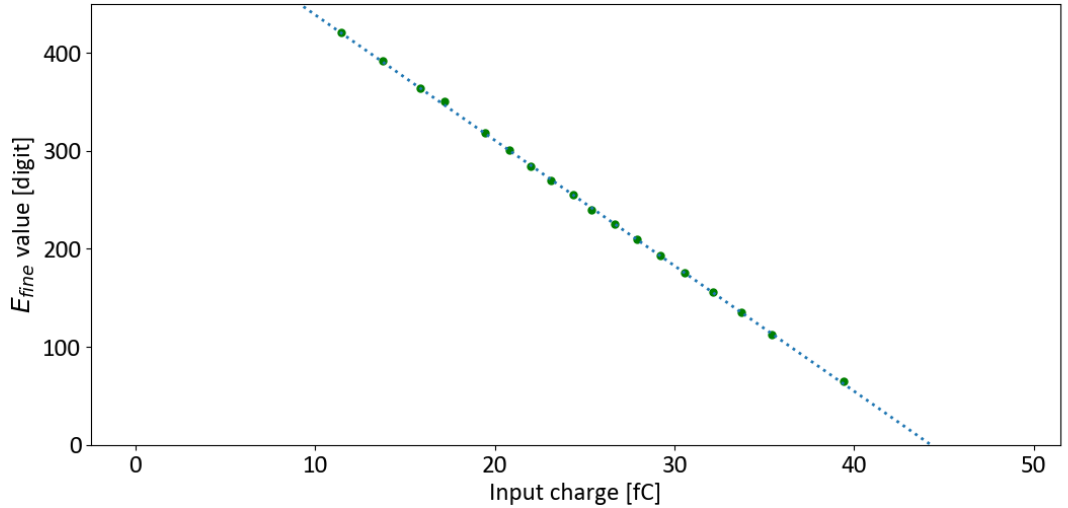
Time over Threshold





Sample & Hold





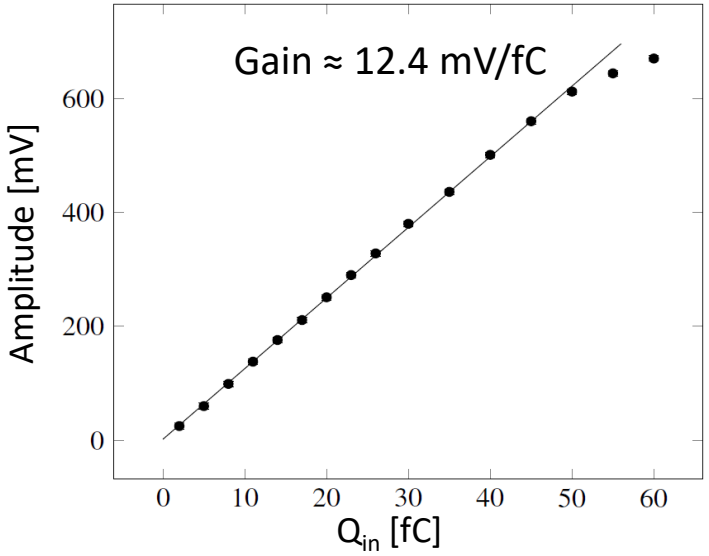
Digital backend

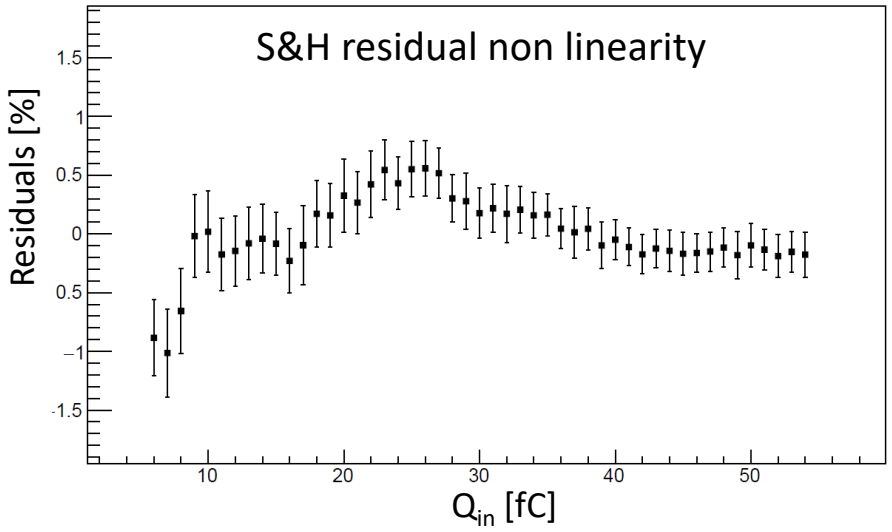
- Backend inherited from TOPFETv2
- 160-200 MHz system clock
- Full digital output with time and charge information
- 4 TX SDR/DDR LVDS links, 8b/10b encoding
- 10 MHz SPI-like configuration link
- SEU protections

The chip hit rate capabilities were tested and confirmed on silicon

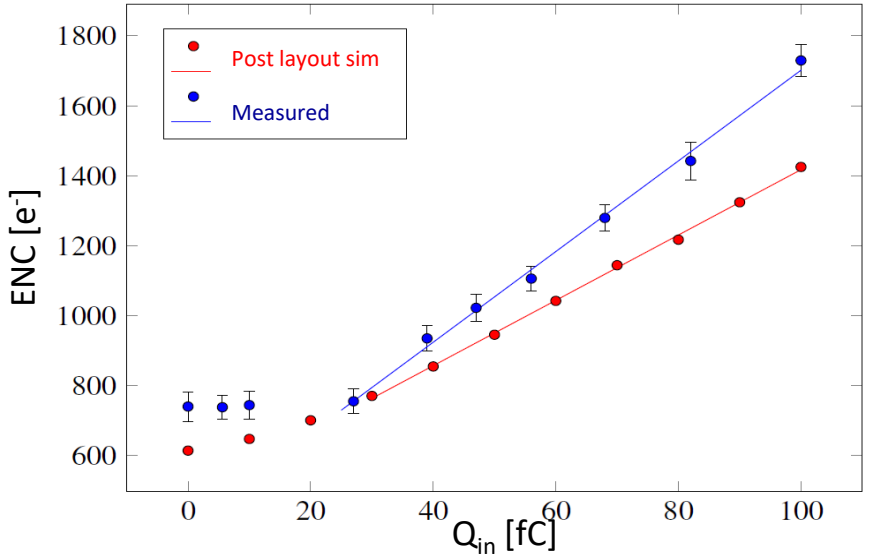
- 100 kHz for a single channel
- 60 kHz per channel when all are firing

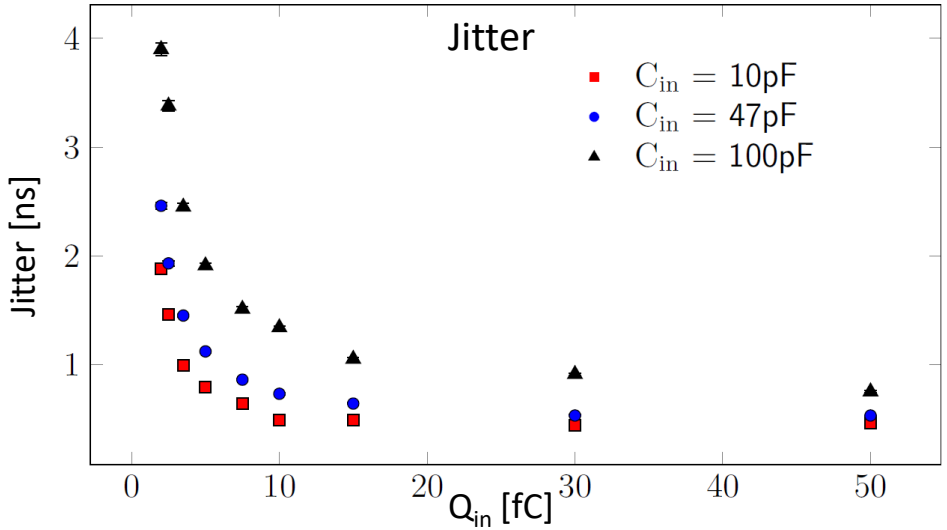
Performances on silicon

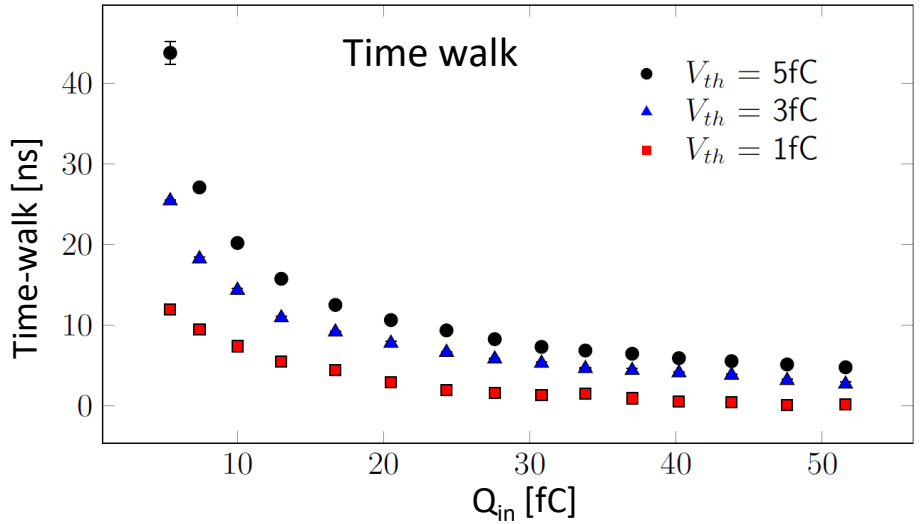




Noise (E-branch) @100 pF ≈ 1800 e-



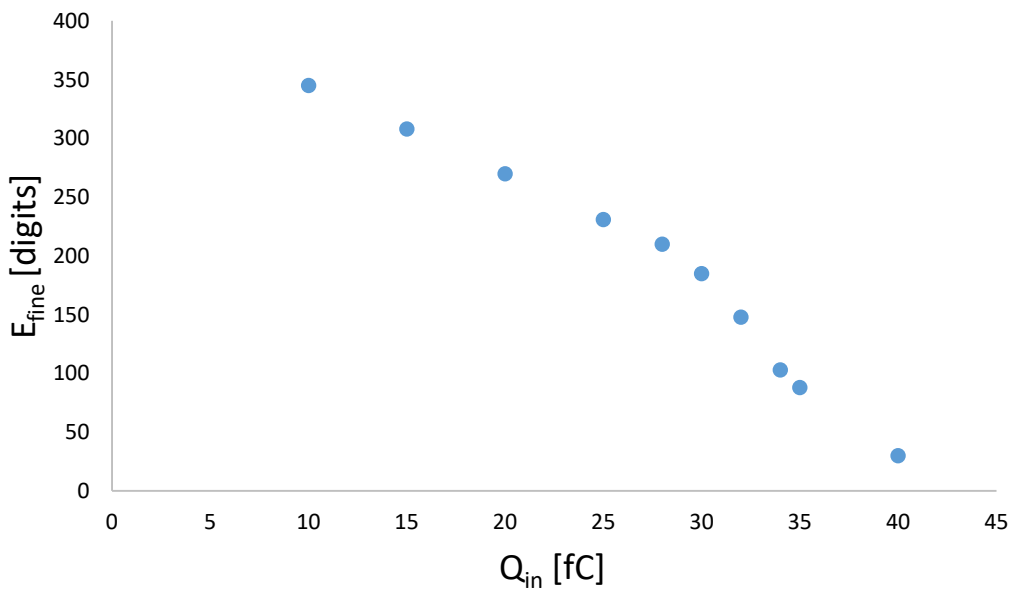




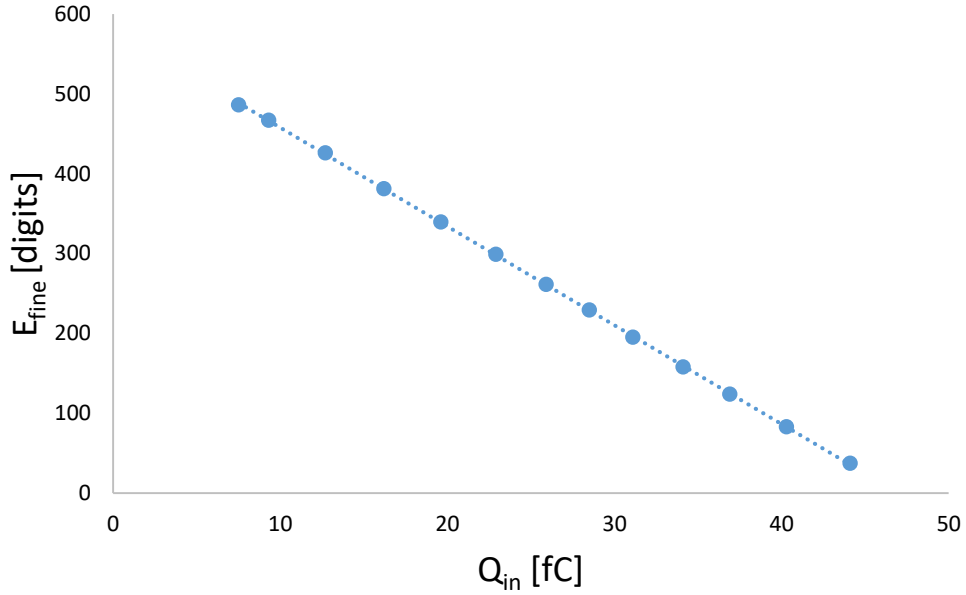
Ref. Fabio Cossio *"A mixed-signal ASIC for time and charge measurements with GEM detectors"* , PhD Thesis (PoliTO-2019)

Tuning

S&H with initial configuration



S&H with new configuration



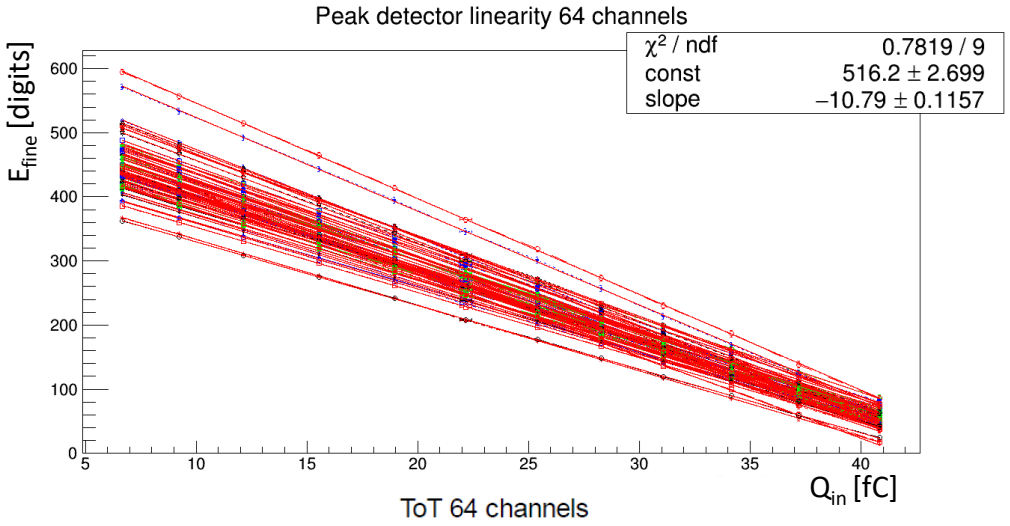
Production yield with our configuration*

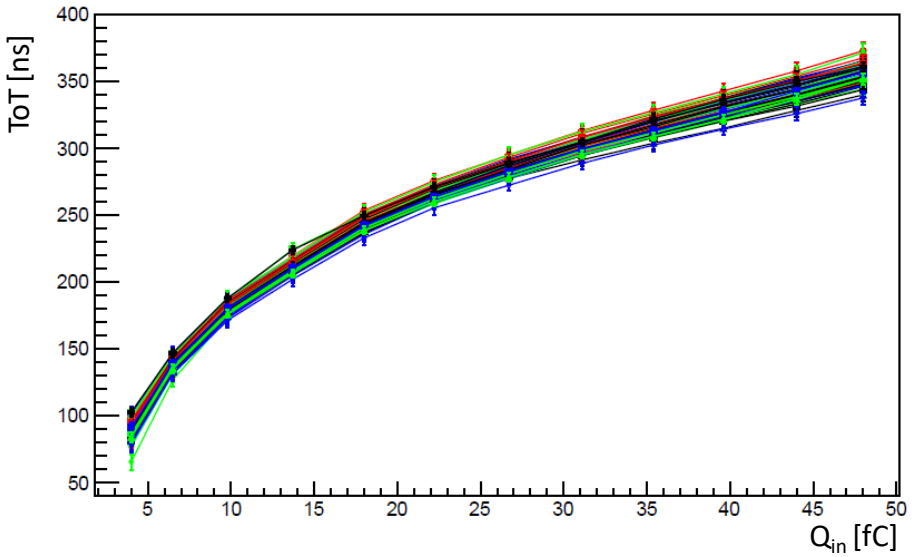
- 98% working chips:
  - 80% meeting our requirements
  - 18 % unusable
- 2 % totally faulty chips

Requested performance achieved

*Data from the layer 1 production

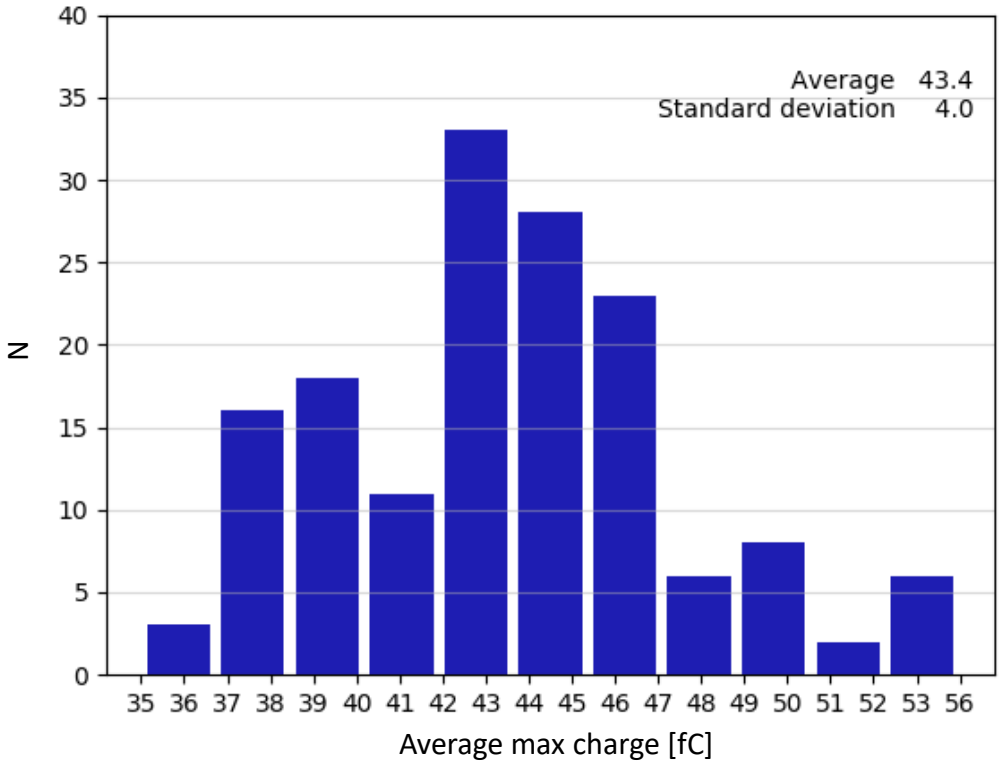
Calibration results





S&H range

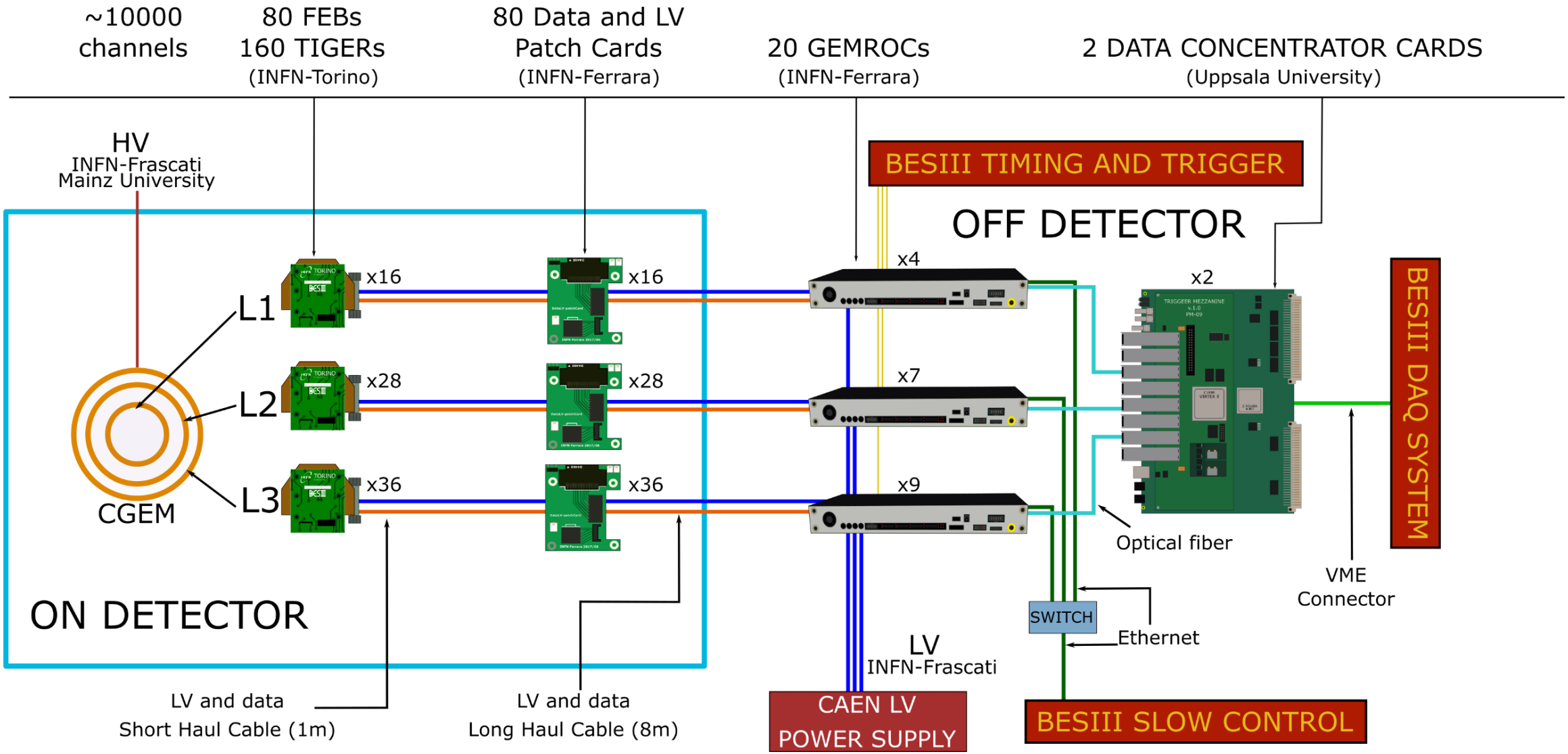
Maximum input charge (channel average)



Calibration completed for 10k channels

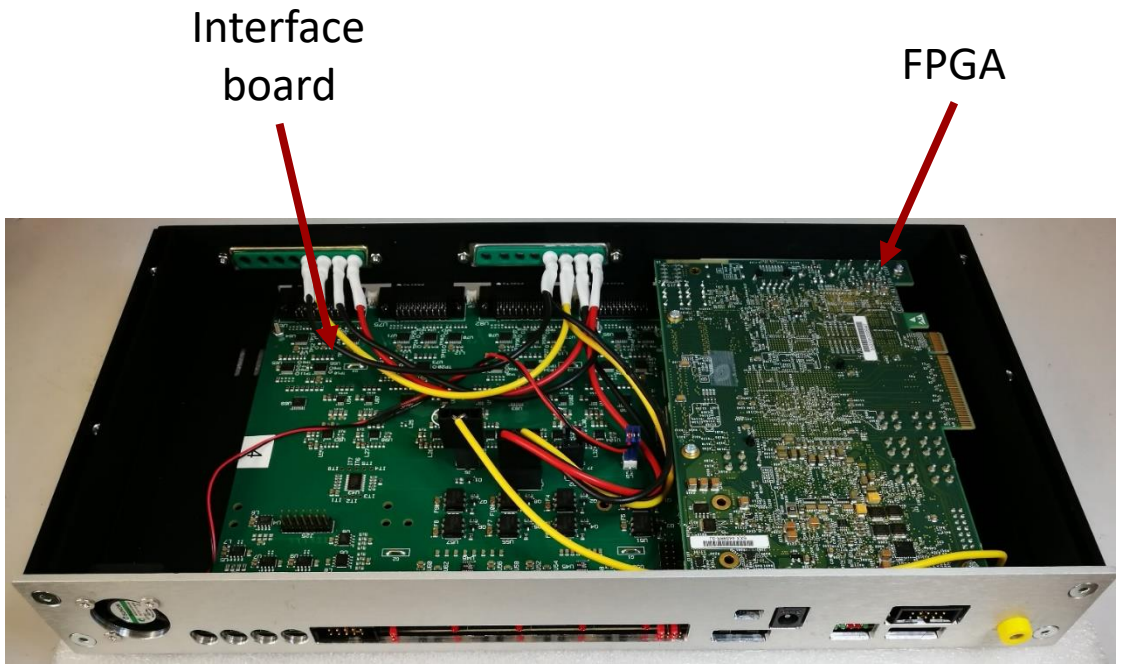
Full electronics chain

Electronics read-out



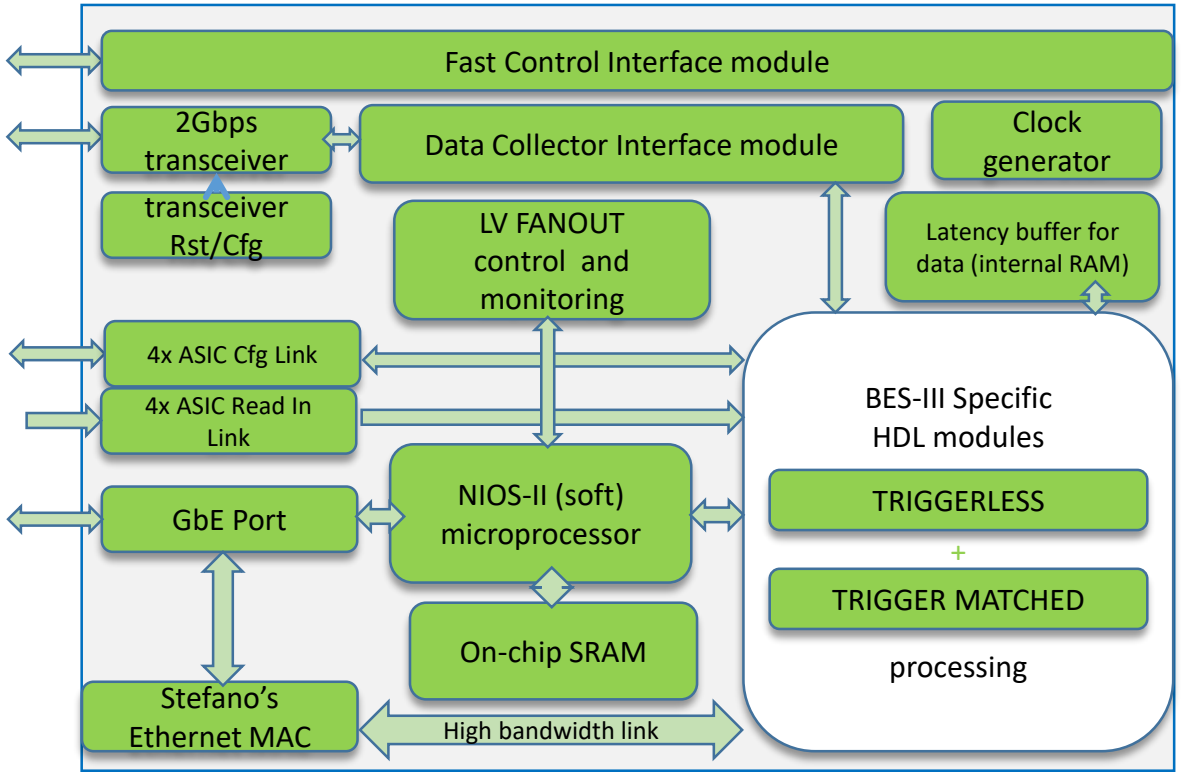
GEM Read-Out Cards

Designed by Electronic workshop INFN-Ferrara



GEMROC module

FPGA block scheme

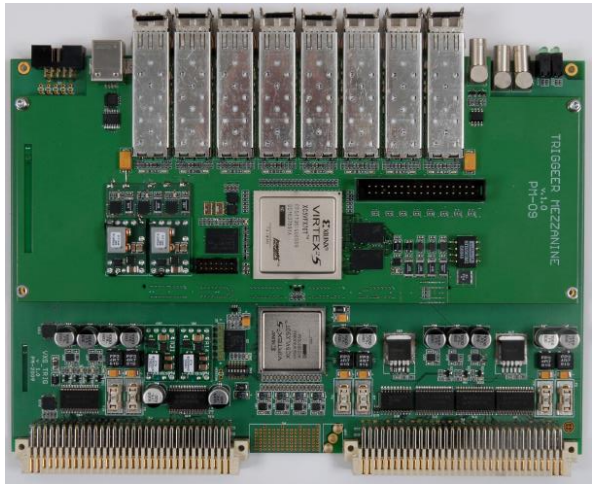


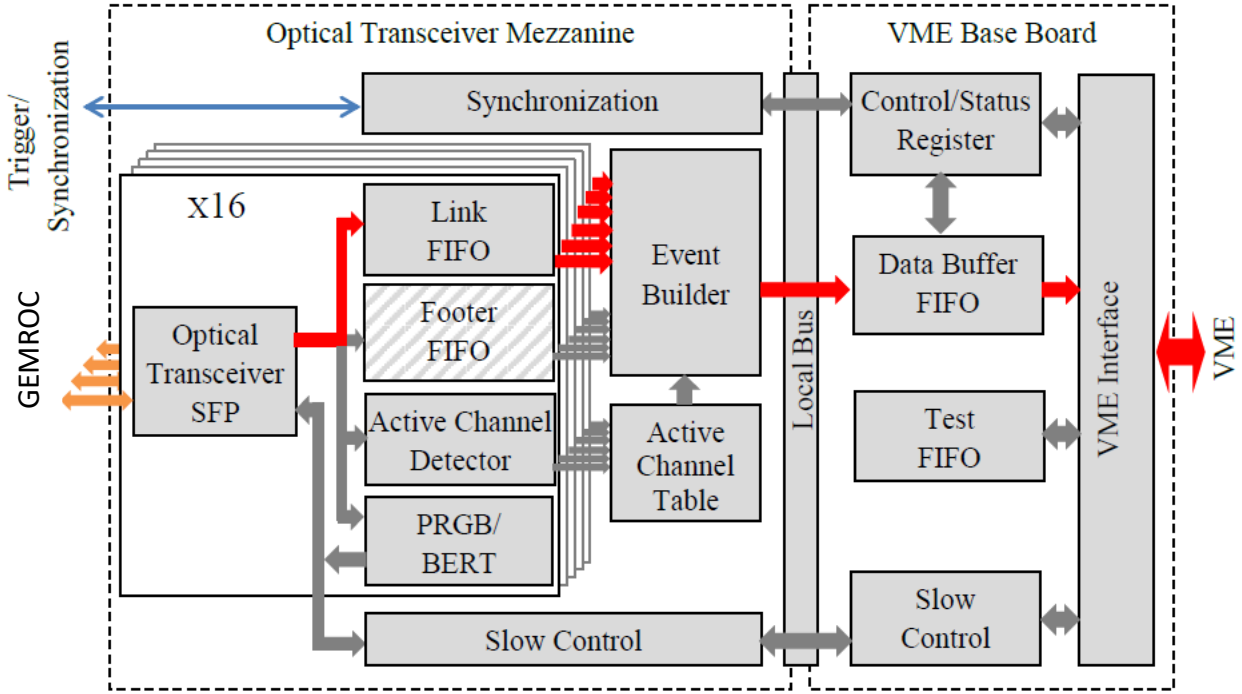
All blocks working, final tests ongoing

GEM-Data Concentrator

Designed by Uppsala University

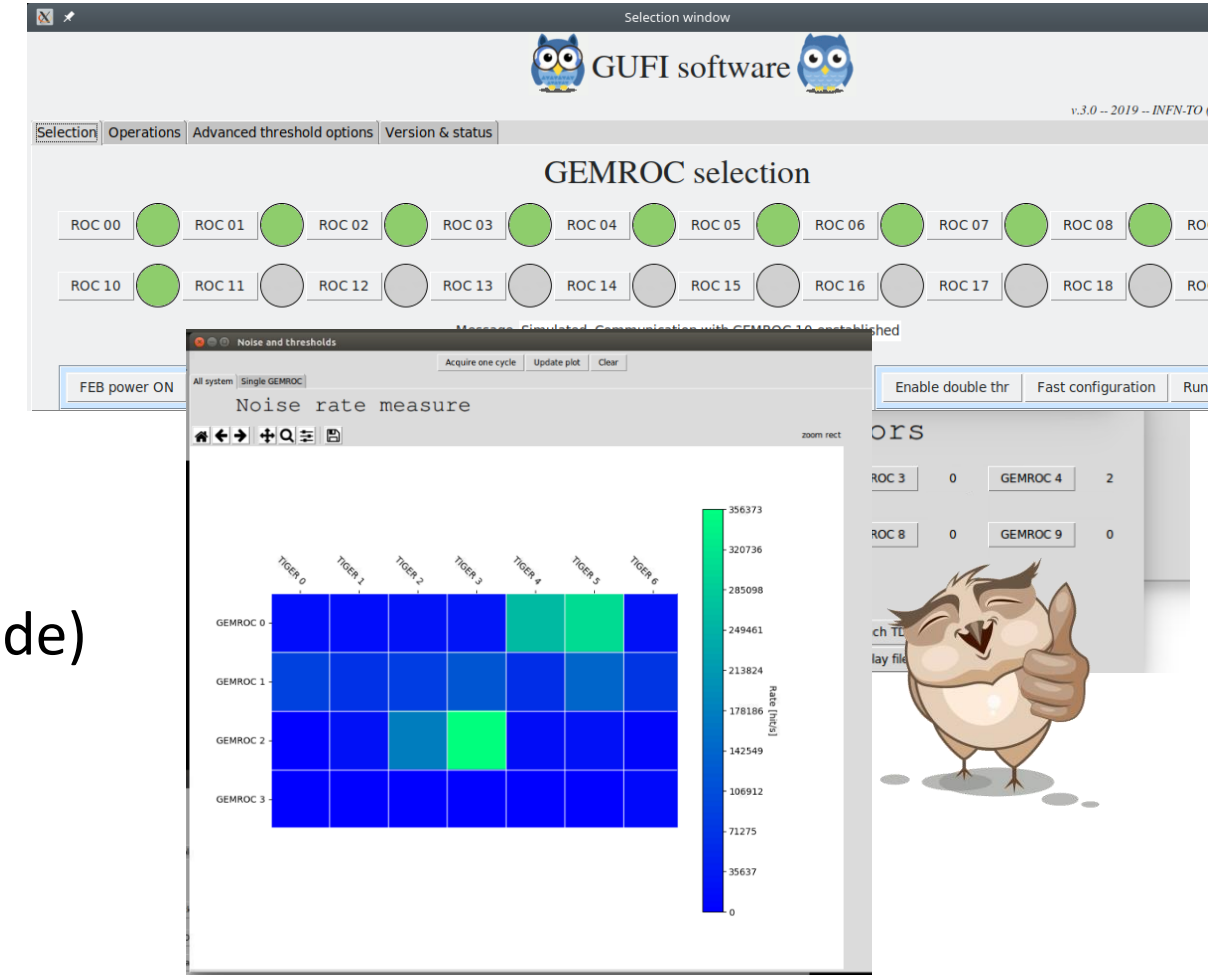
- Receives signal from the GEMROCs via optical links
- Build the events
- Optical links @ 2 Gb/s
- Interface trough VME with the BESIII DAQ





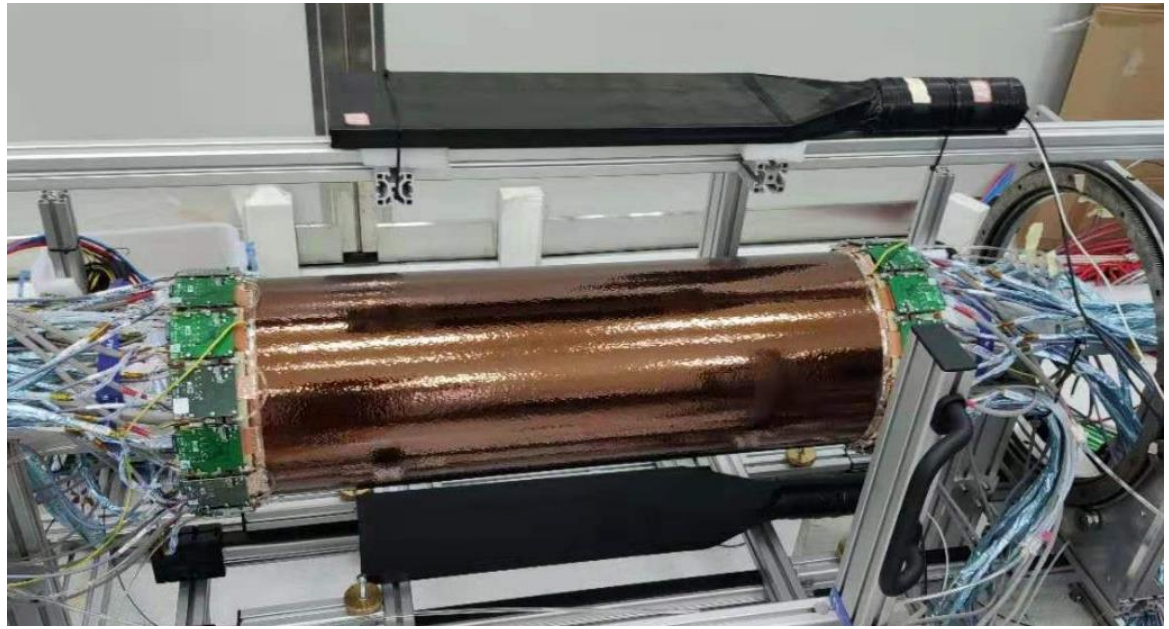
Graphical User Frontend Interface

- Interface with GEMROCs and TIGERs
- Configure both the devices
- Manage acquisition
- Online monitoring
- Measure noise rate and other performances
- User friendly interface (user mode/expert mode)



On detector performances

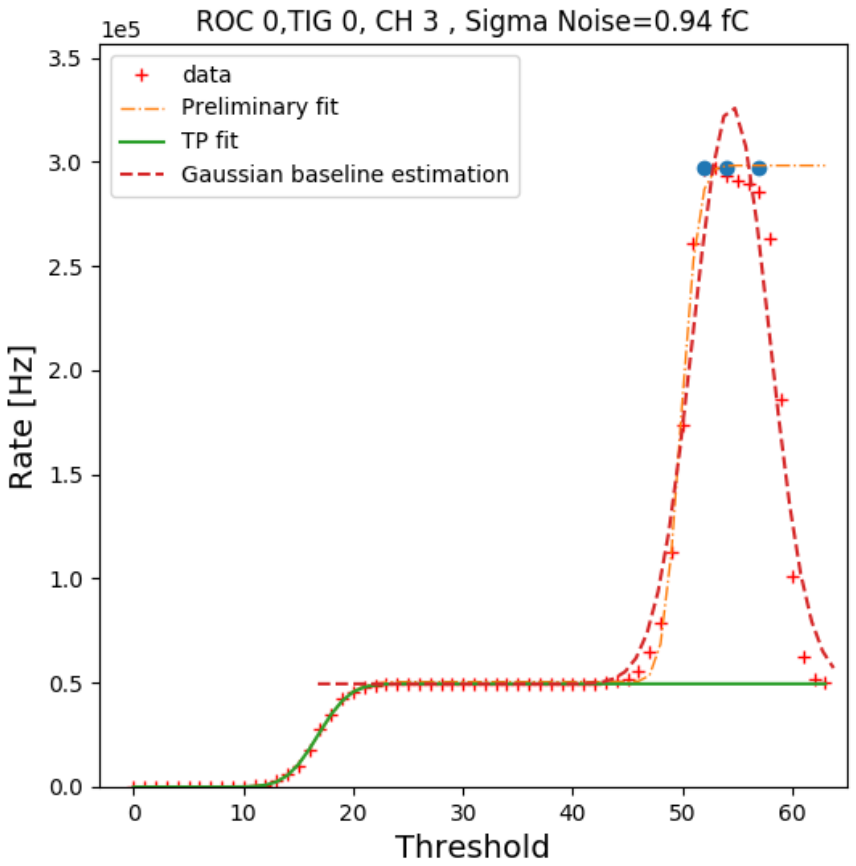
Setup status

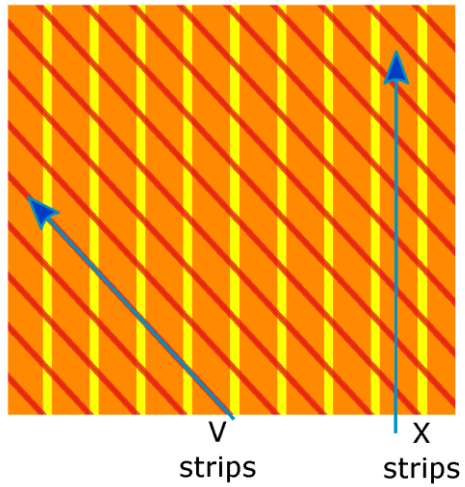


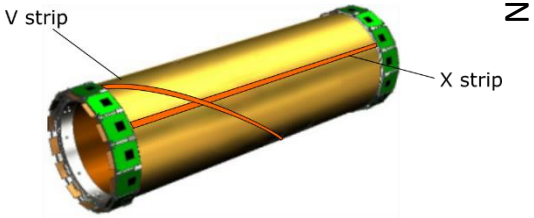
The readout chain integration is ongoing:

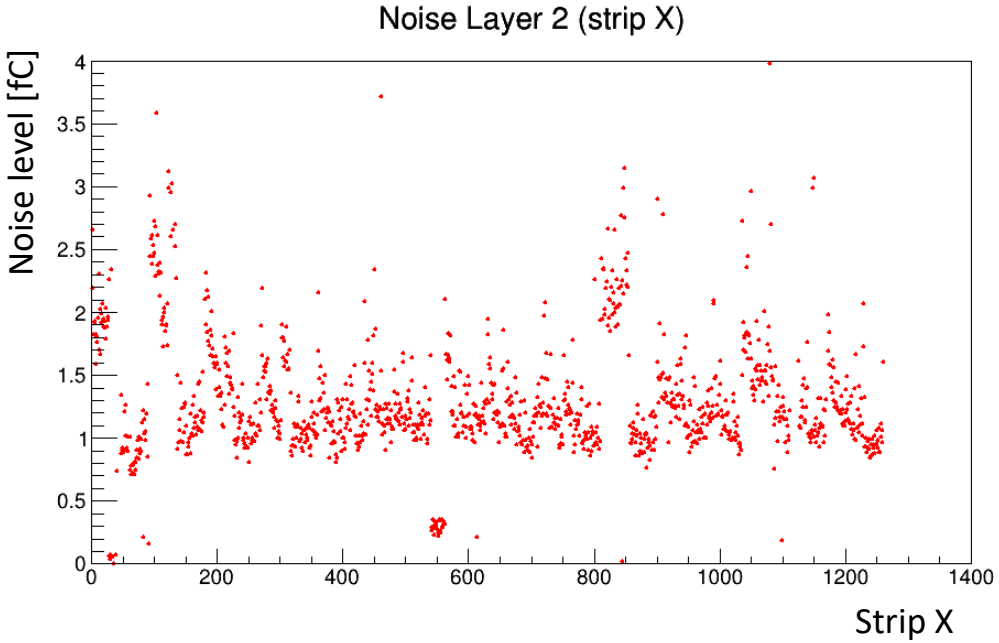
- L1 and L2 are instrumented with the ASICs
- Cosmic rays are acquired to evaluate system condition
- The GEMROC firmware is continously updated to maximize trigger-matching and communication performance and robustenss
- Software tools are constantly developed to improve the system understanding and capabilities
- The final layers of the detectors will arrive within 2019

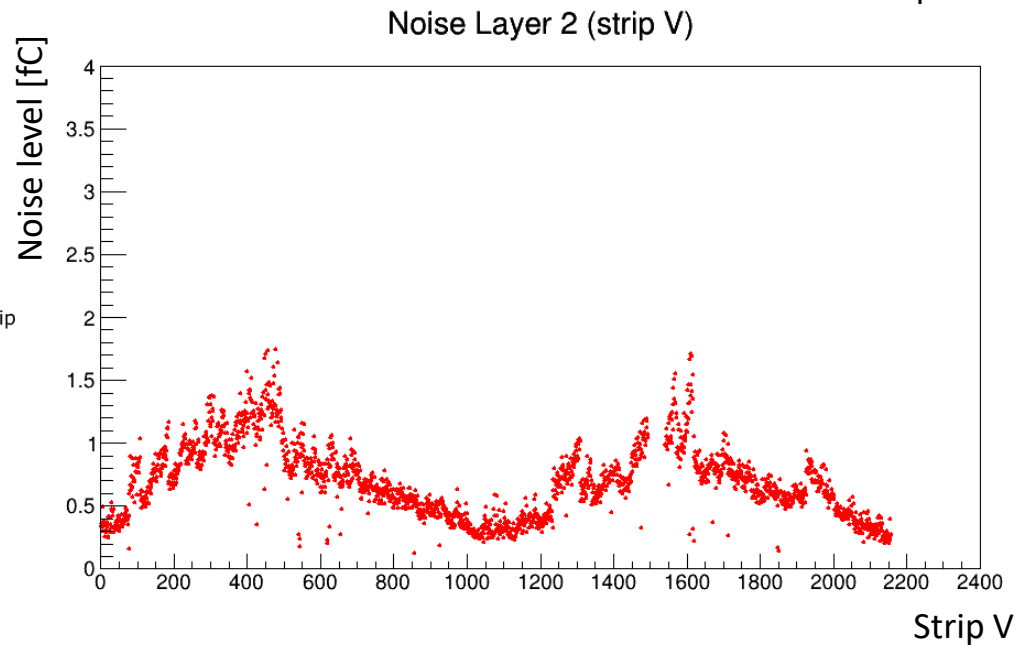
Noise levels









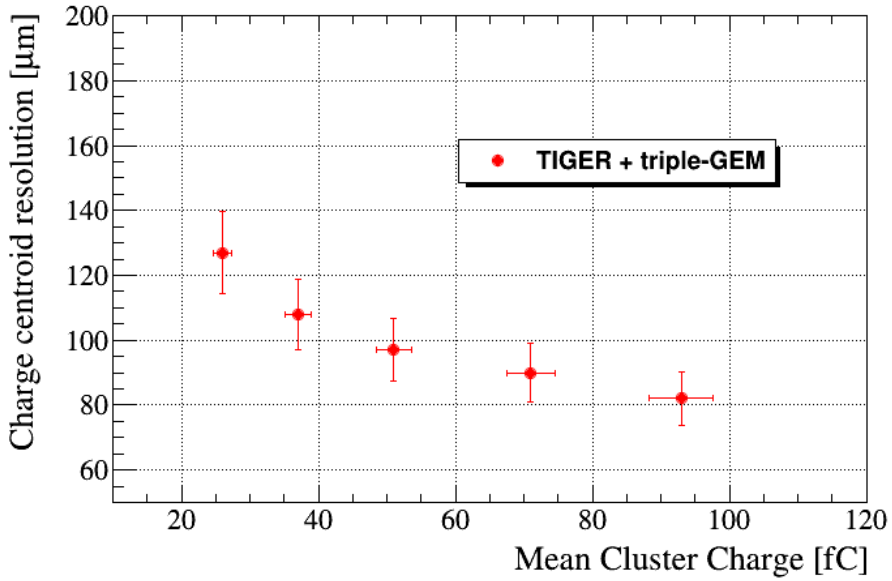


The noise is measured on the system using the internal test pulse and a threshold scan

Tracking performances

Planar detector

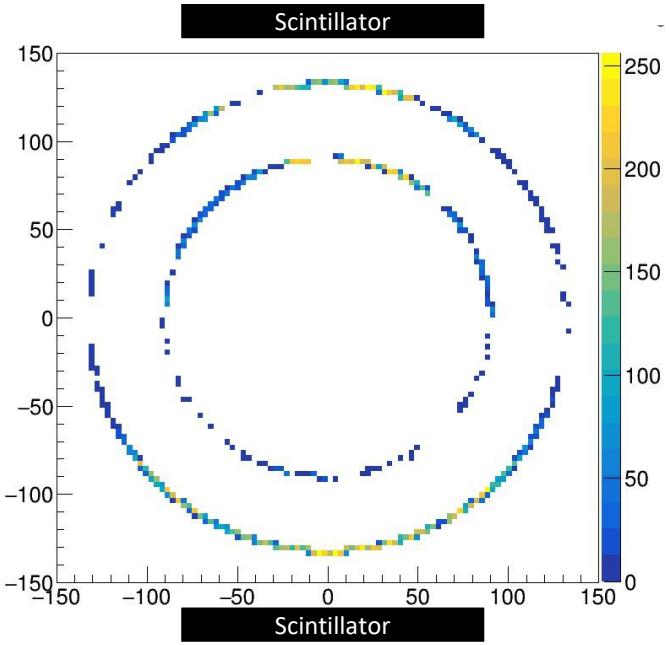
Last year beam test results



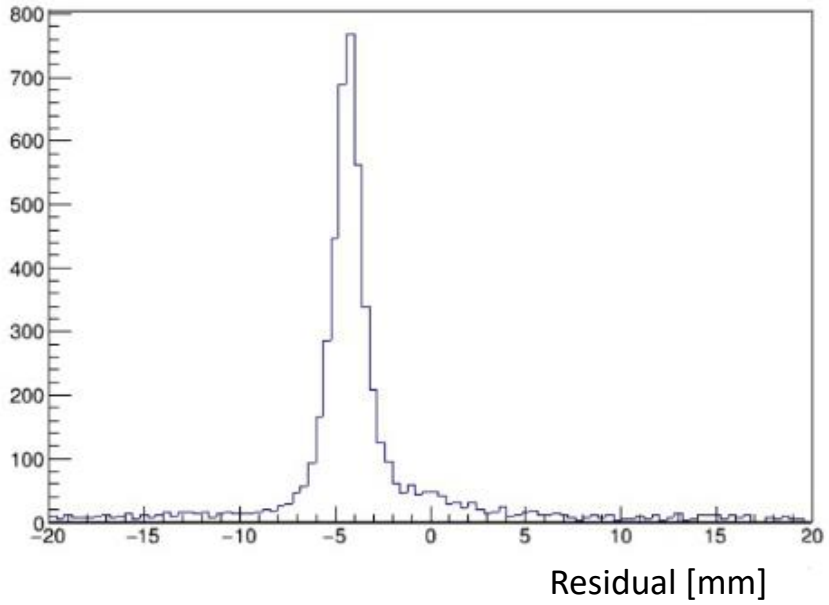
Ref. R. Farinelli *"Research and development in cylindrical triple-GEM detector with µTPC readout for the BESIII experiment"* , PhD Thesis (UniFe-2019)

Cylindrical detector

Detector hit rate



Residual distribution (X strips)



Results

- All the parts are tested and ready to be installed, 2 layers are already instrumented
- The system is stable and reliable
- We are able to produce data with good quality, useful for the tracking software final tuning and the detector performance evaluation

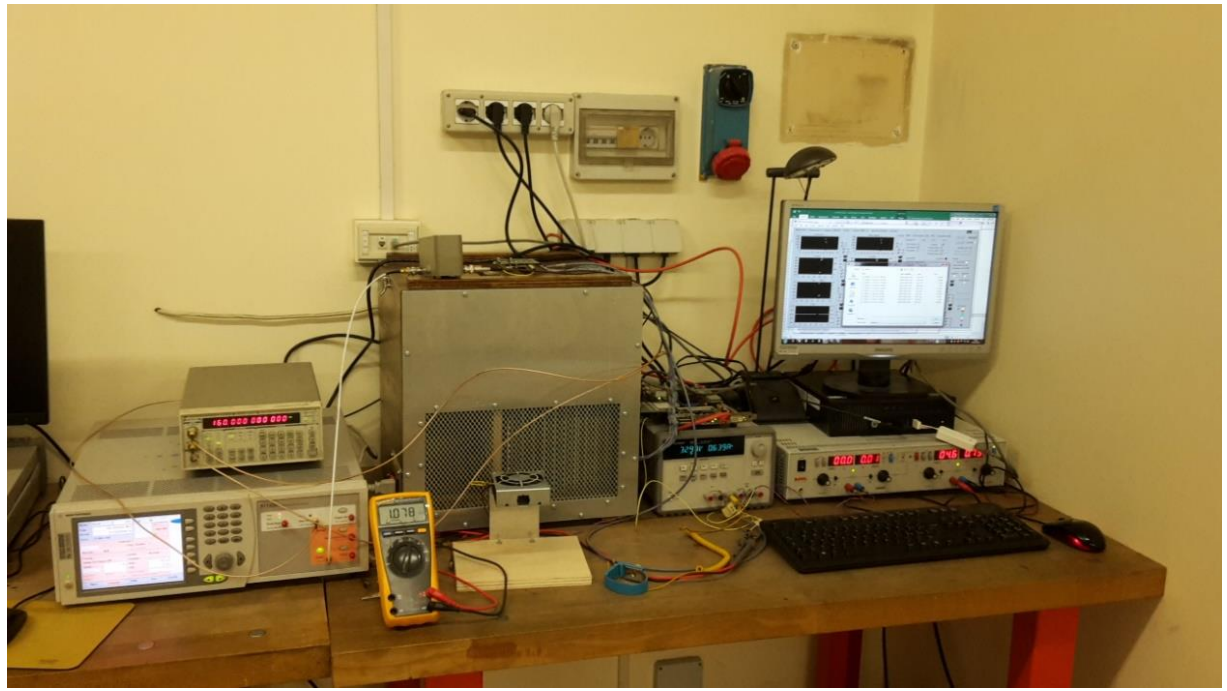
Next steps

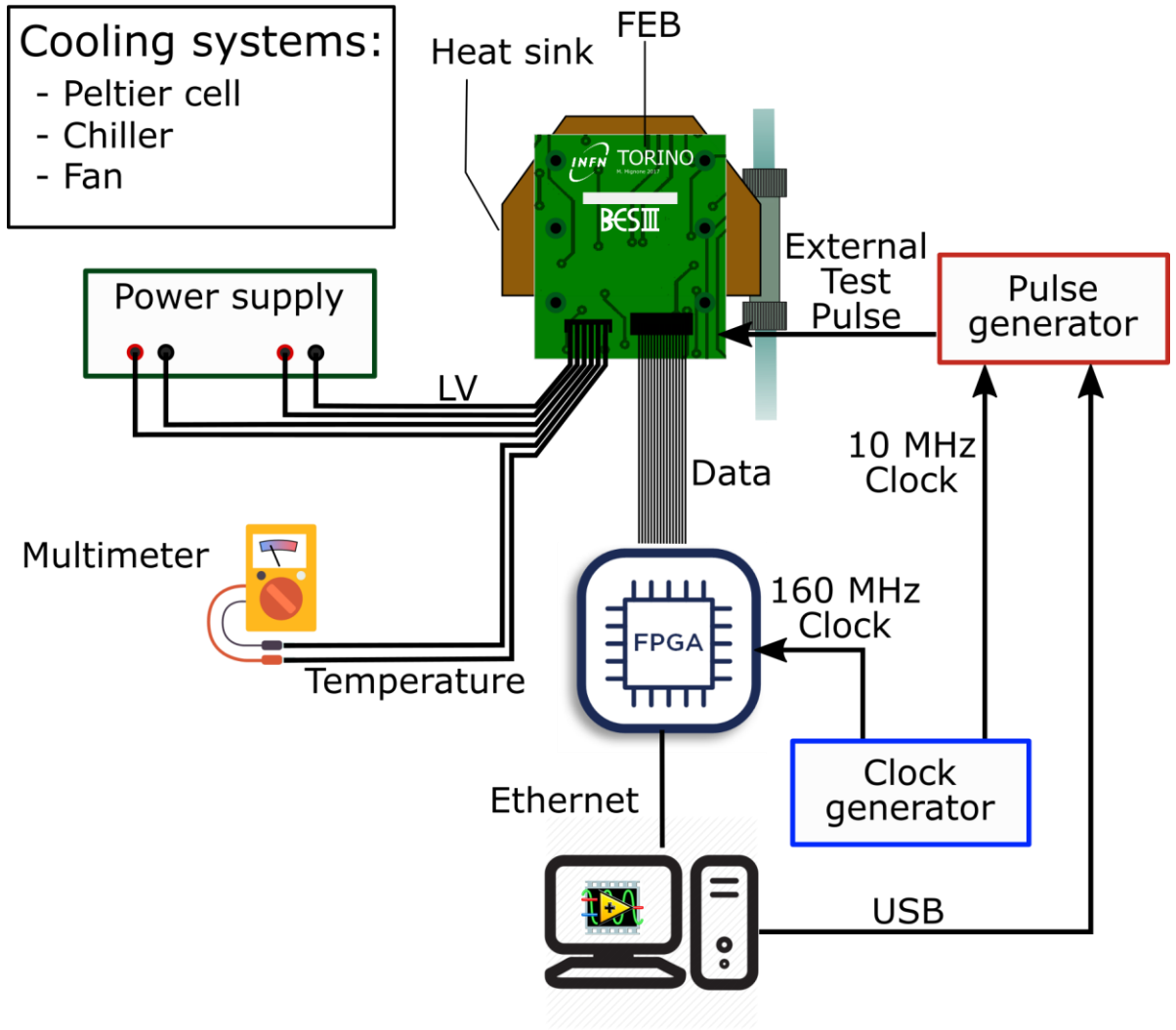
- Complete the integration with the full detector
- Equalize and lower the thresholds
- Optimize the grounding in order to reduce the noise
- Compatibility tests with the MDC are ongoing
- Tracking and efficiency results with the current setup will be presented to the BESIII collaboration soon
- Installation within the end of next year

THANK YOU FOR YOUR ATTENTION

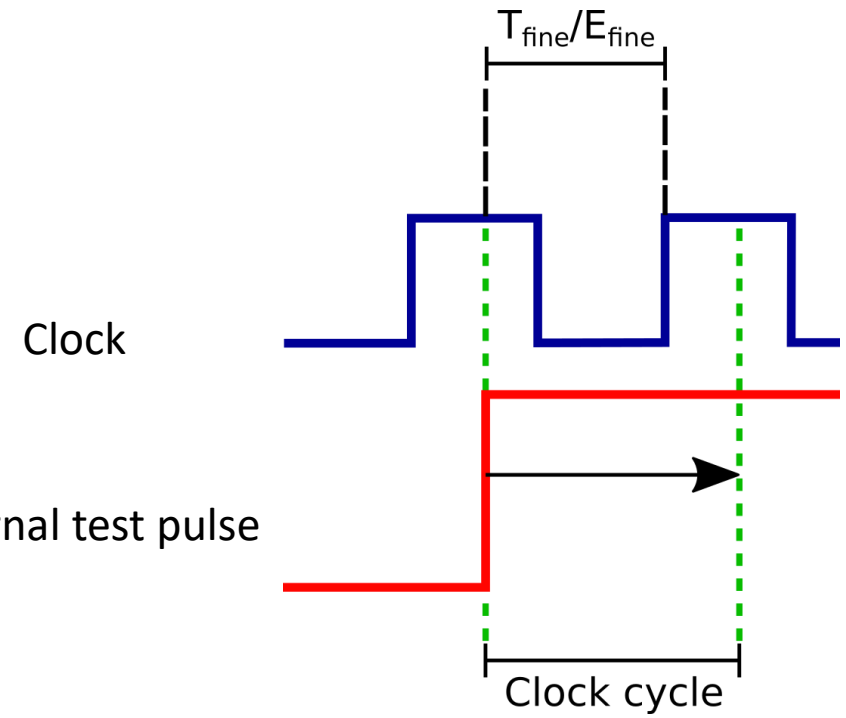
BACKUP SLIDES

Test and calibration setup

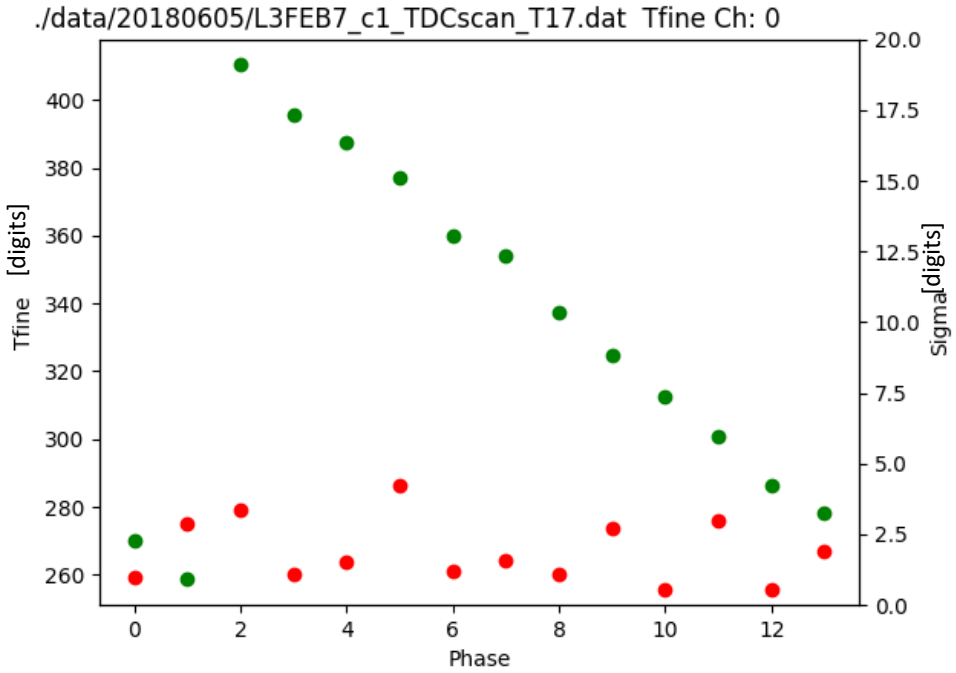


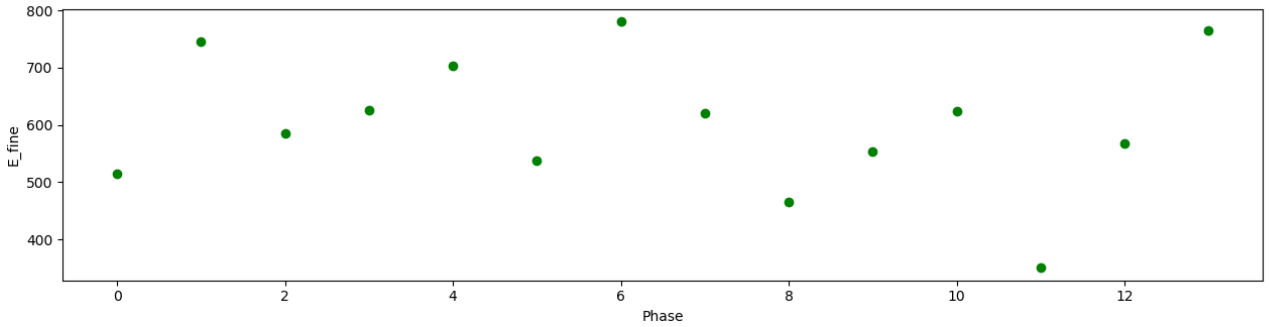


TDC scan

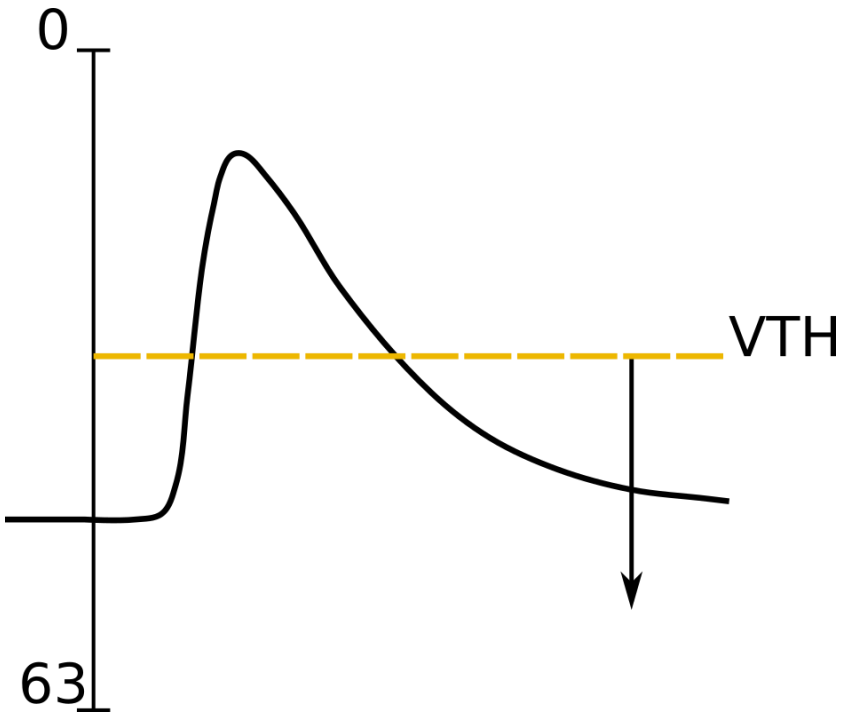


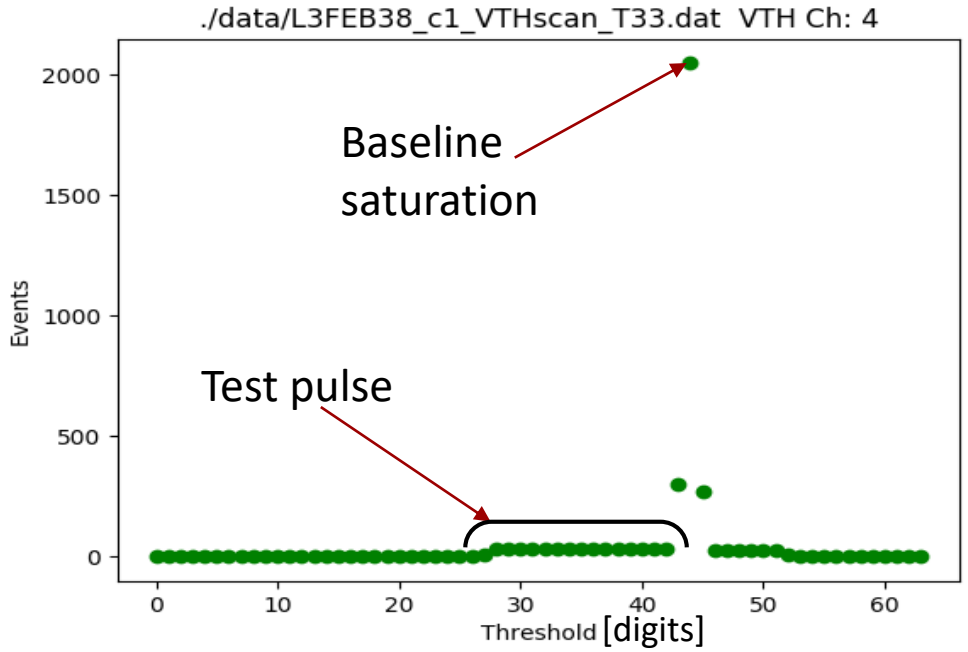
Sweep test pulse phase, along one clock cycle,
to scan TDC response

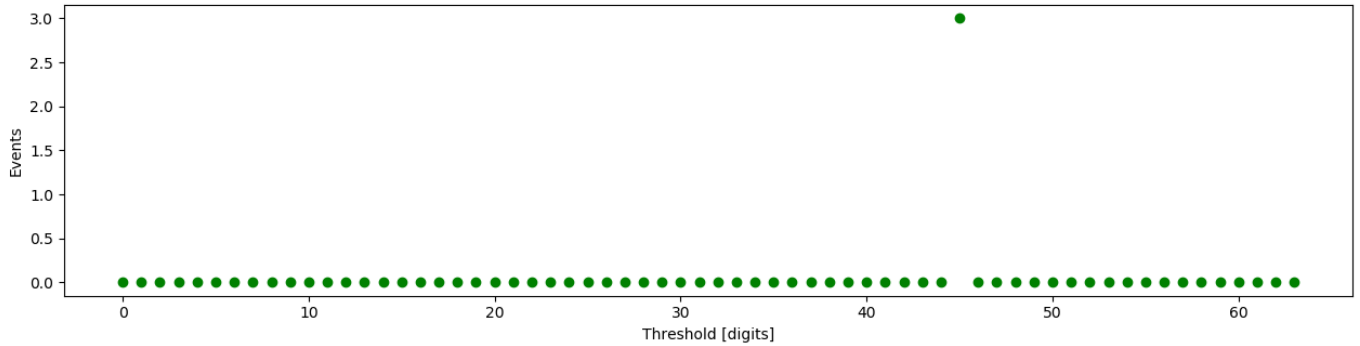




Threshold scan

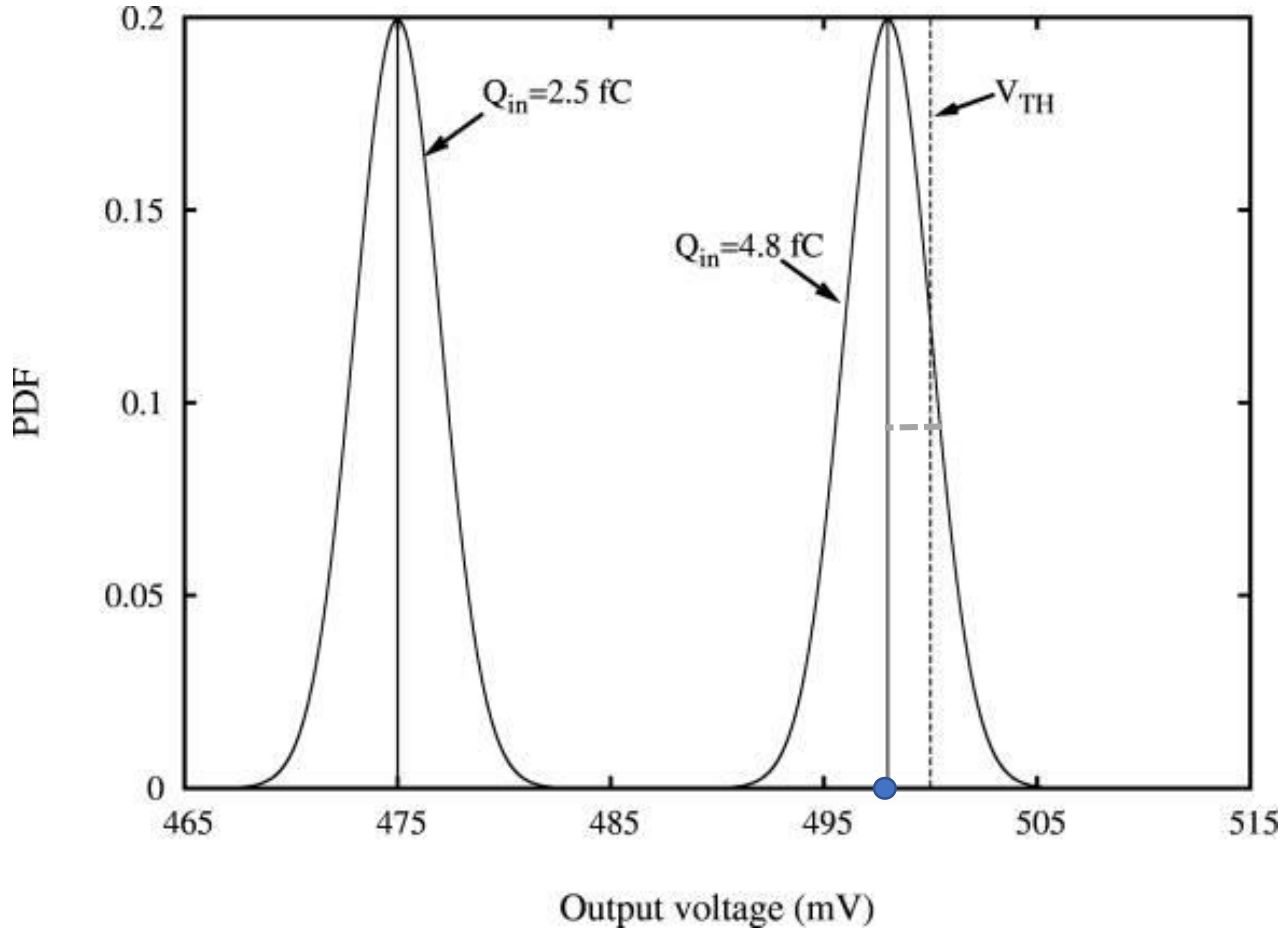




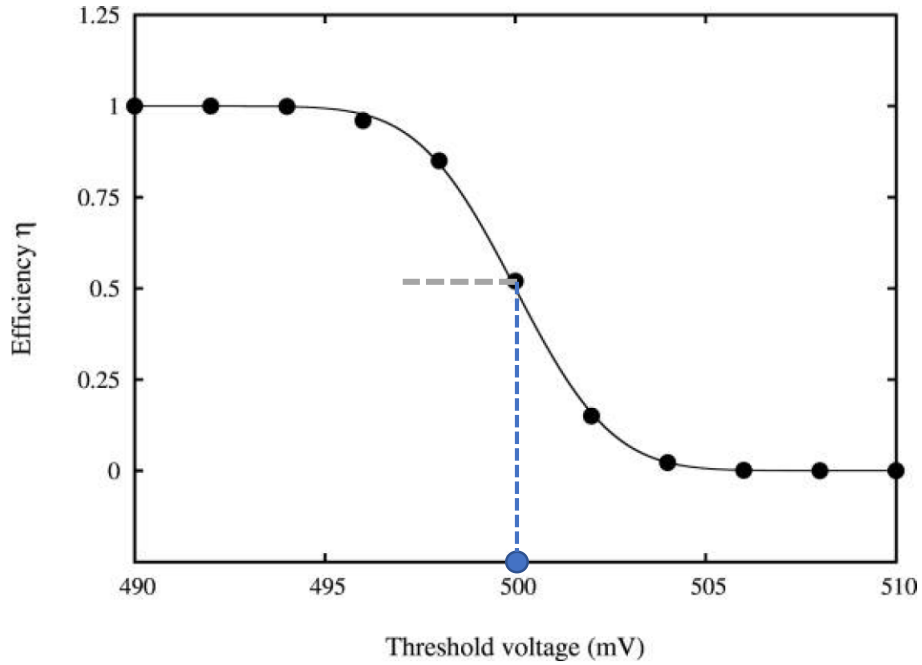


Sweep threshold value to test front end behavior and measure baseline and noise

S-CURVE FITTING



$$\eta = \frac{\text{Number of answers}}{\text{Number of sent signals}}$$

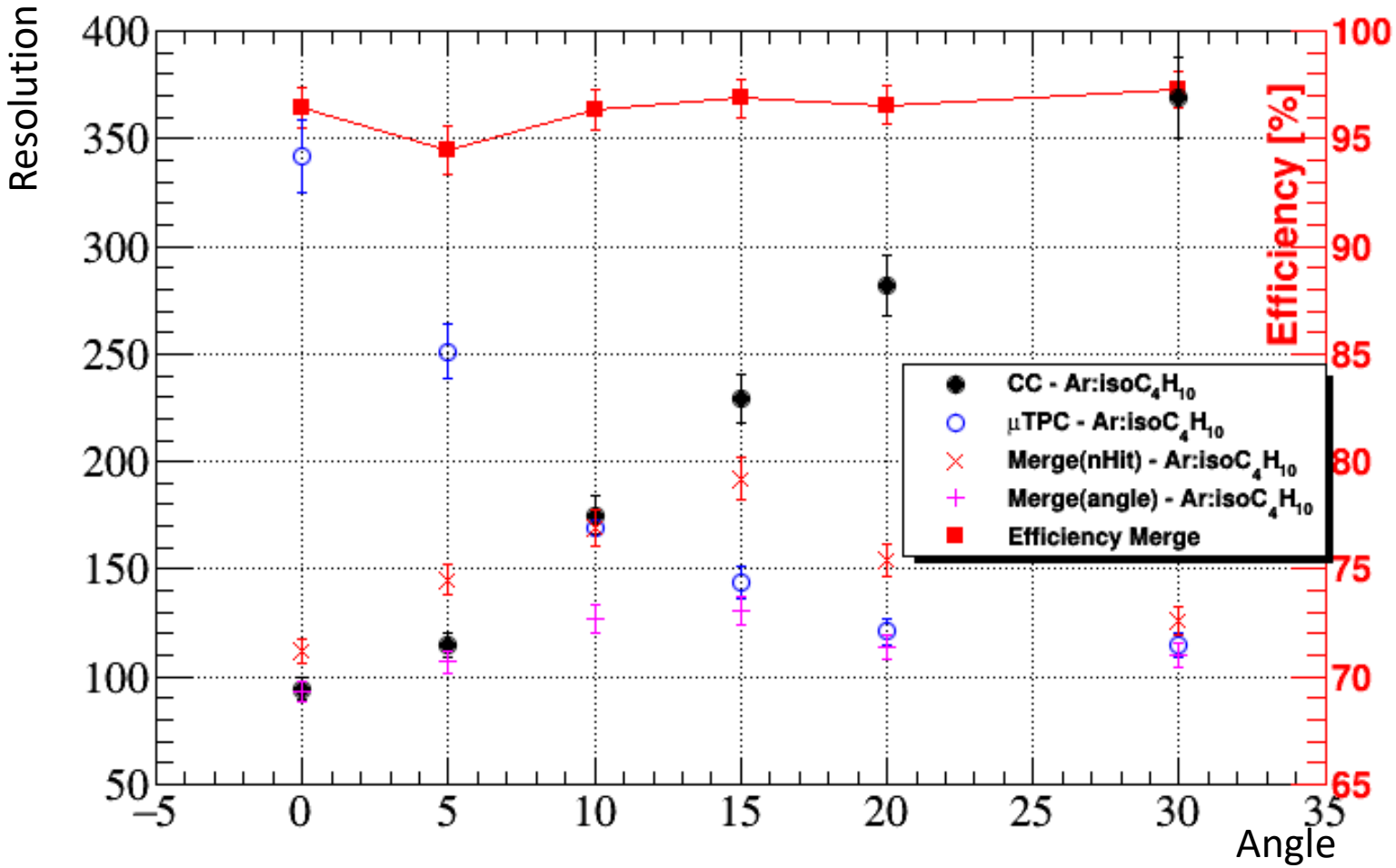


$$\eta(Q) = \frac{1}{2}\left[erf\left(\frac{Q-\mu}{\sqrt{2}\sigma}\right)+1\right] \qquad (1.45)$$

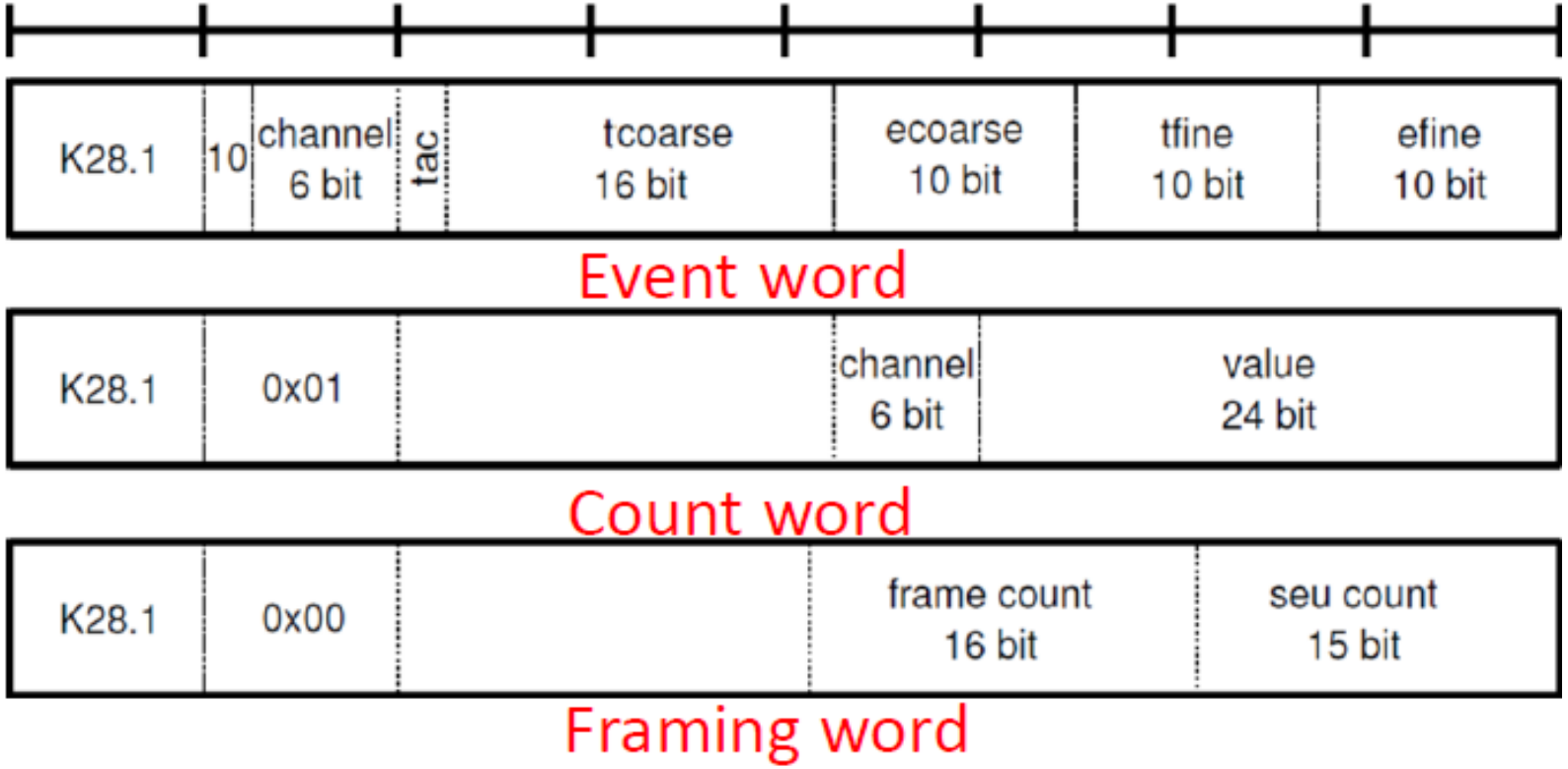
Reference: A. Rivetti CMOS **Front-End Electronics for Radiation Sensors**

Merging

Two different merging procedures, integrated with iterative algorithm

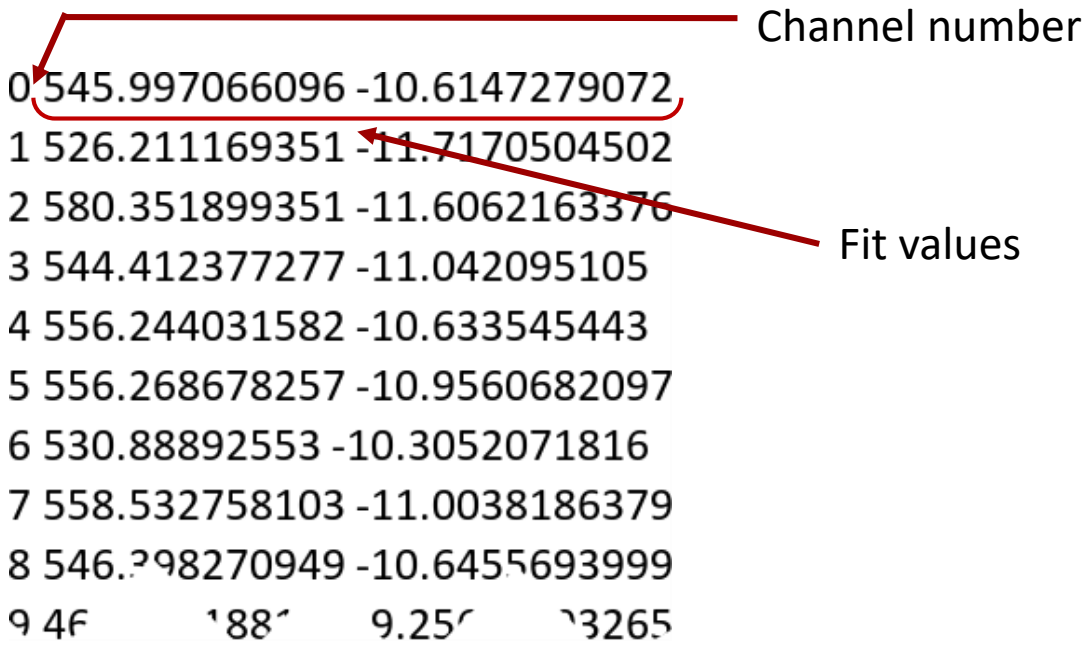


Transmitted words



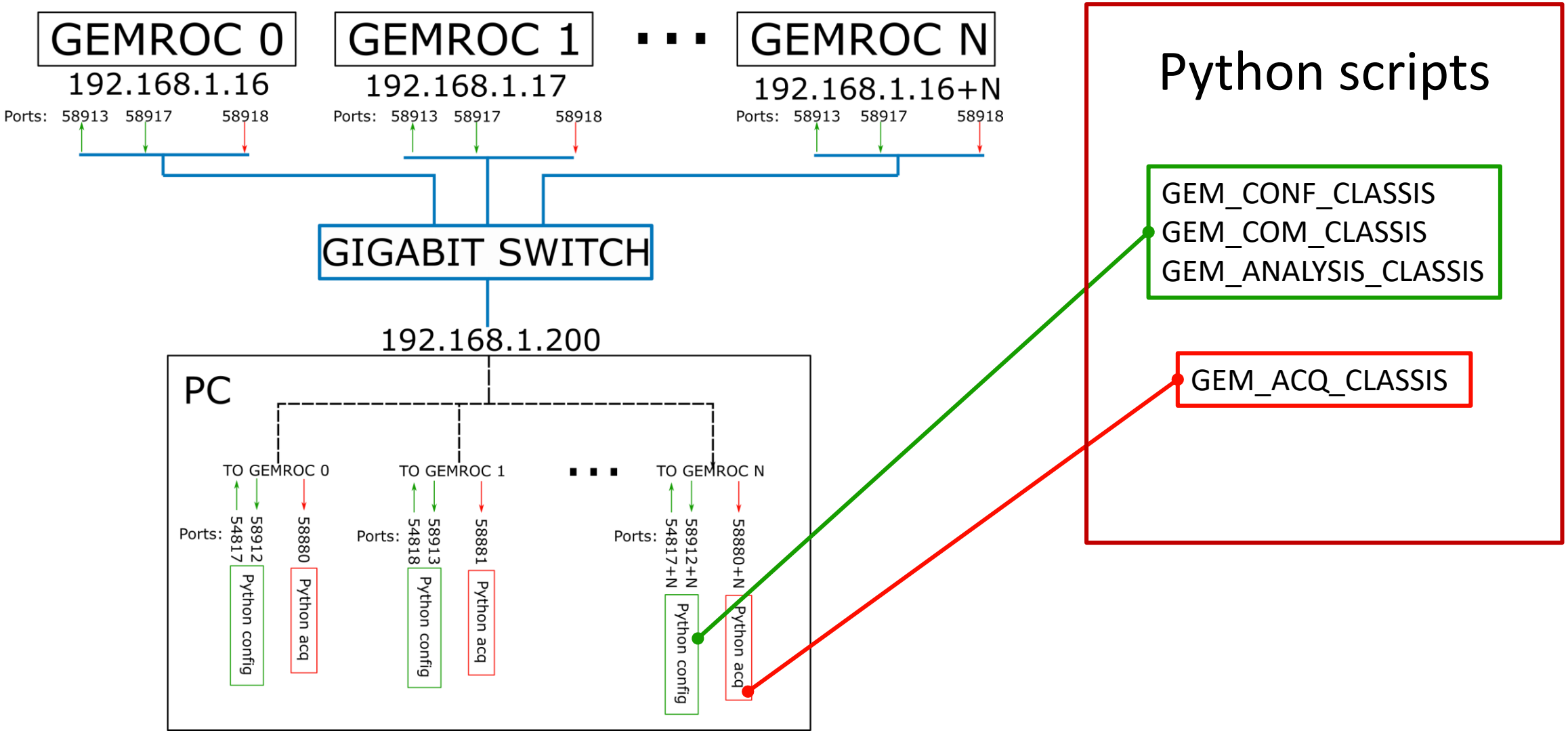
Calibration

- Calibration of both S&H and ToT needed to compensate offset between the 64 channels
- The number of chips made mandatory to implement a fast calibration system



Look up table sample

Network architecture



UDP buffers settings

1. #!/bin/bash
2. sysctl -w net.core.netdev_max_backlog=64000
3. sysctl -w net.core.rmem_max=1677721600
4. sysctl -w net.core.wmem_max=1677721600
5. sysctl -w net.core.rmem_default=1677721600
6. sysctl -w net.core.wmem_default=1677721600
7. ifconfig enp2s0f1 txqueuelen 100000
8. ethtool -G enp2s0f1 rx 2047

- Line 1 makes the script executable.
- Line 2 changes the backlog size. The backlog is a buffer where the incoming data from the interface card are stacked waiting for the CPU to read the content of the packets, recognize the protocol used and route the packets into the correct buffer, there is one backlog buffer for each core.
- Lines from 3 to 6 increase the size of the buffers allocated for each socket created by the Python script for both incoming and outgoing data.
- Line 7 increases the length of the transmission queue at the kernel level. In this stack, the data incoming from the socket and going to the interface card are stored.
- Line 8 increases the ring memory allocated on the interface card for the reception buffer.

Procedures

Chip validation (done at T_{amb} and cooled)

- **TDC** scan → functioning of the ASIC TAC and digital back-end
- Fast **Vth scan** →front-end response

Chip calibration

- **TDC scan** → calibration of fine time
- **Vth scan** → thresholds equalization
- **Internal Test Pulse calibration** using external pulse generator on one channel
- Test and **calibrate 64** channels for both ToT and S&H with internal test pulse
- **Python script** to generate calibration references (*FEB id*, *chip id*, *channel id, ADC counts vs Qin*)