SALT, a 128-channel readout ASIC for Upstream Tracker in the LHCb Upgrade

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Outline

- Introduction
- SALT design
  - ➢ Main blocks (FE, ADC, PLL, DLL, DSP)
  - ➢ SALTv3 versus previous versions
- SALT measurements
  - ➢ Analog test channels – scope measurements
  - ➢ SALT on hybrid with sensor type A – full tests with transmission of digitized data
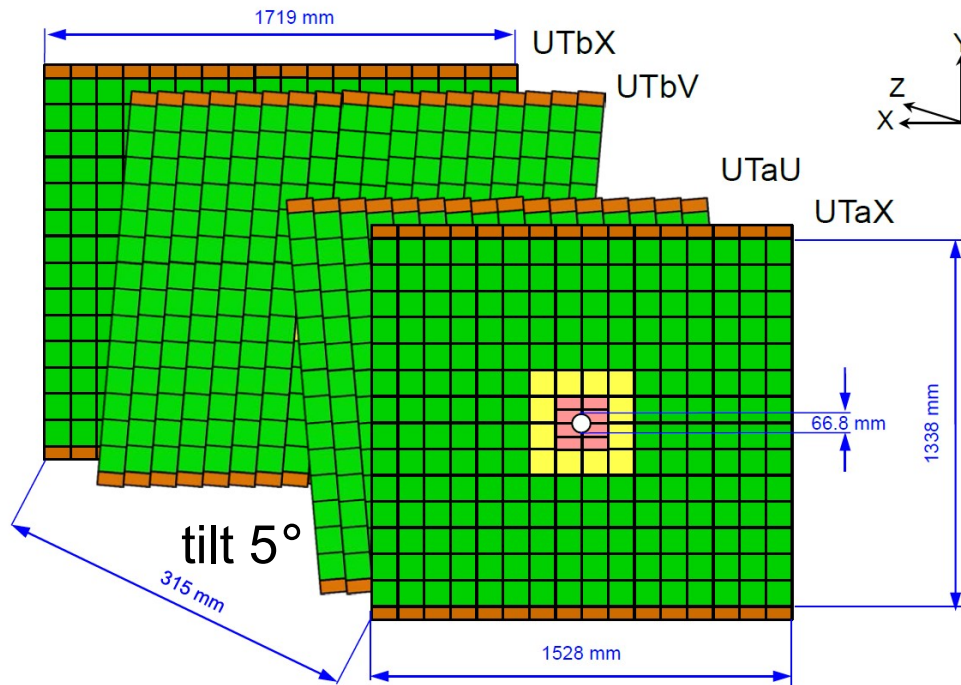- Summary and plans

- Upstream Tracker (UT) replaces the Tracker Turicensis (TT)

- 500 000 silicon strip detector channels

- Readout frequency increases to 40 MHz – *currently Level-0 trigger output is limited to 1MHz*
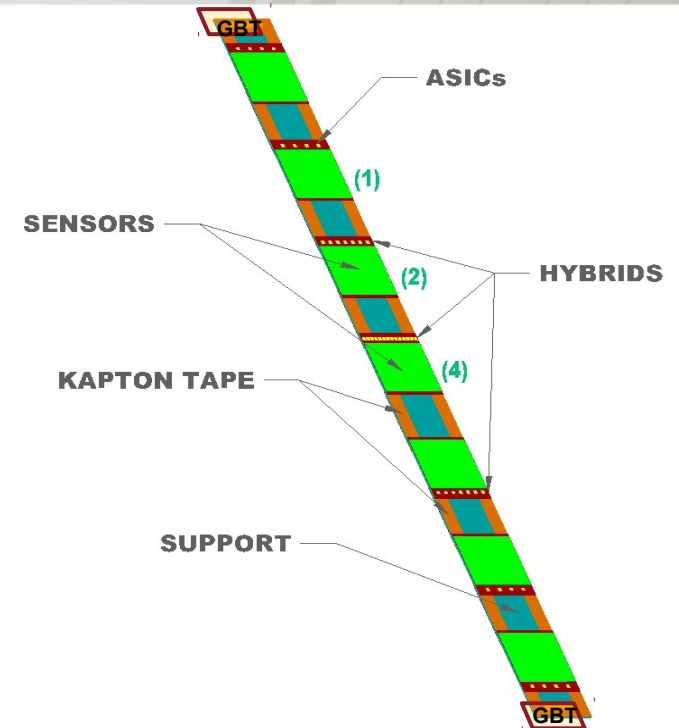
- New readout electronics is needed

UT
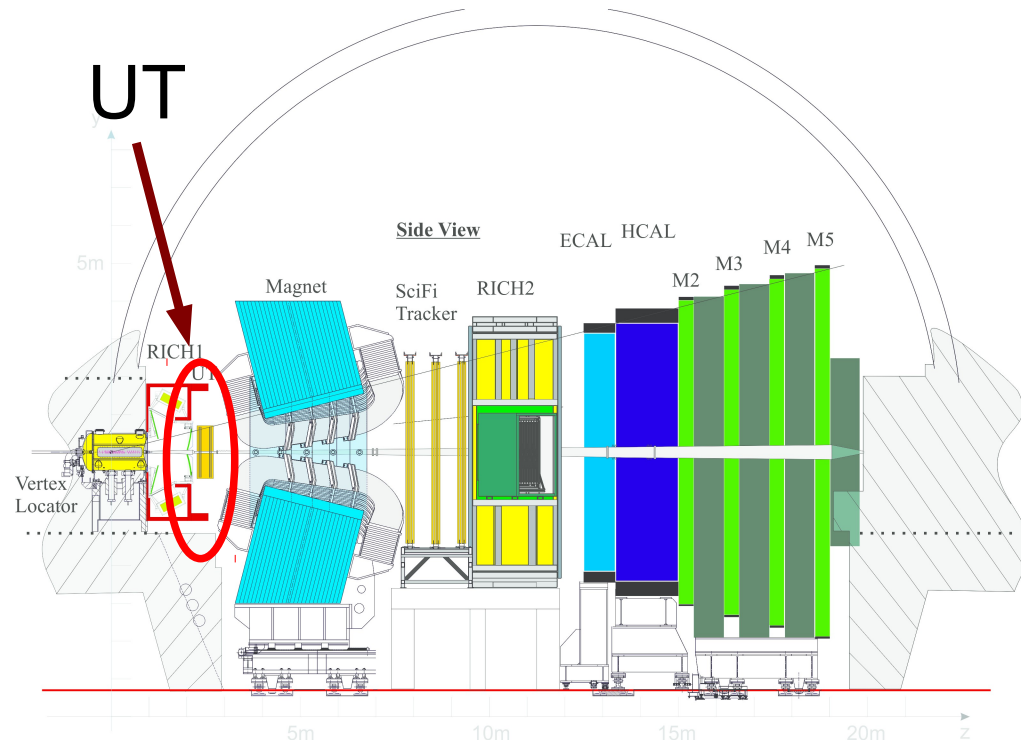
LHCb detector

Introduction
Upstream Tracker (UT)

- 4 silicon strip sensor types
  - p^+-in-n, 10 cm
  - n^+-in-p, 10/5 cm
- ~1000 hybrids with 4 or 8 ASICs

- ~4000 128-channel readout ASICs – SALT
- Data rate depends on position – different number of active e-links in SALT

Introduction
SALT specification

- CMOS 130 nm technology
- 128 channels, Front-end & ADC in each channel
- In/Out pitch 80/140um, No Top/Bottom pads (previous versions) SALTv3 uses it
- Sensor: capacitance 1.6–12 pF, AC coupled
- Both input signal polarities (p^+-in-n and n^+-in-p)
- Input charge range ~30ke−
- Noise: ENC ~1000e− @10pF + 50e−/pF
- Pulse shape: T_{peak} ~25 ns, very short tail: ~5% after $2*T_{peak}$
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit&polarity), 40MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Serialization & Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I2C
- Power < 6 mW/channel
- Radiation hardness ~30 MRad

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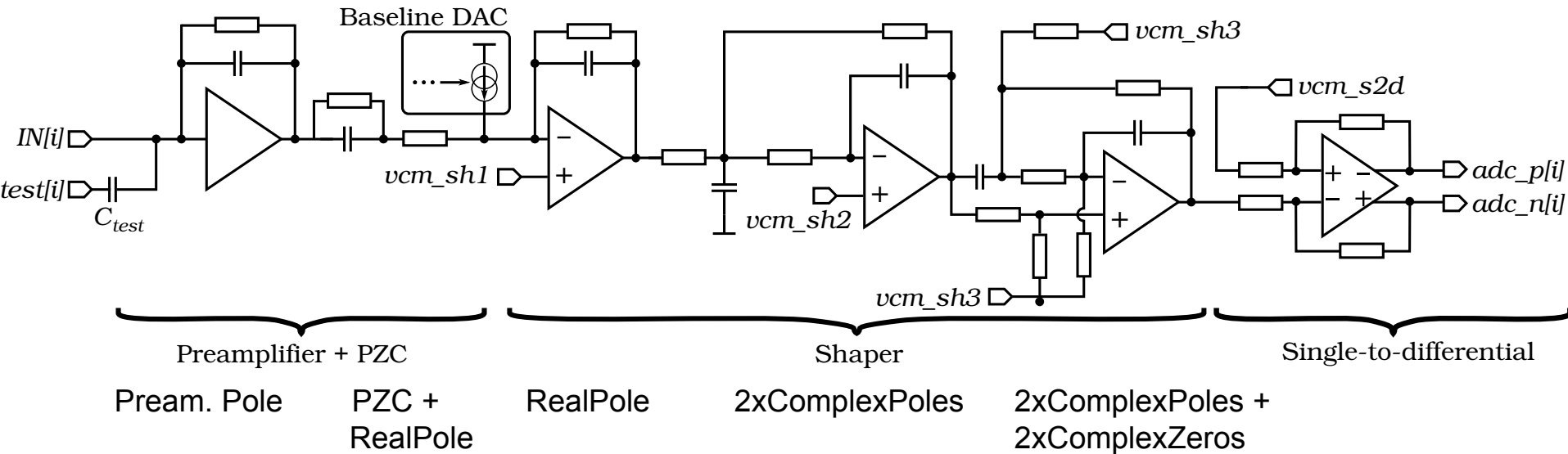# SALT – Silicon ASIC for LHCb Tracking Architecture
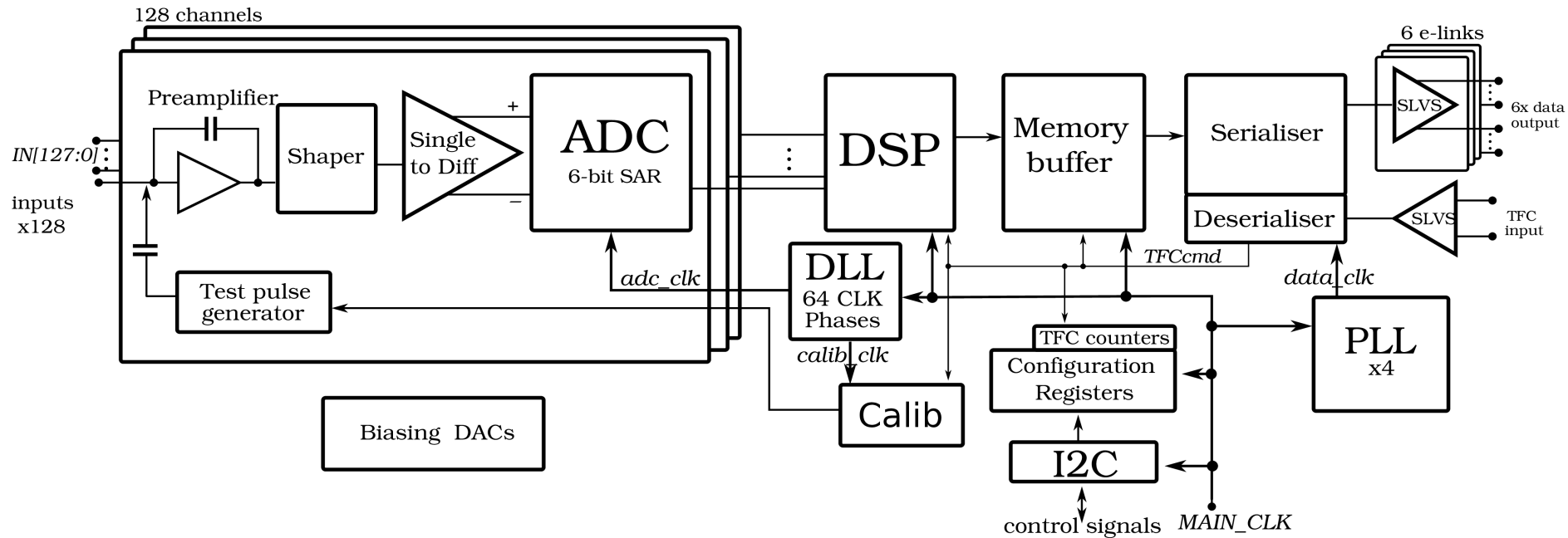
- Front-end & ADC in each channel - 128 standard channels plus 2 test channels (nr -1,128 not shown) with analog outputs
- Digital Signal Processing (DSP) of the ADC data
- And many other features/blocks: PLL, DLL, TFC, I2C, serialiser, SLVS I/O, biasing DACs, monitoring ADCs, ... (not all shown)
- Only key functional blocks are discussed

Simplified circuit diagram

Preamplifier + PZC

Shaper

Single-to-differential

Pream. Pole   PZC + RealPole   RealPole   2xComplexPoles   2xComplexPoles + 2xComplexZeros

- 3-stage shaper (complex poles and zeros) gives the pulse with short tail
- Common mode (vcm_sh) at half power supply for both pulse polarities
- Single-to-Differential converter to generate differential signal for ADC
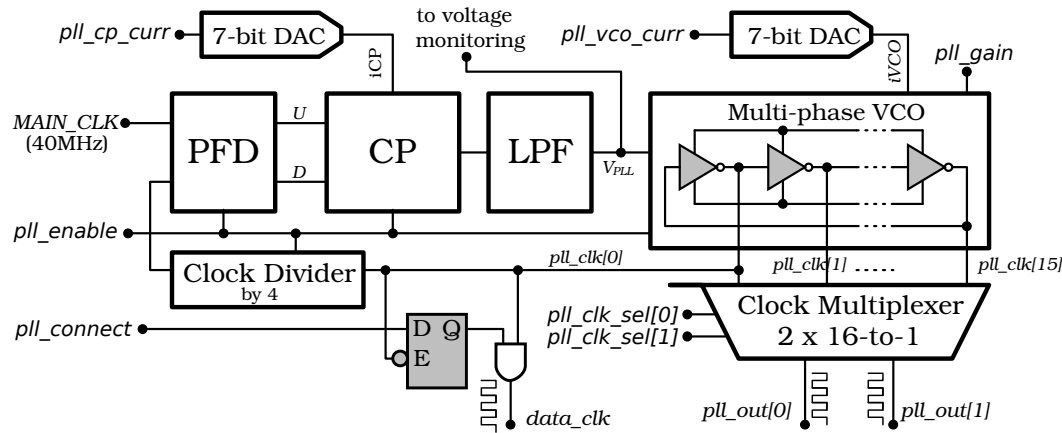- Power consumption: ~1.5 mW

SALT design
6-bit ADC
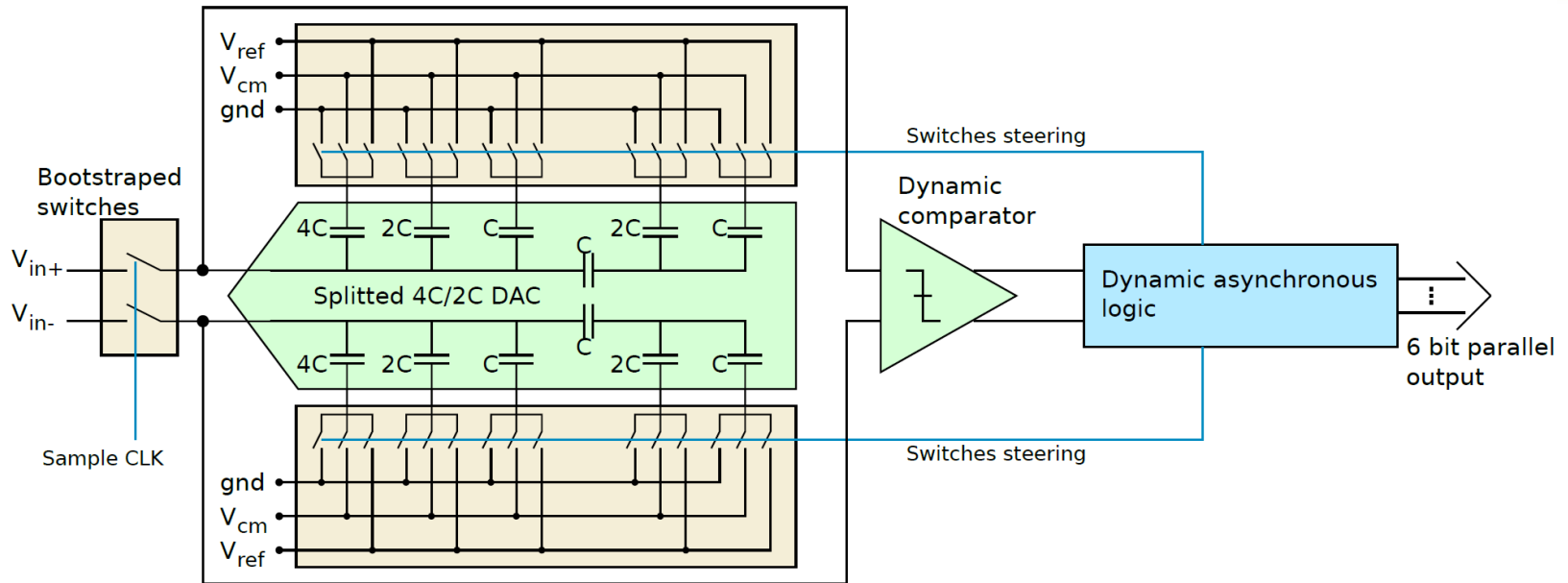
Main features:

- SAR architecture, 6-bit resolution
- 40 MSps nominal sampling rate
- Merge Capacitor Switching (MCS)
- Capacitive DAC with 3b/2b split
- Dynamic comparator
- Dynamic asynchronous logic
- Bootstrapped input switches
- Power consumption ~350μW

Update - dummy current option ON/OFF (const. current after conversion) added (additional ~400uW) to keep current consumption more stable
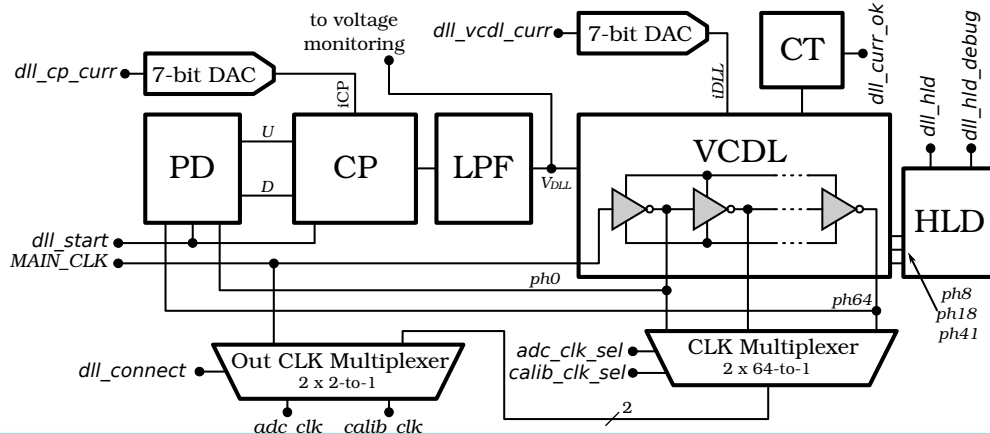
SALT design
PLL, DLL

PLL

DLL

PLL features:

- High frequency (160 MHz) clock for DDR serializer
- Input frequency 40 MHz
- Power consumption ~0.5 mW @ 160 MHz
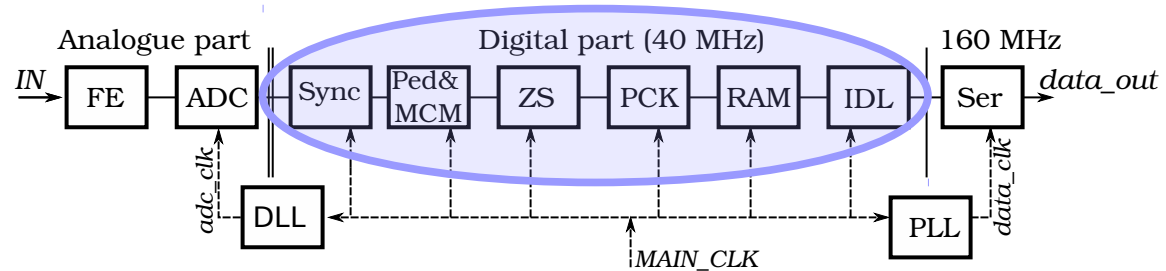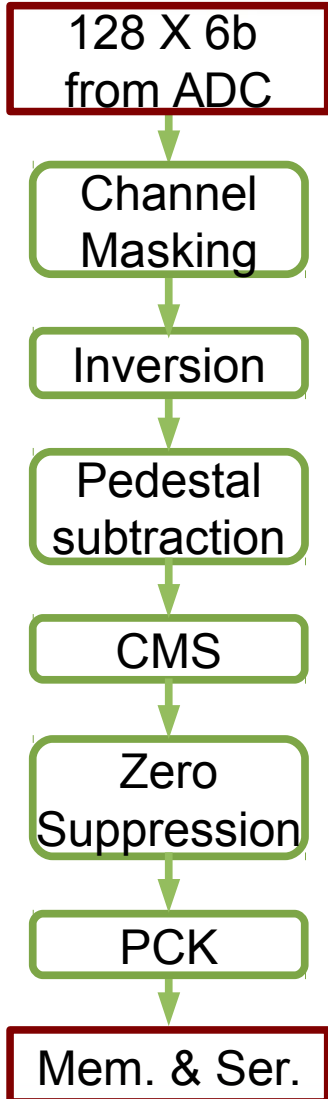- 2 output phases (multiplexing) selected from 16 uniform phases (receiver synchronization)

DLL features:

- ADC sampling phase setting
- Test pulse phase setting
- Input frequency 40 MHz
- Power consumption ~0.7 mW
- 2 output phases (multiplexing) selected from 64 uniform phases

SALT design
DSP operations

128 X 6b from ADC

→ Channel Masking

→ Inversion

→ Pedestal subtraction

→ CMS

→ Zero Suppression

→ PCK

→ Mem. & Ser.

- Input data: 6 bits (5 bits plus sign)
- Noisy or dead channels can be masked
- All channel values can be inverted (1 config bit)
- Pedestal subtraction – subtraction in each channel
- CMS – (Mean) Common Mode Subtraction
  - sum of channels below CM threshold
  - division by number of channels – average
  - subtraction in each channel
- ZS – Zero suppression
  - only channels above ZS threshold are sent out
- PCK – Packet building

- Measurements showed that SALTv2 did not fulfil specification:
  - main issue – 40MHz disturbance observed as baseline shift, when sensor connected

- We have attributed the unsatisfactory SALTv2 performance mainly to large internal inductances (L) of power distribution lines and their couplings (amplifying the effects of large ADC current fluctuations)

- These inductive effects were not seen in simulations of SALTv2 since design tools extract from the layout only R,C but not L

- Contrary to previous SALT prototypes, SALTv3 was designed and simulated basing, NOT on layout-extracted chip, but on mix of schematic-extract with power distribution inductances added

- List of main modifications in next slide...

- Single Channel
  - ➢ Analog front-end – highly improved PSRR
  - ➢ ADC - dummy current option added to minimize current fluctuations
  - ➢ Power supply domains separation optimized for inductive effects
  - ➢ Decoupling of analog supply removed to minimize LC factor
- Power distribution network
  - ➢ Analog front-end supplied from **top&bottom** pads (issue for 8-chip hybrid),
  - ➢ ADC supplied from **digital domain mesh** (output side)
  - ➢ Layout of analog power distribution drawn to minimize inductances

4095um x 10900um
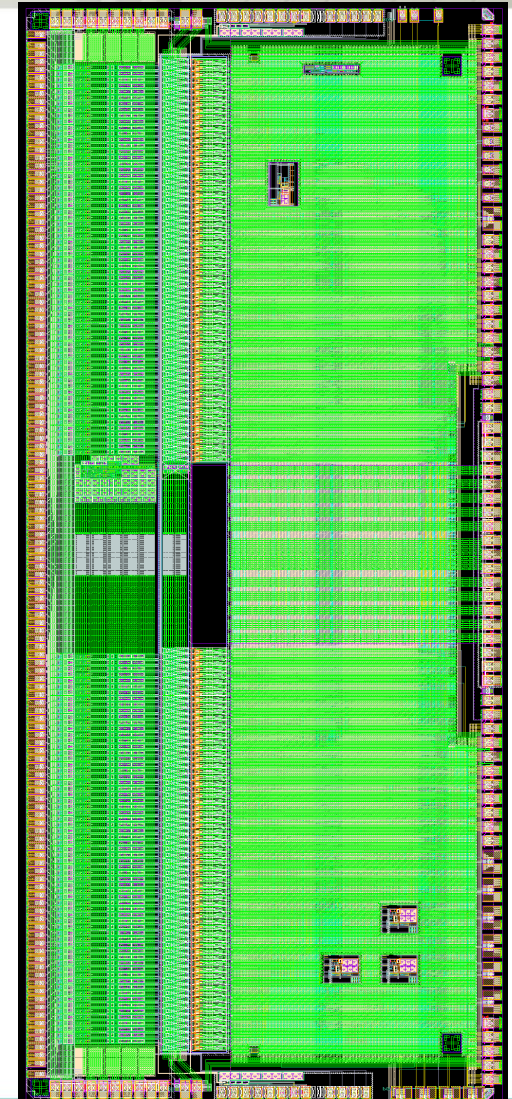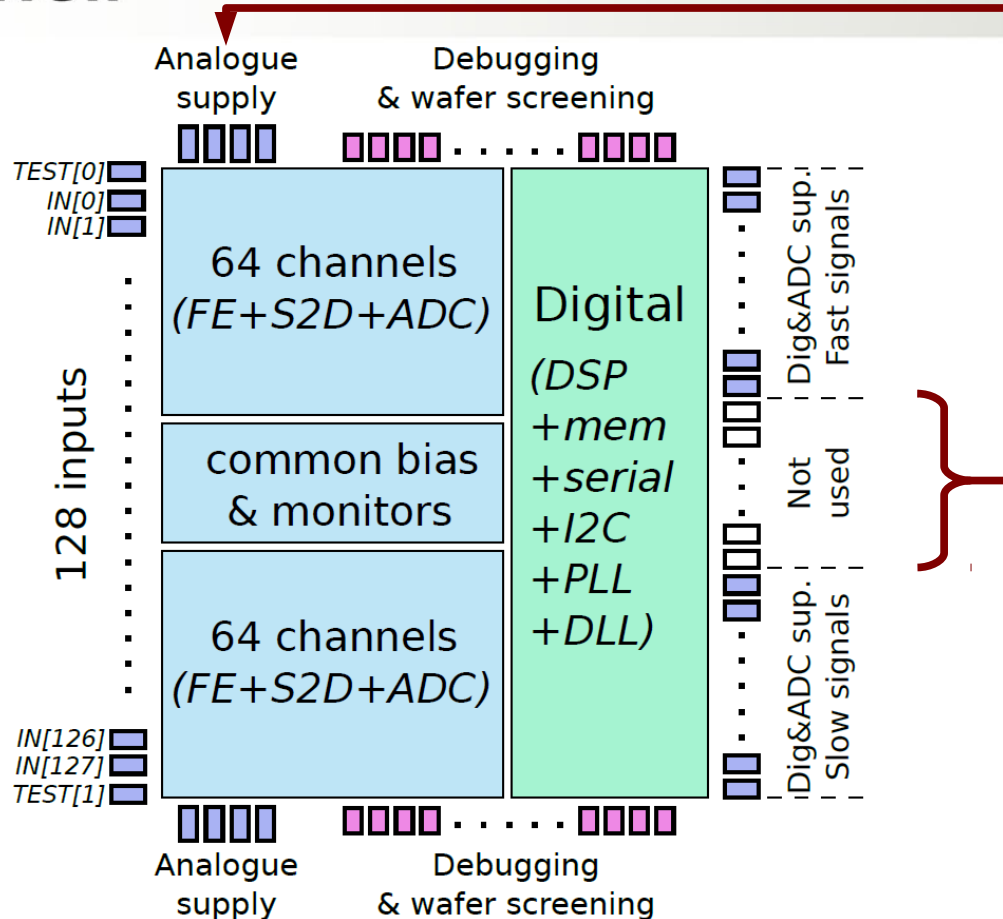
- Left & right sides bonded to the hybrid.
- **Top&bottom pads for analog supply** (issue for 8-chip hybrid) and wafer screening

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Measurements on analog test channel Transient response to MIP (~4fC) with 12pF external input capacitance
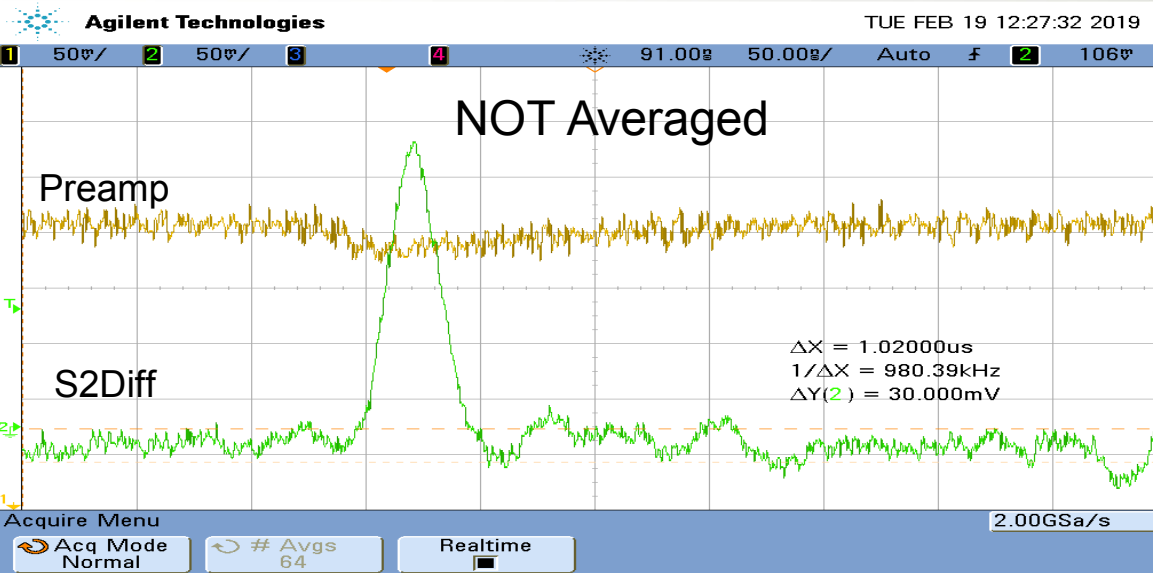
For SALTv3 good pulse response is seen with large input capacitance.
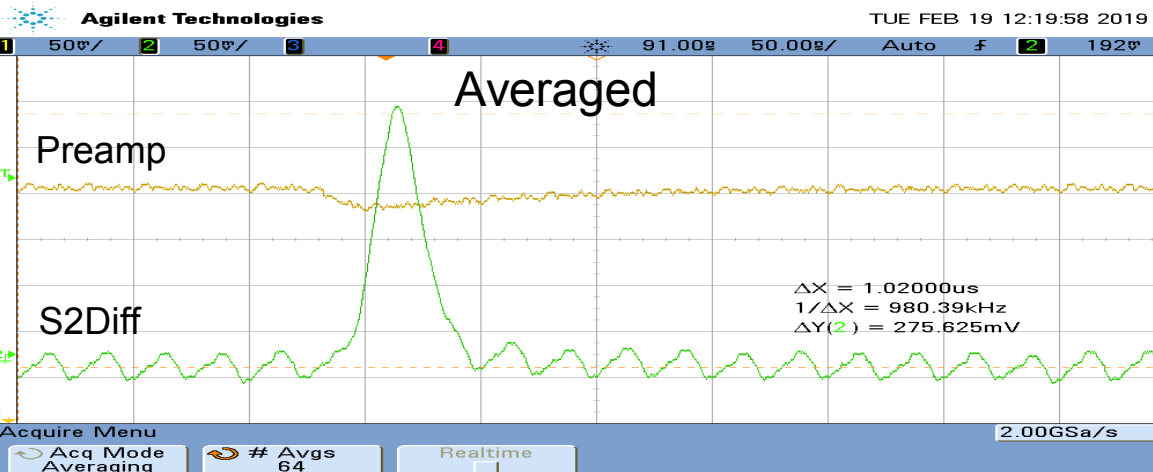
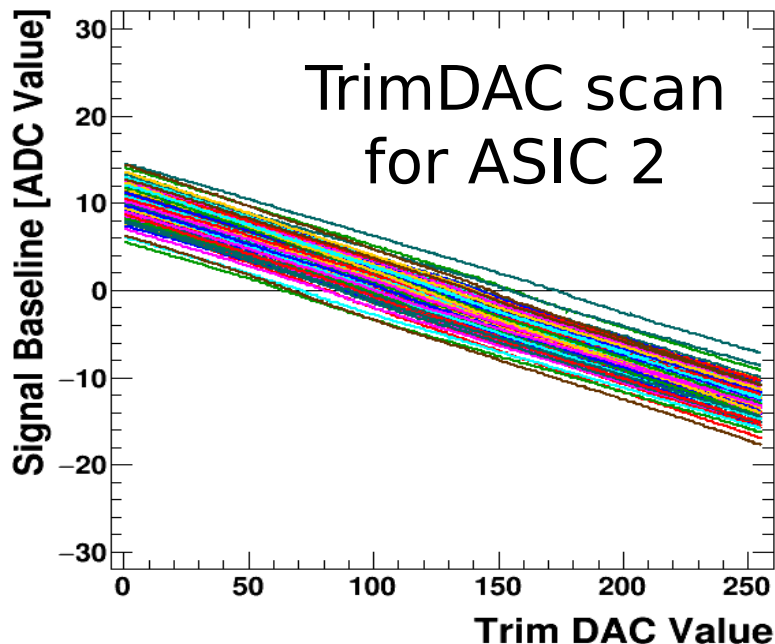

With large input capacitance small 40MHz disturbance is still present (also in simulations)

Setup

- Cdet=12pF
- Dummy current ON
- Default biasing

SALTv3 – $V_{peak-peak}$ at Preamp. and Single-to-Diff (S2D)
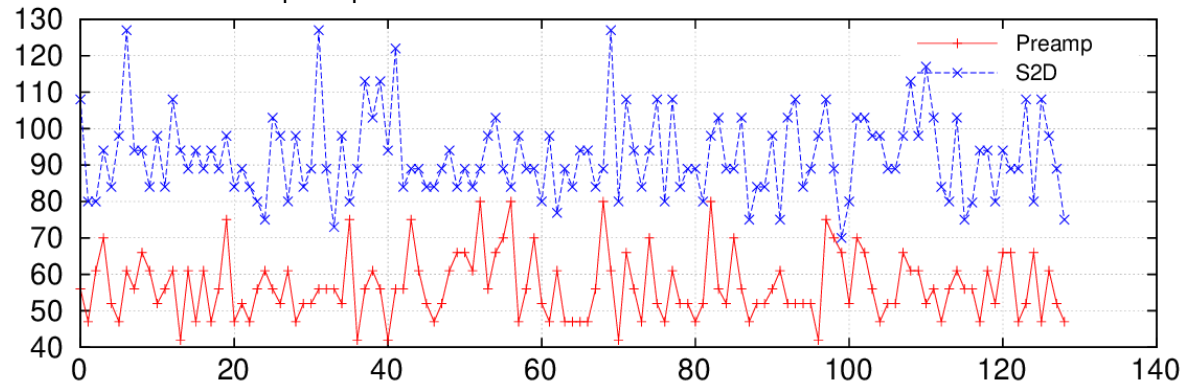
SALTv2 – Preamp. and S2D $V_{peak-peak}$
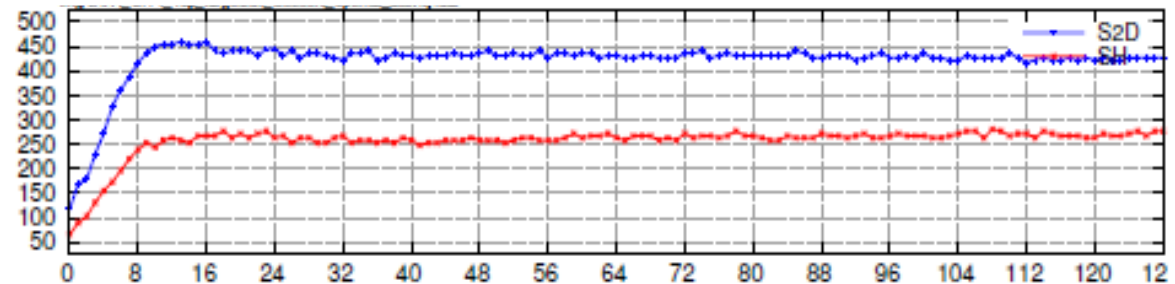
In SALTv3 the baseline $V_{peak-peak}$ (disturbances + noise) does not depend on number of working ADCs, contrary to SALTv2 where 40MHz oscillations saturated already for 8 ADCs ON

SALTv3

baby2 sensor
Cdet<2pF/strip
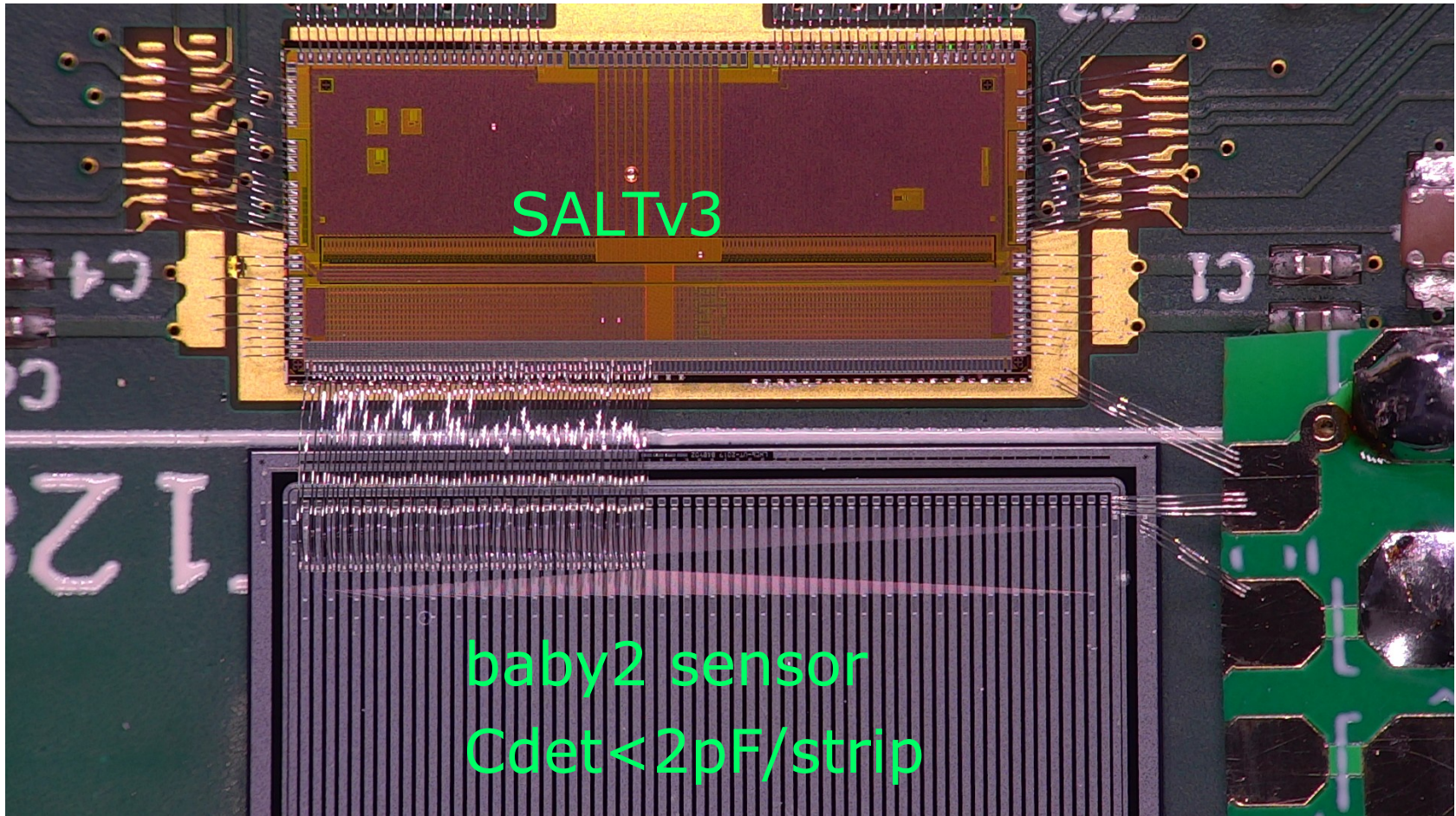
PCB with "baby2" sensor bonded to SALTv3

Measurements on analog test channel Transient response to MIP (~4fC) HV=200V, Dummy current ON
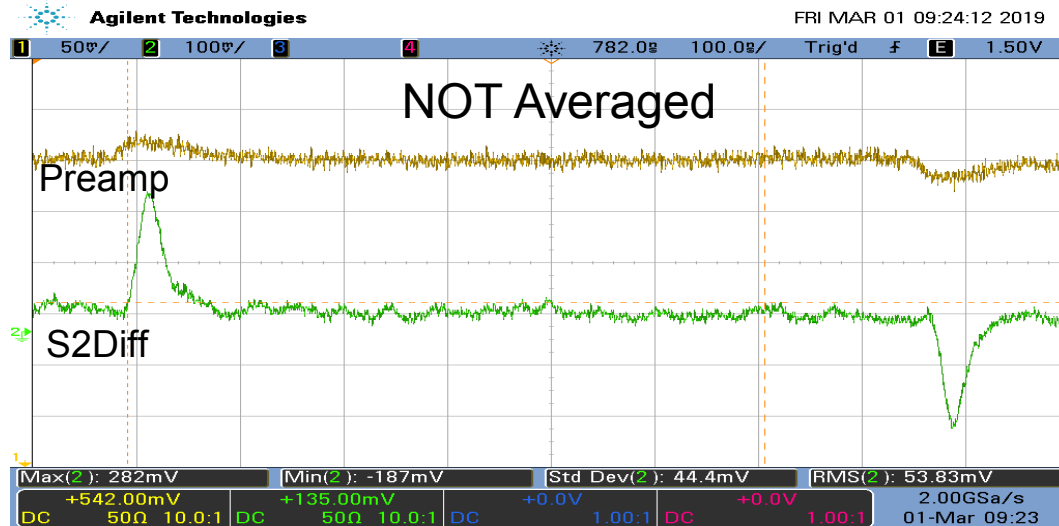
In SALTv3 good pulse response is observed with "baby2" sensor connected
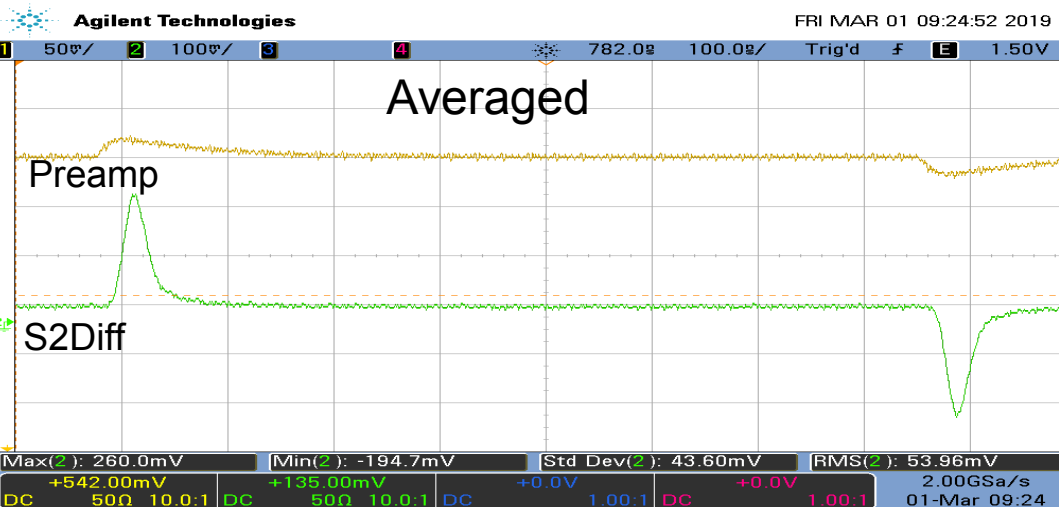
With "baby2" sensor connected 40MHz disturbance is practically NOT observed

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ASIC 0

ASIC 1

sensor type A

~12pF/strip

biased @200V

ASIC 2

ASIC 3
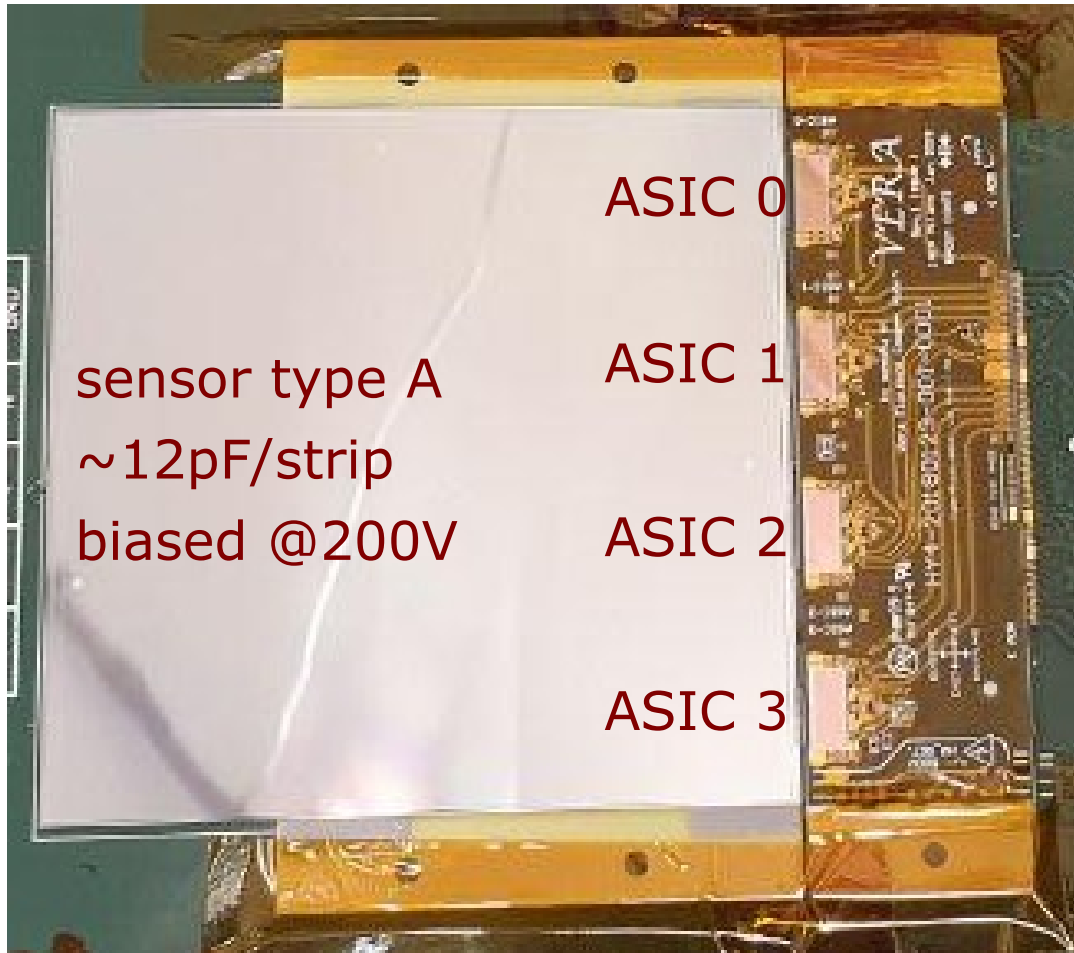
SALT power consumption (@Vsup=1.2)

- ~440mA (dummy current OFF)
- ~480mA (dummy current ON)

Hybrid with the largest sensor and 4 SALT ASICs

TrimDAC scan for ASIC 2

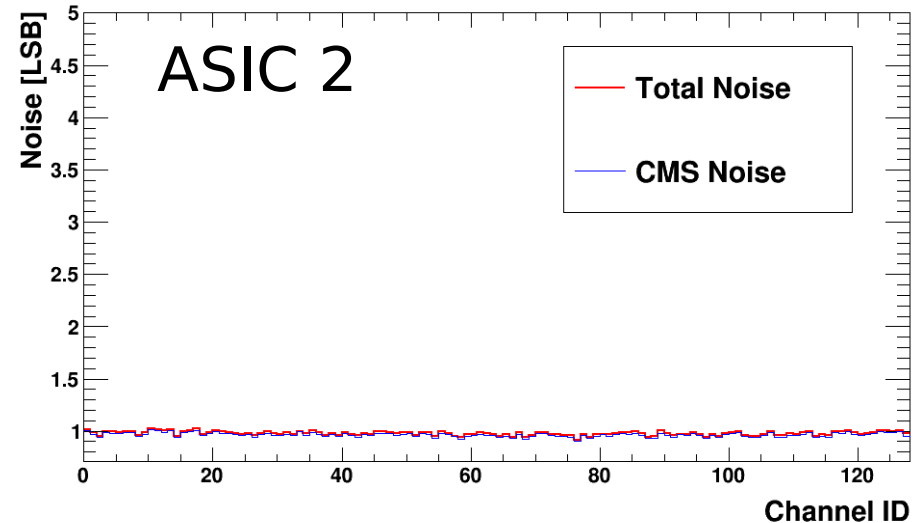Each channel is corrected by setting its own TrimDAC

ASIC 2 before correction

ASIC 2 after correction
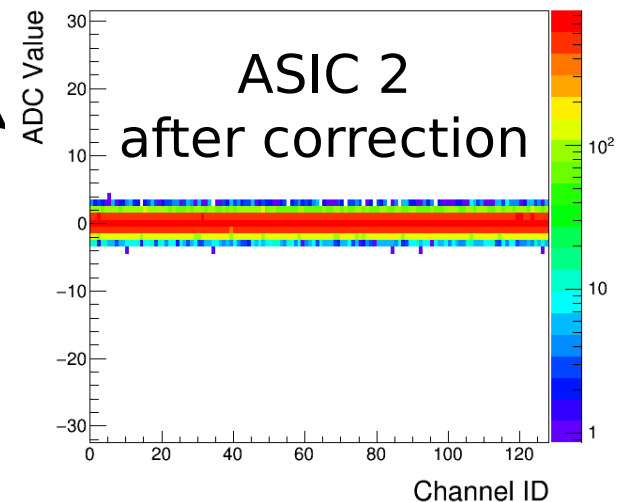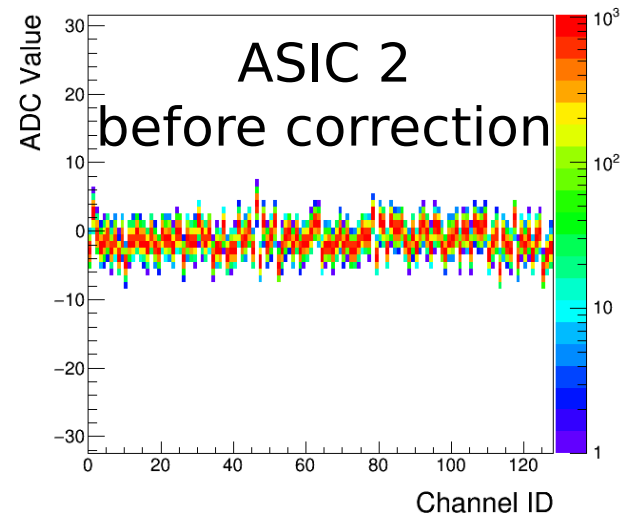
- Baseline correction works well
- Obtaining such data confirms that full processing chain (analog&digital) is functionally correct

SALT on hybrid with sensor type A Noise

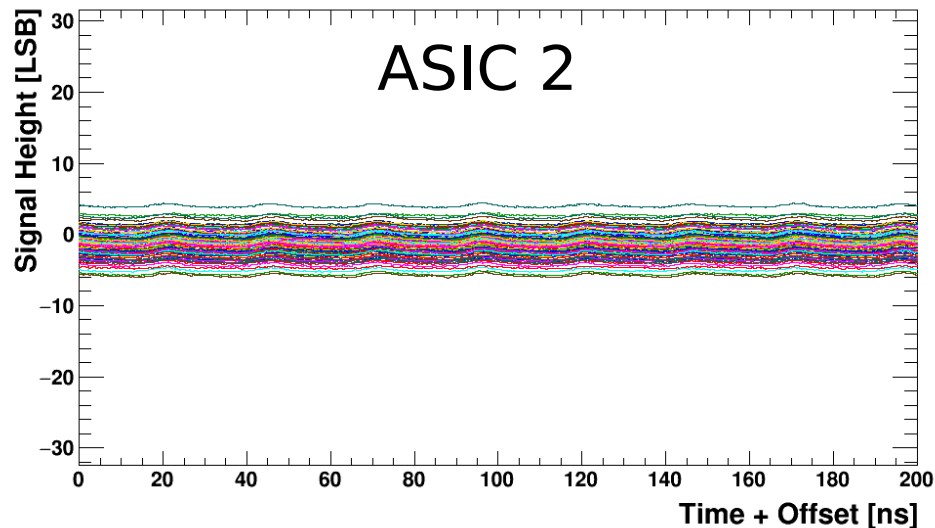Before TrimDAC correction
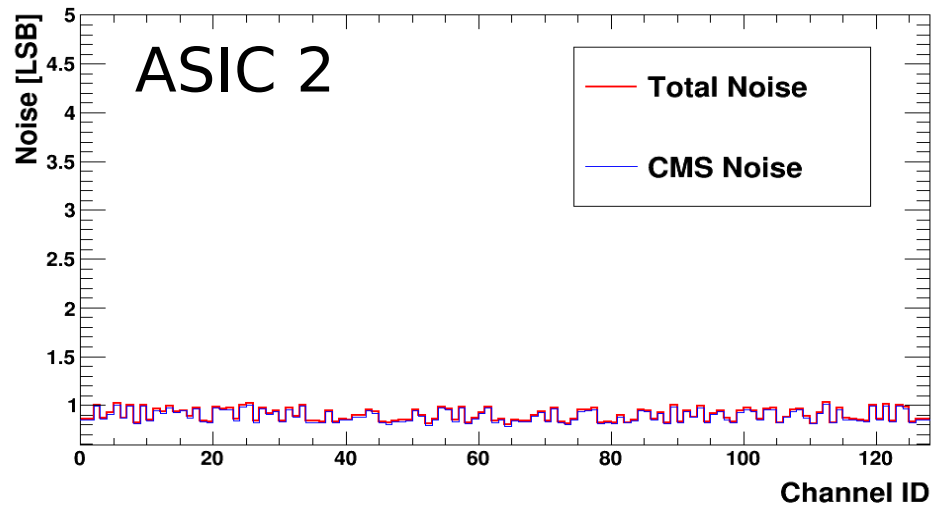
After TrimDAC correction

- Various measurements showed noise rms slightly below 1 LSB
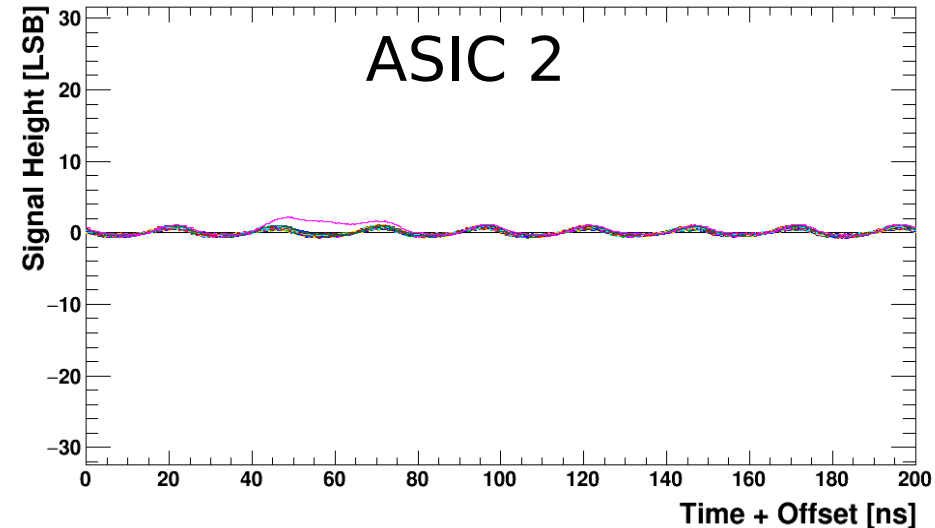- SNR above 10 is estimated for MIP
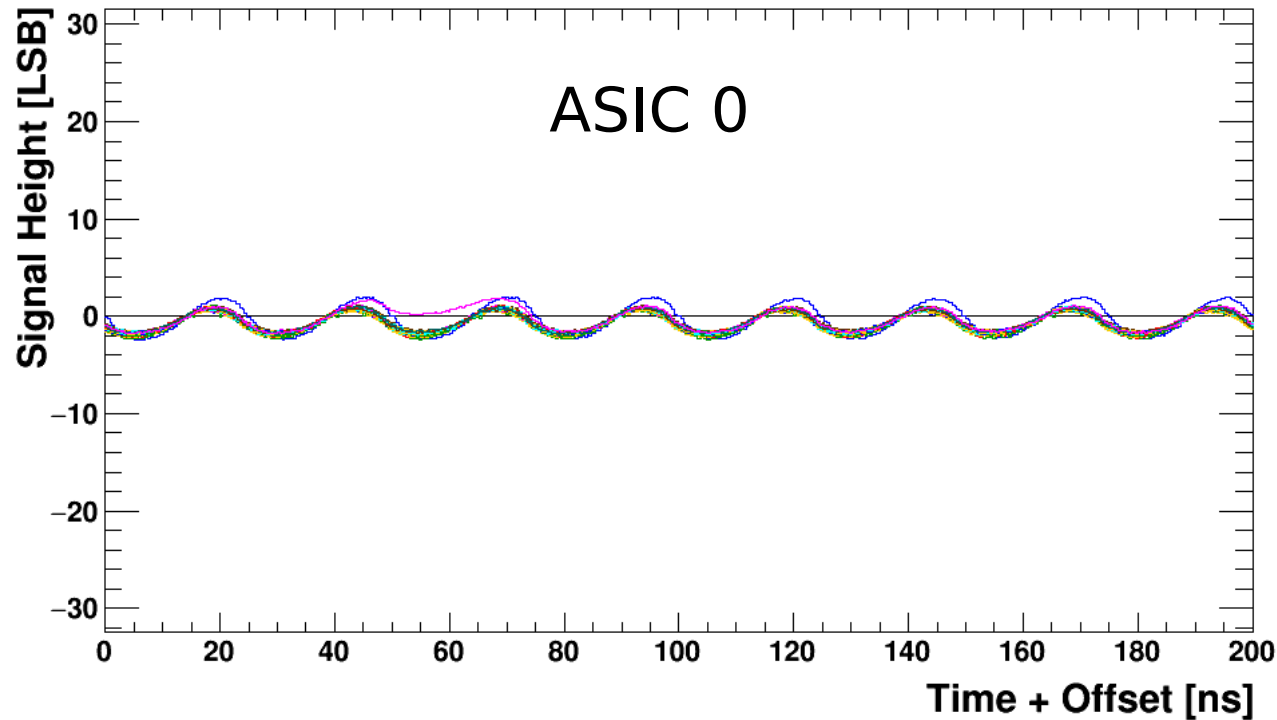
Before TrimDAC correction

After TrimDAC correction

- In standard operation samples are taken every 25ns
- To obtain above plots internal DLL was scanned over all 64 phases ($\Delta t = 25ns/64$) and data was averaged for each phase
- In standard operation small 40MHz component is seen as constant offset and can be subtracted

SALT on hybrid with sensor A
Baseline versus time
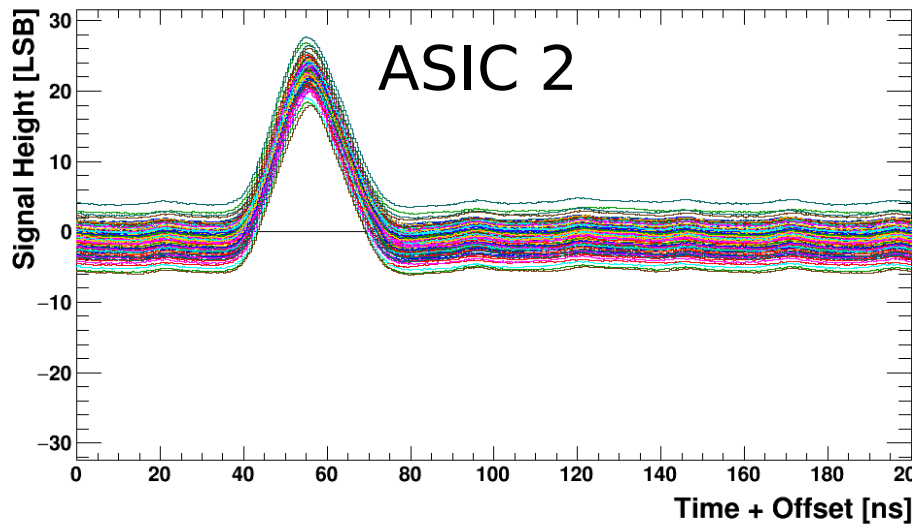
After TrimDAC correction

ASIC 0

- In hybrid the worst 40MHz disturbance is seen in position "0"
  - ➢ Hybrid design (sensor biasing) is crucial for SALT performance
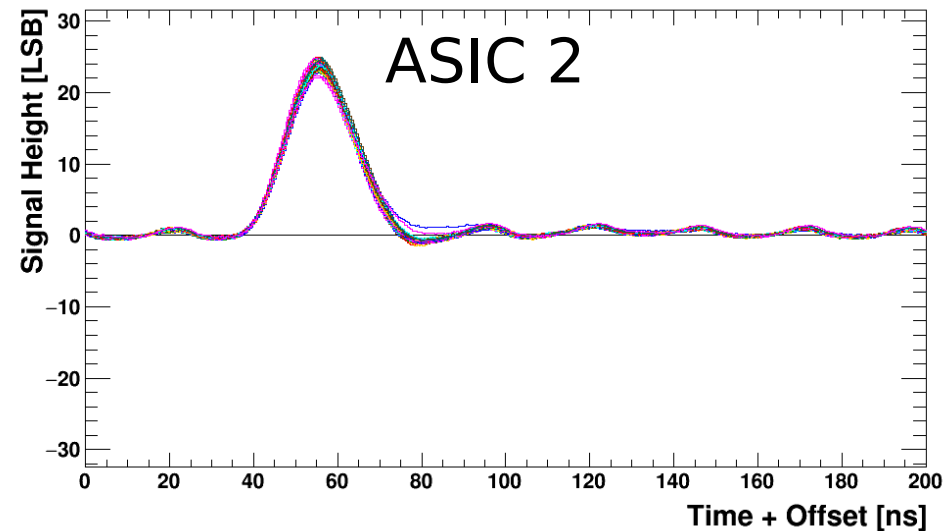- In standard operation 40MHz disturbance is removed as offset

Before TrimDAC correction

After TrimDAC correction

ASIC 2

ASIC 2

- Pulse shape is obtained via DLL scan
- Expected pulse shape is observed

- The third SALT prototype was fabricated and tested. The tests confirmed that the measures taken against suspected inductive issues have proved effective

- Good results have been obtained for 4-chip hybrid. Full stave tests have been already started

- SALT production for 4-chip hybrids have been recently completed, wafer tests done, analysis of results ongoing

- For 8-chip hybrid a modified SALT version (without using top&bottom pads for power supply) is in fabrication. Will be checked a.s.a.p.
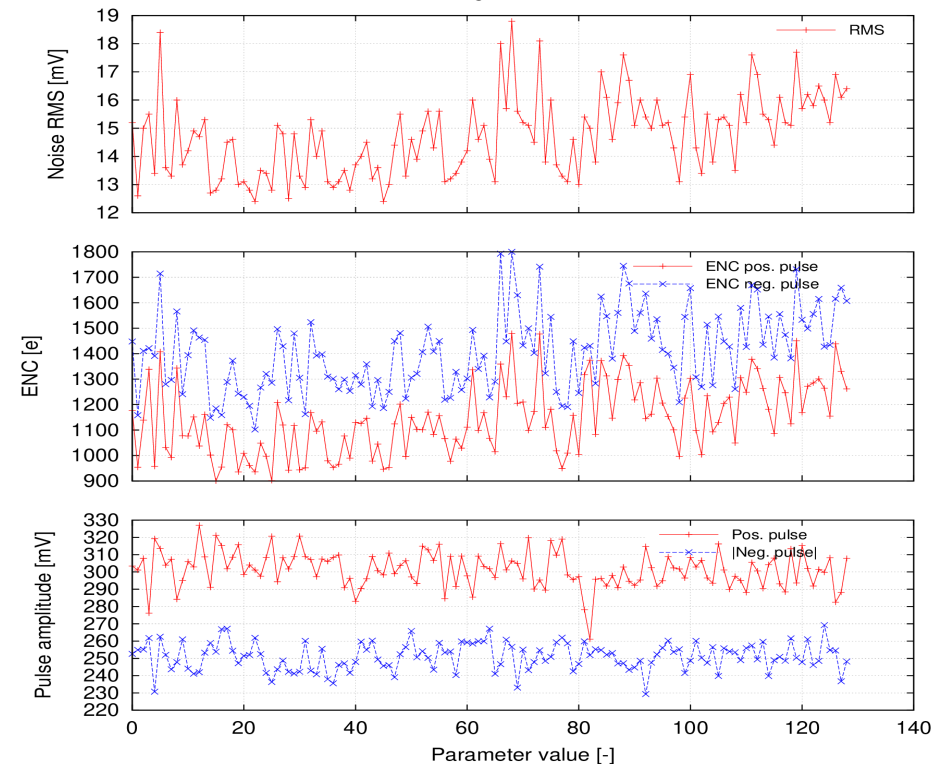
# *Thank you for attention*

Backup
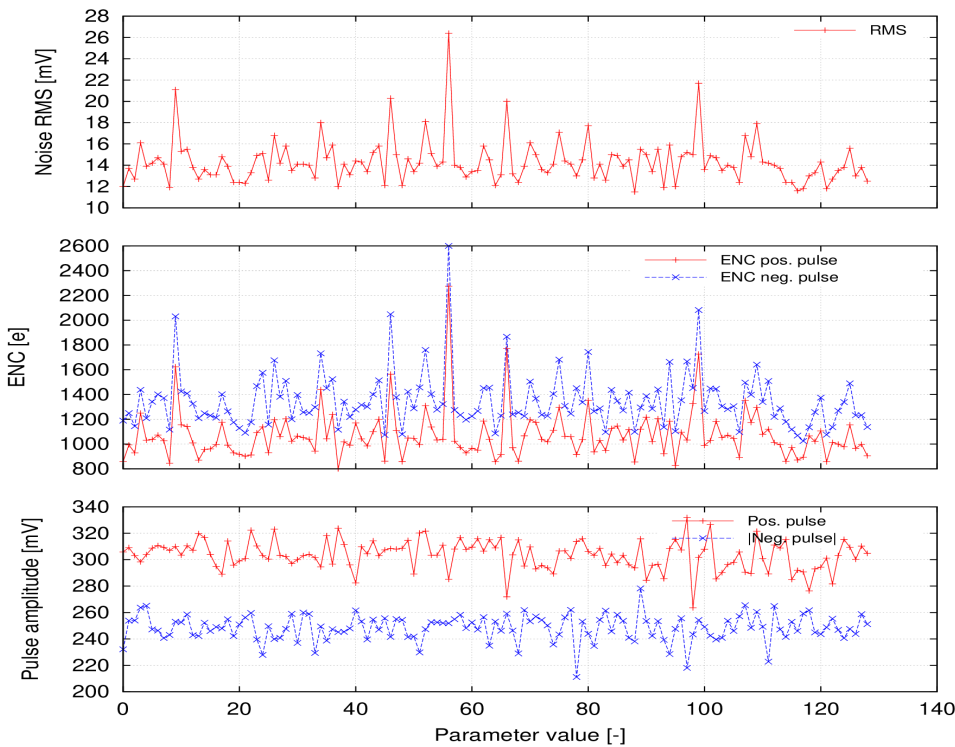
Dummy current ON

Dummy current OFF

Satisfactory noise performance and good SNR (MIP pulse Cdet=12pF) observed with dummy current ON
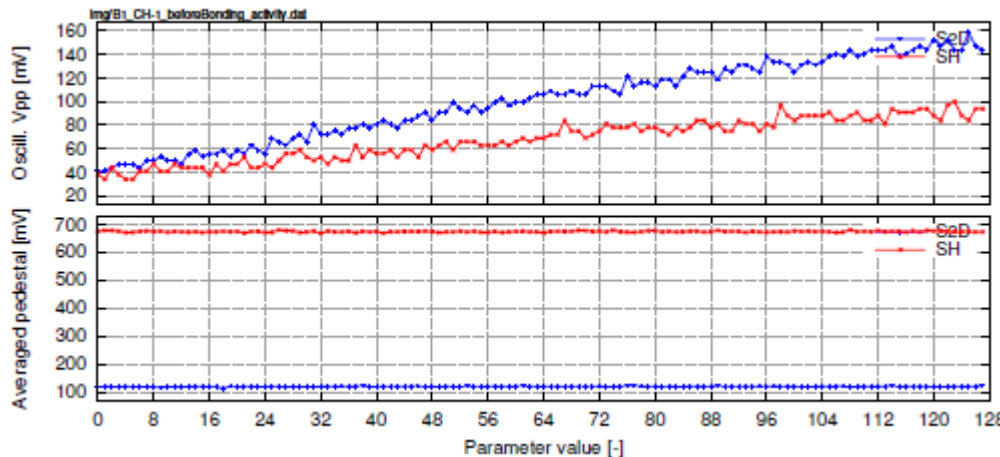
Bare chip, NO capacitance
Vpp & baseline vs no. ADCs ON for chan. 128

Pulse shapes for bare chip are not shown since for each prototype nice pulses were observed without input capacitance

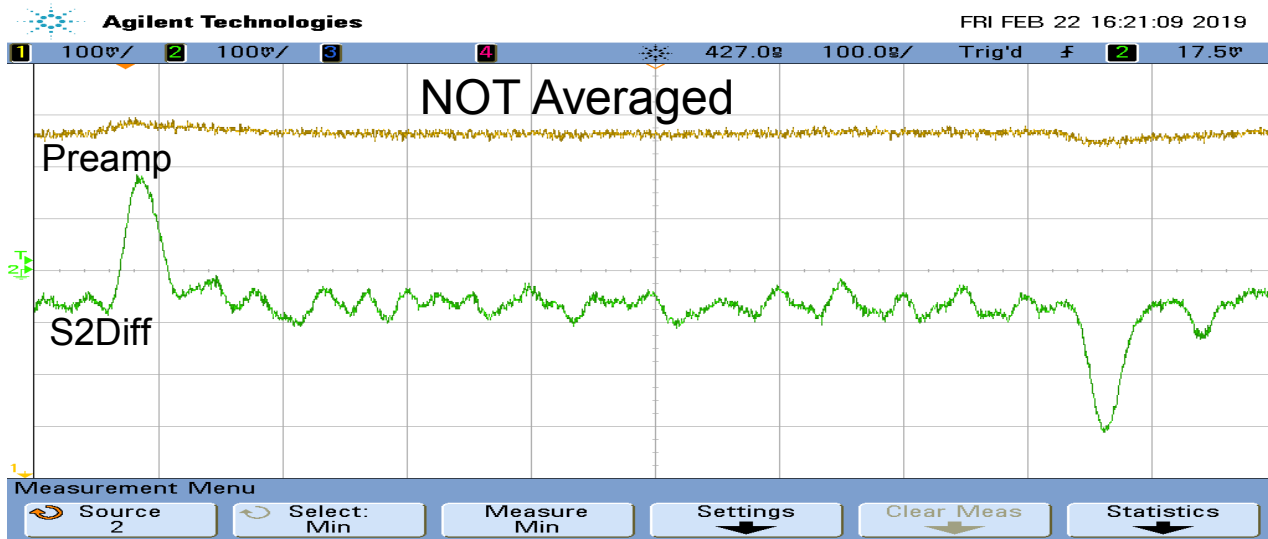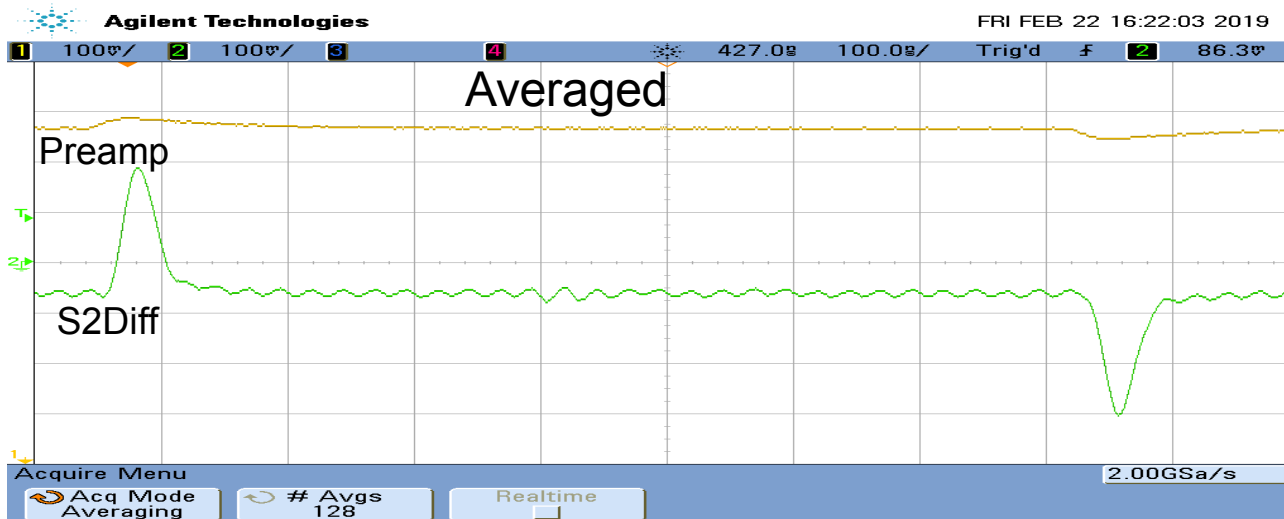SALT3_noInput_noDummy_ch128_activity.dat
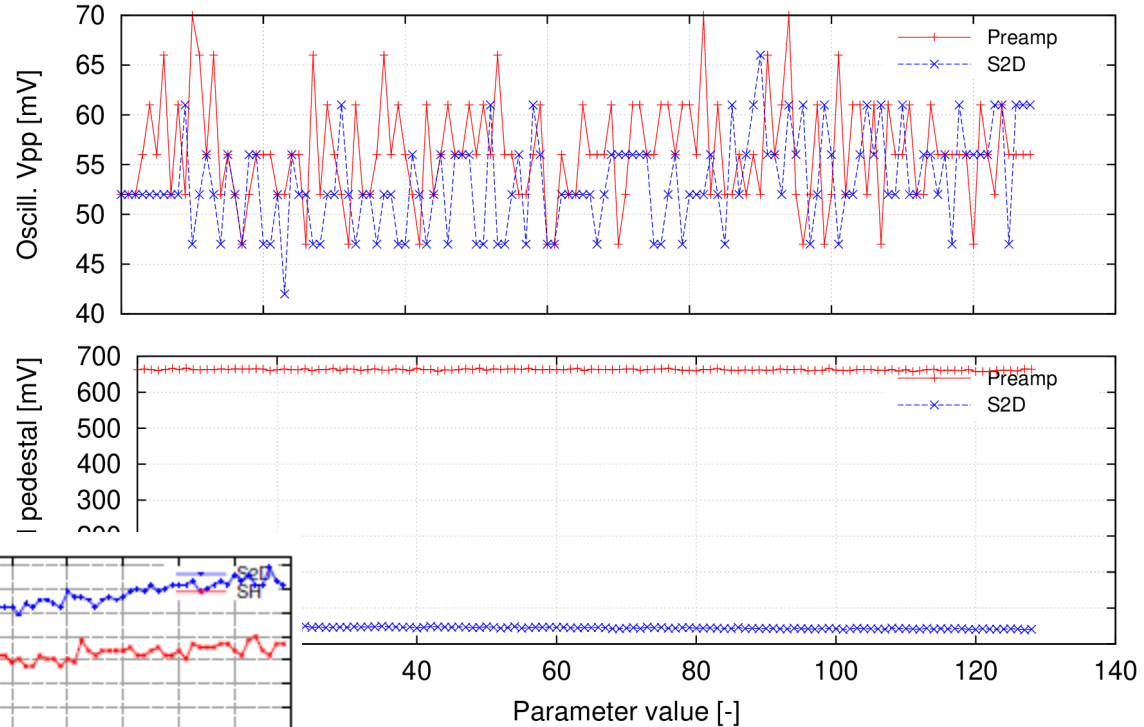
SALTv2

In SALTv3 practically NO oscillations observed, contrary to SALTv2

Transient response to MIP (~4fC) Channel -1, C=24pF, Dummy current ON

Good pulse response is seen even with 24pF external input capacitor

With 24pF external input capacitor 40MHz disturbance is still small