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SALT, a 128-channel readout ASIC for Upstream Tracker in the LHCb Upgrade

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SALT is a 128-channel readout ASIC, designed in CMOS 130˜nm process, for silicon strip detectors in the upgraded Tracker of LHCb experiment. It extracts and digitises analogue signals from the sensor, performs digital signal processing and transmits serially the output data. SALT uses the innovative architecture comprising of a low power analogue front-end and a 40˜MSps 6-bit ADC in each channel. The prototypes of SALT have been already tested confirming full chip functionality and fulfilling expected specifications. The design and results of test measurements will be presented.

Summary

Silicon strip detectors in the Upstream Tracker (UT) of LHCb experiment will be read out by a dedicated 128-channel ASIC called SALT.
SALT, designed in CMOS 130 nm technology, extracts, shapes and digitises analogue signals from the sensor, performs Digital Signal Processing (DSP) and transmits serially the output data.
It uses the innovative architecture comprising an analogue front-end and a 40˜MSps 6-bit ADC per channel. The front-end comprises a charge preamplifier and a fast (T_{peak}=25ns and almost symmetrical) non-standard shaper with complex poles and zeros in transfer function, allowing to distinguish subsequent signals at the LHC bunch crossings 40˜MHz rate. The front-end works with both sensor polarities for capacitances up to $\sim$ 20pF. The phase of the ADC sampling is controlled by a low power DLL.

Digitised data from each ADC channel are processed in the DSP block which subtracts pedestals, calculates the
mean common mode (MCM) and subtracts it in each channel. The last DSP step is zero suppression (ZS). After ZS the data are buffered in SRAM and sent in packets to DAQ via serial DDR e-links equipped with SLVS drivers. A low power PLL generates 160˜MHz clock for data serialization and fast 320˜Mbps DDR transmission circuitry.

SALT is a System-on-Chip type ASIC. Besides already mentioned blocks (front-end, ADC, PLL, DLL, DSP, SRAM, SLVS) it includes: calibration circuitry, reference voltage generators, various 5-8 bit DACs (for biasing, baseline, SLVS, calibration), monitoring ADCs (for PLL, DLL, DACs), variable number of active e-links, I2C block, TFC Timing and Fast Control block, etc...

Many tests have been already performed. First, the digital functionality (e-links, DSP, I2C, TFC, etc.) was positively verified. Next, analogue pulses were observed in analogue form in two test channels and then in all channels after ADC conversion (DLL was used to shift ADC sampling phase to reconstruct pulse shape). The measured performance well agrees with expectations. In next step the measurements were repeated with external capacitances/sensors connected to SALT inputs. In previous prototype large oscillations were seen when capacitance/sensor was connected. This problem was attributed to large internal parasitic inductances in the power network. Designing the present chip the main focus was on proper simulations of parasitic inductances. Measurements done with capacitance/sensor fully confirmed suspected inductance issue. Expected pulse shapes were observed with capacitance/sensor in test channels and in all channels after digitisation and pulse shape reconstruction. For analogue test channels SNR of $\sim$ 20 was measured with $\sim$ 10pF capacitance. For all channels, with largest sensor ($\sim$ 12pF/channel), first measurements show SNR of about 12. The small

pick-up of 40MHz is still present on the baseline but it is expected from simulations and it can be removed by MCM subtraction.
Presently the pre-production tests of larger system with multiple SALT chips on hybrids are ongoing in order to verify whether the UT system specifications are fulfilled.

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