A multi-channel multi-data rate eLink receiver circuit for the lpGBT

Dongxu Yang²³, Szymon Kulis¹+, Datao Ghong², Jingbo Ye², Paulo Moreira¹

1) CERN, Geneva, Switzerland
2) Department of Physics, Southern Methodist University, Dallas, TX , USA
3) Department of Modern Physics , University of Science and Technology of China, Hefei, China

+) szymon.kulis@cern.ch
Outline

• Motivation
• eLink receiver
  • Requirements
  • Architecture
  • Implementation
  • Measurement setup
  • Measurement results
• Summary
Data transmission in HEP experiments

High radiation doses
LHC: up to 100 Mrad $(10^{14} \text{ 1MeV n/cm}^2)$
HL–LHC: up to 1 Grad $(10^{16} \text{ 1MeV n/cm}^2)$

No or small radiation doses

On-Detector
Radiation Hard Electronics

SerDes

TIA

PD

LD

FPGA

Timing & Trigger

DAQ

Slow Control

Off-Detector
Commercial Off-The-Shelf (COTS)

Custom ASICs

Timing & Trigger

Electrical links to the frontend modules.
Lengths: $cm$ to few $m$ (up to several ns)

Short distance optical links:
Lengths: 50 to 300 m (up to 1us)
IpGBT ASIC

- FE Module
- E-Port
- Phase Aligners + Ser/Des for E-Ports
- 160 Mbps to 1.28 Gbps ports
- One 80 Mbps port
- GBT – SCA
- E-Port
- eLink
- data-down
- data-up
- clock

IpGBT

- Phase Shifter
- DSCR
- DEC
- DeSER
- CLK Manager
- CDR/PLL
- SCR
- ENC
- SER
- LD
- LR
- EOM
- I2C Masters
- I2C Slave
- PIO
- ADC
- PIO
- I2C Slave
- Configuration (e-Fuses + reg-Bank)

IpGBTIA

- LDQ10
- 2.56 Gbps
- 5.12 Gbps or 10.24 Gbps
- Ref CLK (optional)

- Enable/Disable clock
- Enable/Disable control data
- CDR/PLL

- Process Monitors
- Control Logic

06/09/2019

CERN

SMU

Szymon KULIS | TWEPP 2019
Front-end communication

- How front-end modules sample downlink data and get the timing reference (not covered in this talk):
  - Use synchronous clock from lpGBT (top)
  - Recover clock from the data stream using CDR circuit (bottom)
- How does lpGBT sample uplink data?

Clock (explicitly) provided to the front-end by an eLink clock.

Clock embedded in the data, CDR needed at the front-end.

Phase relationship between the received data and the internal clock unknown!
Requirements

• Reliable data transmission (BER<10^{-12})
• Multi channel design (28 in IpGBT)
• Data rates: 160 / 320 / 640 / 1280 Mbps
• Low power
• Flexible (to support various use cases)
• Total Ionising Dose: < 200 Mrad
• SEU robust
• Process: 65 nm CMOS
• VDD: 1.2 V +/- 10%
• Temperature: from -20 to 100 °C
How does lpGBT sample uplink data?

- The lpGBT always provides the clock to the front-end modules and thus “knows” exactly the frequency of the incoming data and therefore a CDR circuit is not needed for each ePort.

- The phase of the incoming data (up to 28! channels) is “unknown” in relation to the internal sampling clock. (The phase depends on module implementation, power supply voltage, temperature, …)

- Our approach:
  - Measure the phase offset of each eLink input
  - Delay individually each incoming bit stream to phase align it with the internal sampling clock

Data on eLink “a” has be delayed by ~0.5 UI
How to delay data? (Phase aligner)

Delay Line

PD → CP → LPF

MUX

(x4)

Phase Select

Q D CK

Input Data (unknown phase)

Resampled Data

Bit Rate Clock

Delay Line (replica)

(x1)

Reference DLL
Delay Line structure

- Delay cell is made of two identical half delay cells
  - Delay of $T_{bit}/8$ (data rate dependent)
  - Power down feature
  - Output disable feature
- Delay line:
  - Covers $1.75 \times T_{bit}$
  - 28 delay cells but only 14 outputs are presented to the outside
    - First half (1-14) are used for high data rates (320, 640, 1280 Mbps)
    - Even outputs (2, 4, …, 28) are used for 160 Mbps

![Half delay cell diagram]
How to detect edges?

Dedicated FSM to filter the “randomness” coming from the edge detection process (and data jitter)

- $e[1]$ – always 0
- $e[3]$ – 1 when transition
- $e[5]$ – always 0
1. Examine all the phases and detect where the data edges are in relation to the clock; (next slide)

2. Choose the phase that has the edges better centered around the clock;

3. Once aligned, the PA can track the data phase wanderers that cover virtually a full clock cycle:
   - To allow for this the delay line covers more than one bit period: $1.75 \times T_{\text{bit}}$
   - And, during initialization only phases 4 to 11 are allowed
Modes of operation

- **Static phase selection** - user has to select the proper phase (could be done for systems with controlled environment). Possible to reduce the power consumption by:
  - Disable the delay-line outputs, except the one required
  - Prevent the signal from propagating further though the delay line.

- **Automatic phase tracking** - the state machine constantly monitors the edge transitions and updates the selected phase when necessary
  - Outputs from all delay cells are required

- **Fixed phase with auto startup** - combination of static phase selection and automatic phase tracking modes. The FSM looks for the data phase and the phase setting is frozen after the lock is confirmed.

![Graph showing delay line power consumption](image)
- Static mode allows to save up to 30% of power in the delay line
Deserializers

- ePortRx group produces:
  - 640 Mbps (lpGBT uplink @ 5Gbps): 1x640 / 2x320 / 4x160 Mbps
  - 1280 Mbps (lpGBT uplink @ 10Gbps): 1x1280 / 2x640 / 4x320 Mbps
- Multi rate / multi channel deserializer

Simplified schematic (latches for retiming and clock gating cells are omitted)
Implementation

• Digital on-top implementation
  • Liberty characterization and behavioral model of full custom block
  • TMRG tool (http://cern.ch/tmrg) used to implement Triple Modular Redundancy (TMR) for FSM to protect them against SEUs
• Total size of the block is 800x200µm²
Test setup

- FPGA data source
  - 28 channels, 50ps delay step
  - Data rates: 160/320/640/1280 Mbps
  - Built-in PRBS generators
  - Phase locked with IpGBT

See “IpGBT Tester: an FPGA based test system for the IpGBT ASIC” by J. Mendez et al. for more details
Measurement results

- Bit Error Rate measurement (with internal checker) for PRBS7 pattern
- lpGBT configured in static phase selection mode
- Data rate 1.28 Gbps (relatively high input jitter)
Automatic phase selection

- Data rate 320 Mbps
- Selected phase tracks the input data delay
- (Initial) phase always stays between taps 4 and 11
Jitter estimation

- Data rate 1.28 Gbps (generated by Agilent 81133A with additional jitter)
- IpGBT operates in static phase selection mode
- Bathtub curves measured with IpGBT (points) matches very well the bathtub curves measured by DSO925A scope (lines)
Power consumption includes: eRx differential receiver (not discussed in this talk), phase aligner, deserializer, and phase selection logic.

• Larger power consumption for low data rates: longer delay line and higher weight of eRx static power.

• Power consumption lower in static phase selection mode.
Total Ionizing Dose

- XRAY machine at CERN, Geneva
- Dose rate ~3.5Mrad/h
- Temperature: 10°C

- Data transmission errors observed for TID > 150 Mrad @ 1280 Mpbs

Test passes (green) if there are no data transmission errors (in $10^6$ bits) for at least four phase in static phase selection mode.
Single Event Effects

SEE experimental setup

- Heavy Ion Facility at UCLouvain, Belgium
- Ions: $^{36}$Ar, $^{53}$Cr, $^{84}$Kr, $^{103}$Rh, $^{124}$Xe
- Maximum ion rate of 15kHz

- Unable to determine threshold
- No significant dependence on data rate and mode of operation
Summary

- eLink receiver circuit (comprising phase aligner, phase selection logic and deserializer blocks) has been designed and successfully prototyped as part of the lpGBT ASIC
- Measurements showed that the block is fully functional at all data rates
- Errorless operation observed up to 150 Mrad at highest data rate
- SEU cross section of $\sim 1 \times 10^{-6} \text{ cm}^{-2}$ for LET $> 10 \text{ MeV/(mg/cm}^2\text{)}$