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A multi-channel multi-data rate circuit for phase alignment of data in the lpGBT

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The design and test results of a multi-channel multi-data rate circuit for phase alignment of data in the lpGBT ASIC fabricated in a 65 nm CMOS technology are presented. The circuit is composed of 4 delay lines regulated by a Delay-Locked Loop followed by logic responsible for phase selection and multi-mode deserializer. The circuit is able to handle up to 4 serial data streams with a data rate of 160, 320, 640, or 1280 Mbit/s. The test results show that all blocks are functional in all modes of operation.

Summary

The presented phase-aligner is a building block of the lpGBT chip, a low power gigabit transceiver for the high energy physics experiments. The phase-aligner is responsible for delaying the input data stream to ensure that it can be properly sampled by an internal clock. Each channel incorporates a delay line with 14 equally-spaced taps controlled by a DLL. Based on signal transitions, the phase selection logic determines the optimum sampling point and decides which tap should be used as an input to multi-mode deserializer.

The DLL has 16 delay cells and is locked to clock period equals 2Tbit. Its control voltage is distributed to 4 replica delay lines ensuring that the unit delay is the same. Each line is made of 28 identical delay cells, but only fully used in the data rate of 160 Mbit/s. In other data rates, the first 14 delay cells are activated, while the remaining are powered down. Delay of one cell has been set to Tbit/8, which is 97.7, 195.3, 390.6, or 781.3 ps for a bit rate of 1280, 640, 320 or 160 Mbit/s respectively. The overall length is 7Tbit/4 enabling the delay line to store more history of data and thus to track the phase in more situations. In 160 Mbit/s, all 28 cells are delayed by 390.6 ps, while two delay cells are joined together to form a delay of 781.2 ps, and only even taps are output to phase selection logic. The delay line of the DLL is located in the center of four replicas to ensure the best matching.

The symmetrical delay cell consists of two half-cells which are based on the current-starved inverter. The half-cell has an inverter cascaded by an active NAND and a dummy NAND. Only the active NAND in the second half-cell can output to the phase selection logic. Active and dummy NANDs are controlled by complementary signals keeping the load of half-cell always the same.

The phase selection logic determines the optimal phase based on the edge detection basis. It has three modes: static phase selection mode in which the tap is selected upon user configuration, training with learned static phase mode in which the phase is automatically selected after power-up, and automatic phase tracking mode in which the logic continuously monitors input data phase and selects the optimum sampling point. While the automatic phase tracking mode is the most robust, it requires that the whole delay line is always active and therefore the power consumption in this mode is the highest. For the other two modes, when the phase is determined, the delay cells after the selected cell can be disabled, so do the output buffer of previous cells.

The radiation resistance of the phase-aligner is enhanced by means of Enclosed Layout Transistor (ELT). The phase selection logic is fully triplicated to ensure robustness against SEU. The phase-aligner has been tested as part of the lpGBT and it is fully functional in all modes of operation.

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