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picoTDC:
A 3ps Bin Size 64 Channel TDC for HEP Experiments

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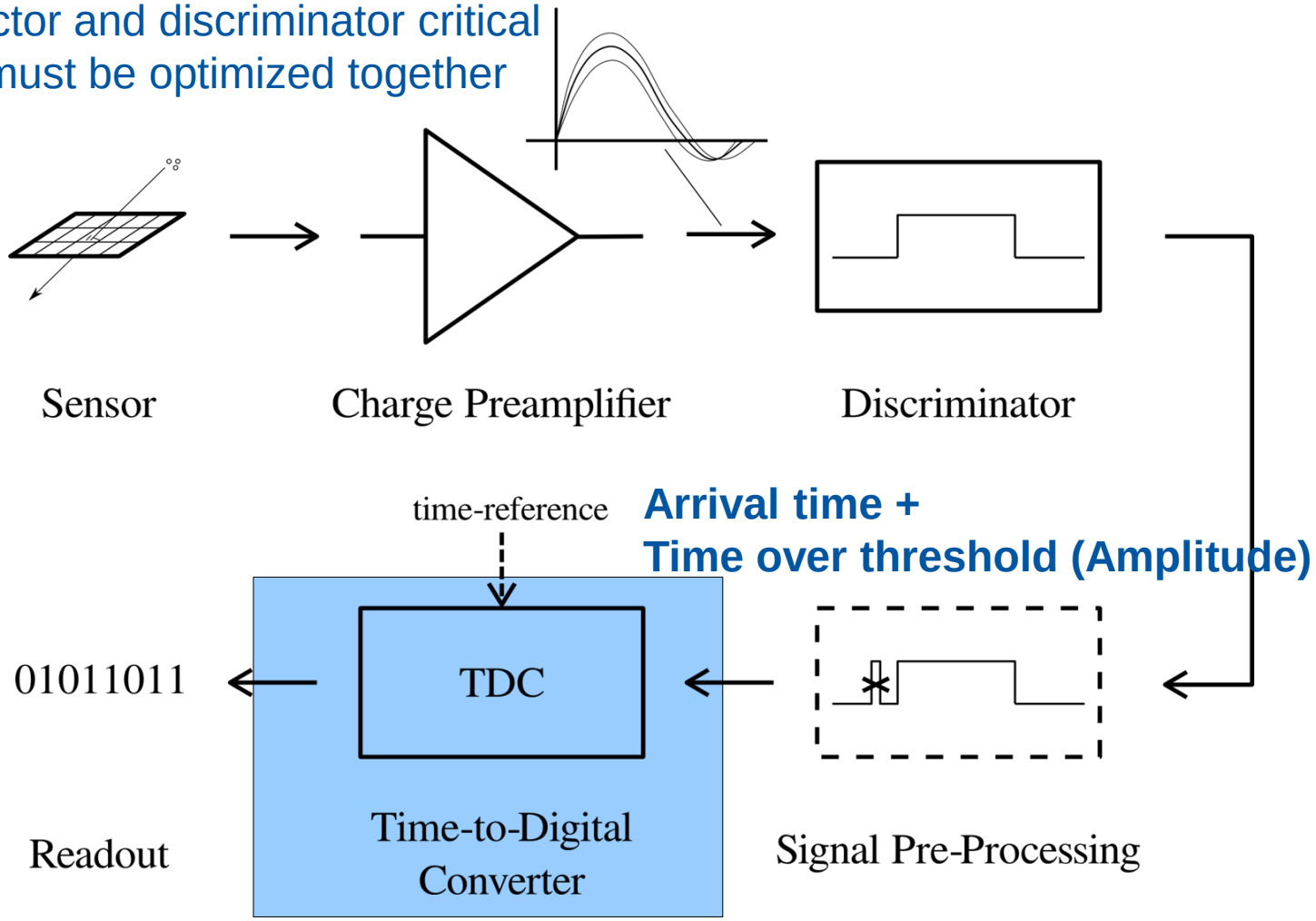
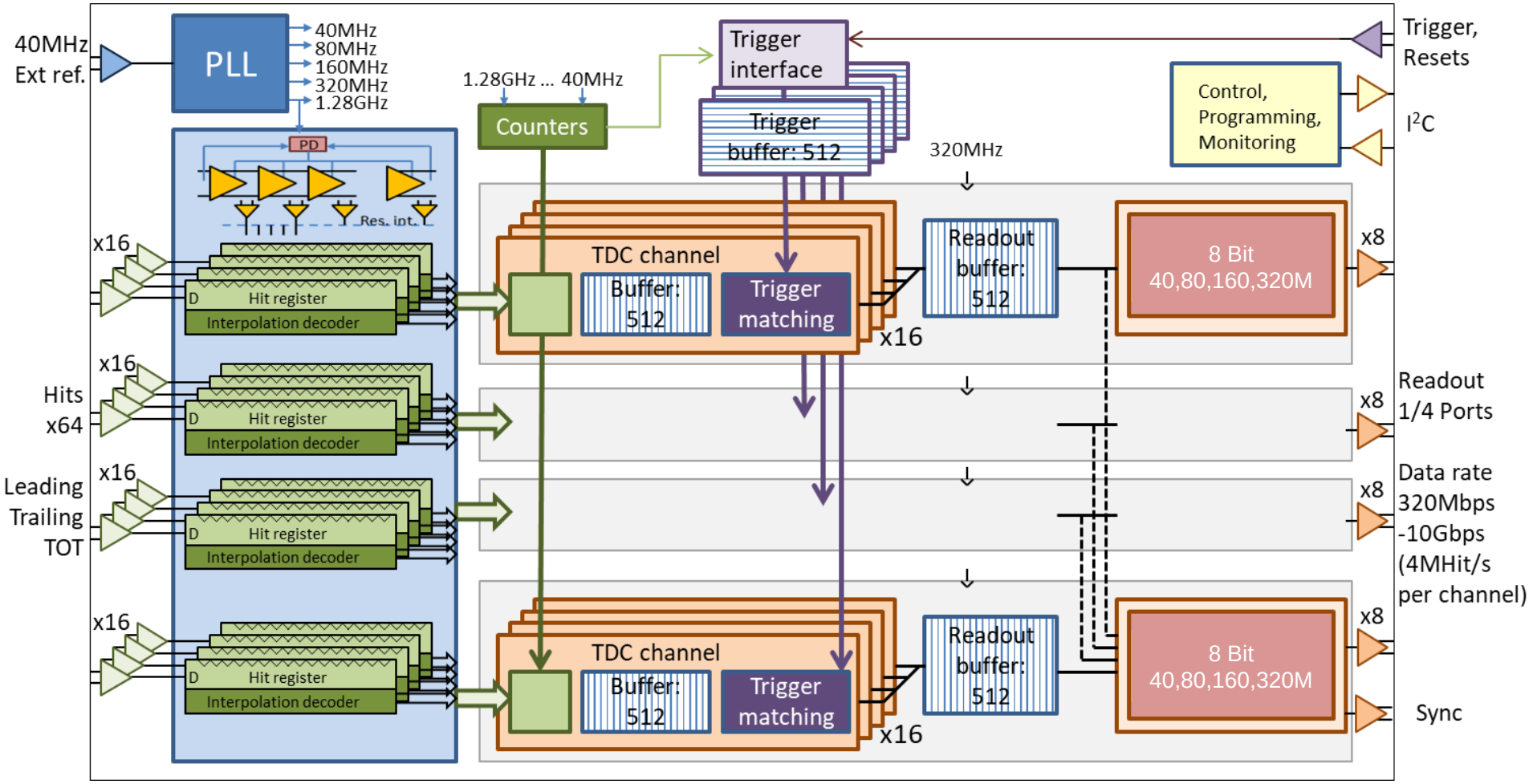
TDC in the Measurement Chain

Detector and discriminator critical and must be optimized together



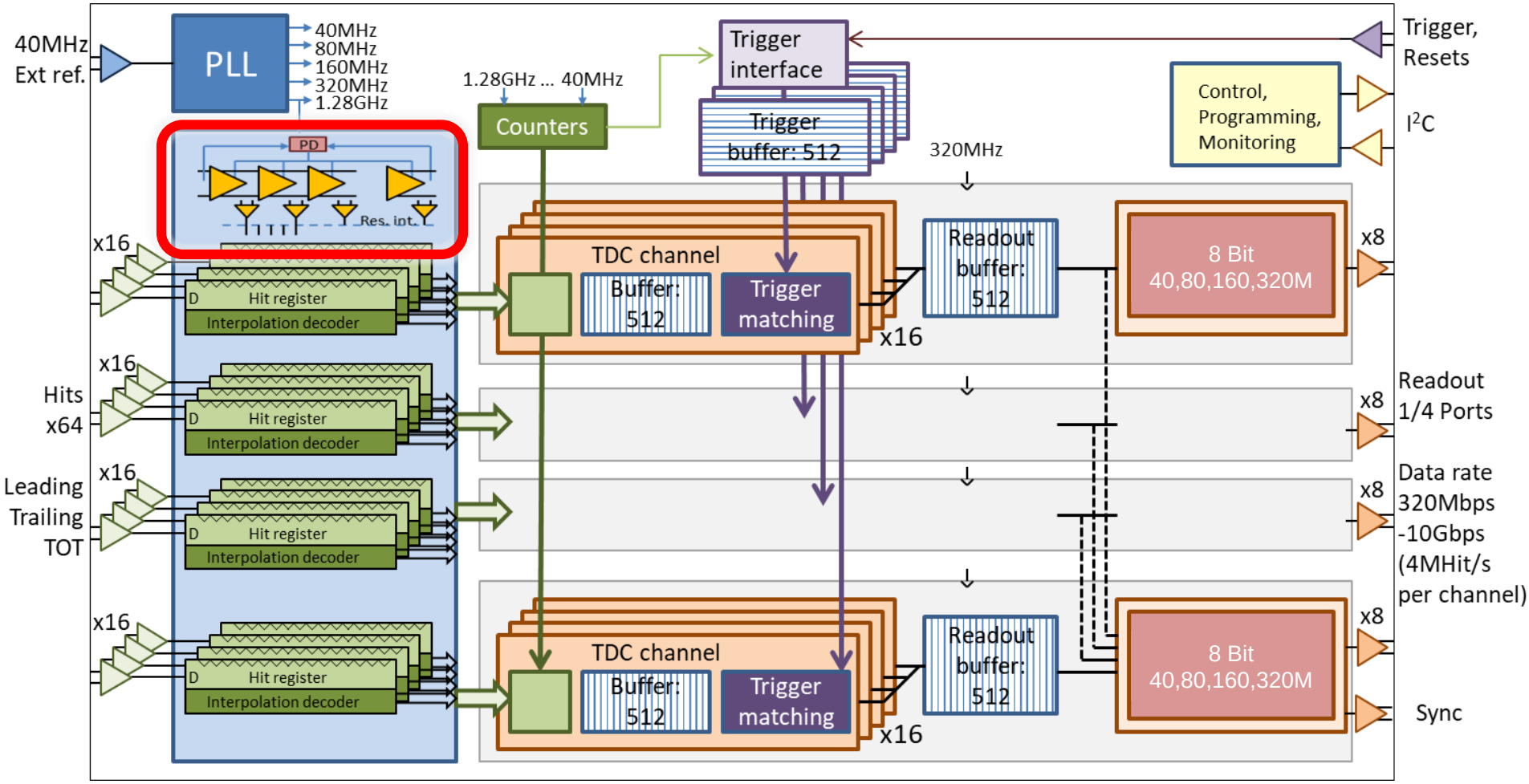
Design Overview

picoTDC Architecture

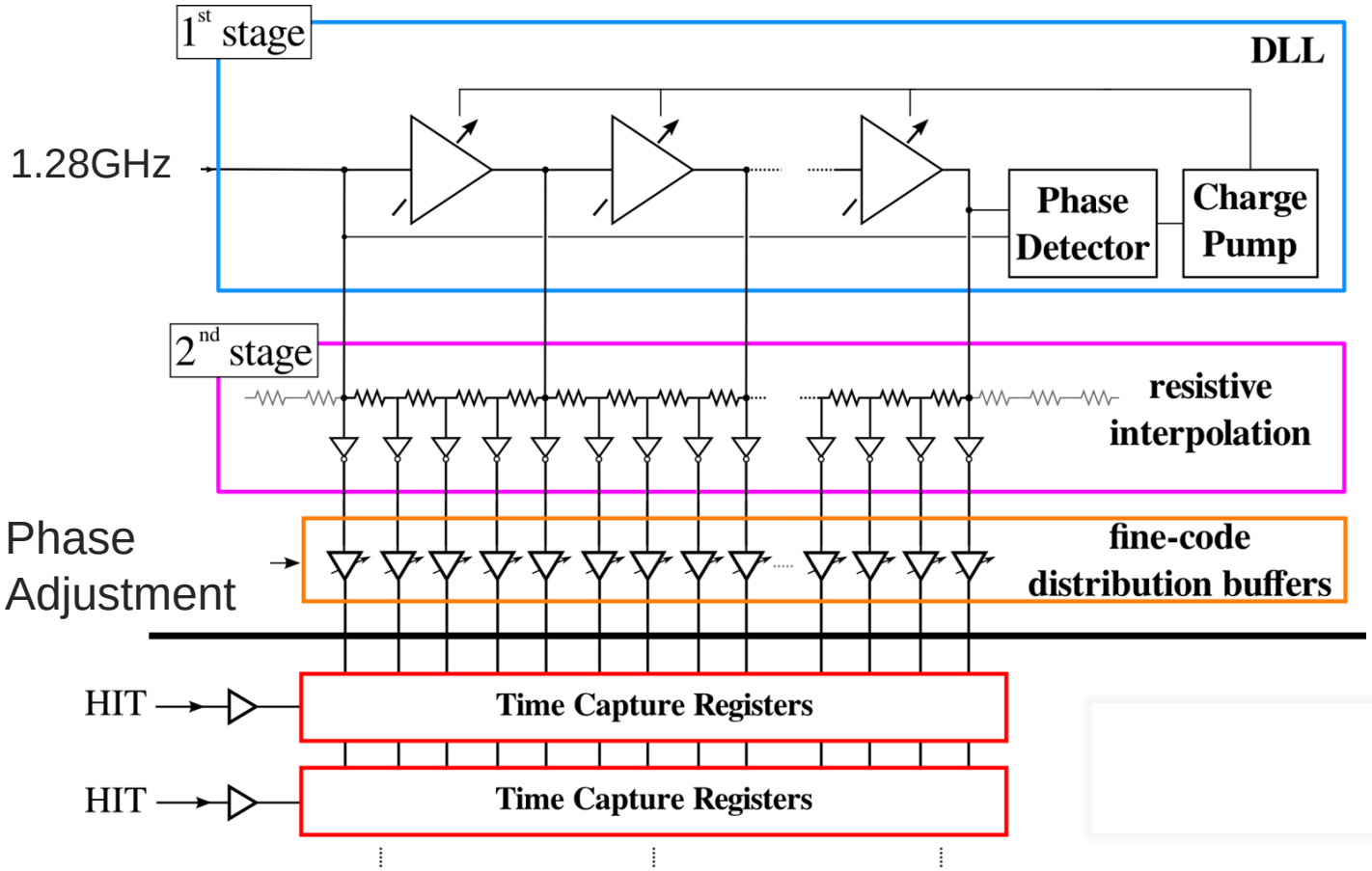


64 channels, 3ps or 12ps time binning, 200us dynamic range

picoTDC Architecture



Two Stage Time Interpolation



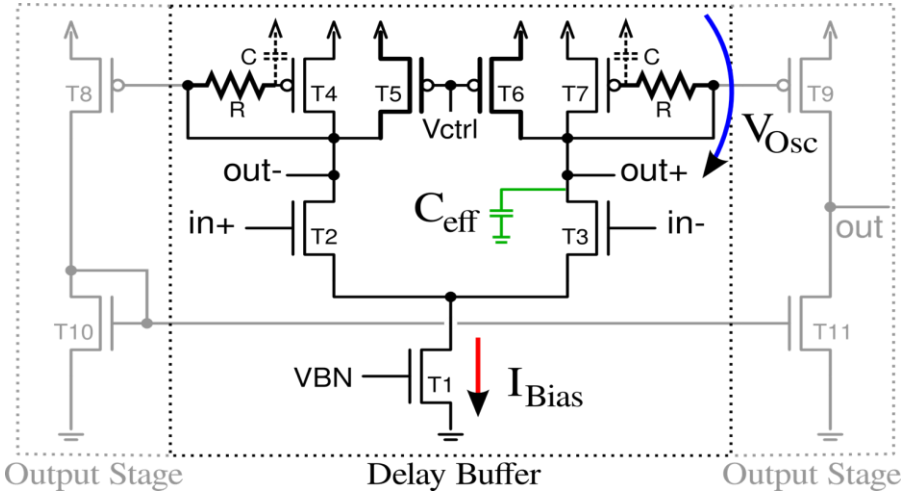
12.2ps delay

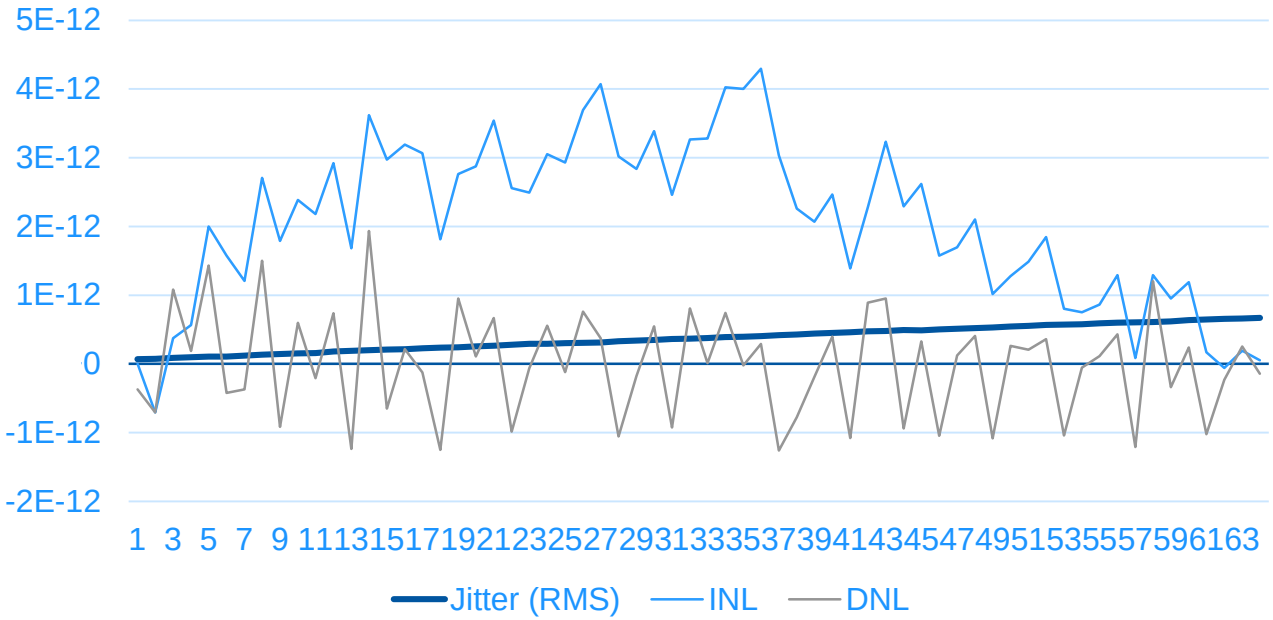
3.05ps delay

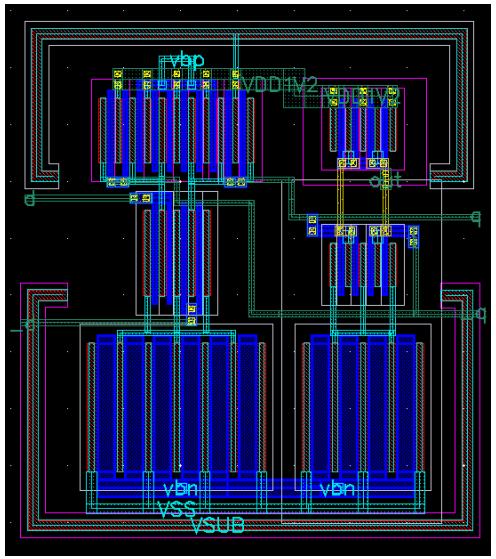
32 steps each with 0.6ps resolution

1st Stage: DLL

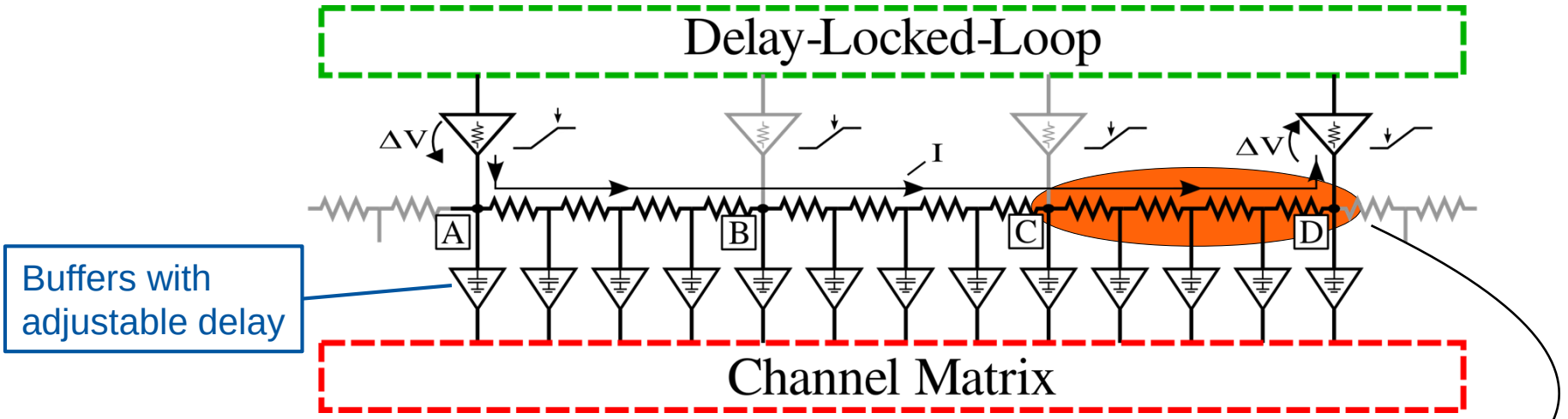
- 64 taps, 12.2ps delay
- Self-Calibrating



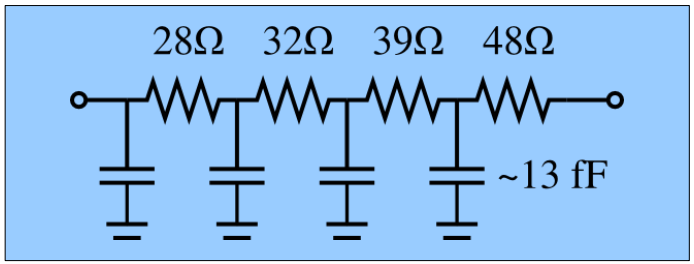


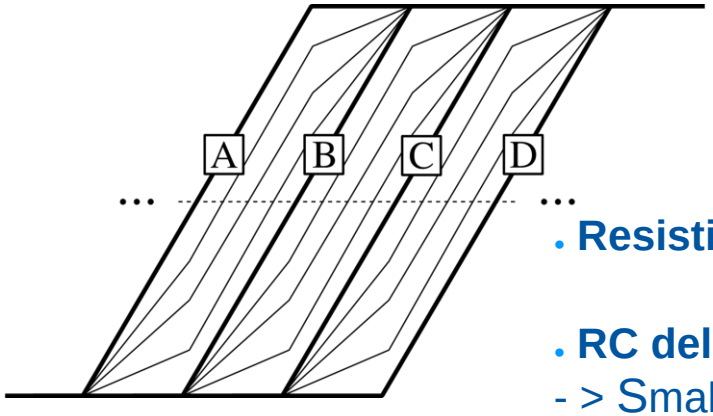


2nd Stage: Resistive Interpolation



Buffers with adjustable delay

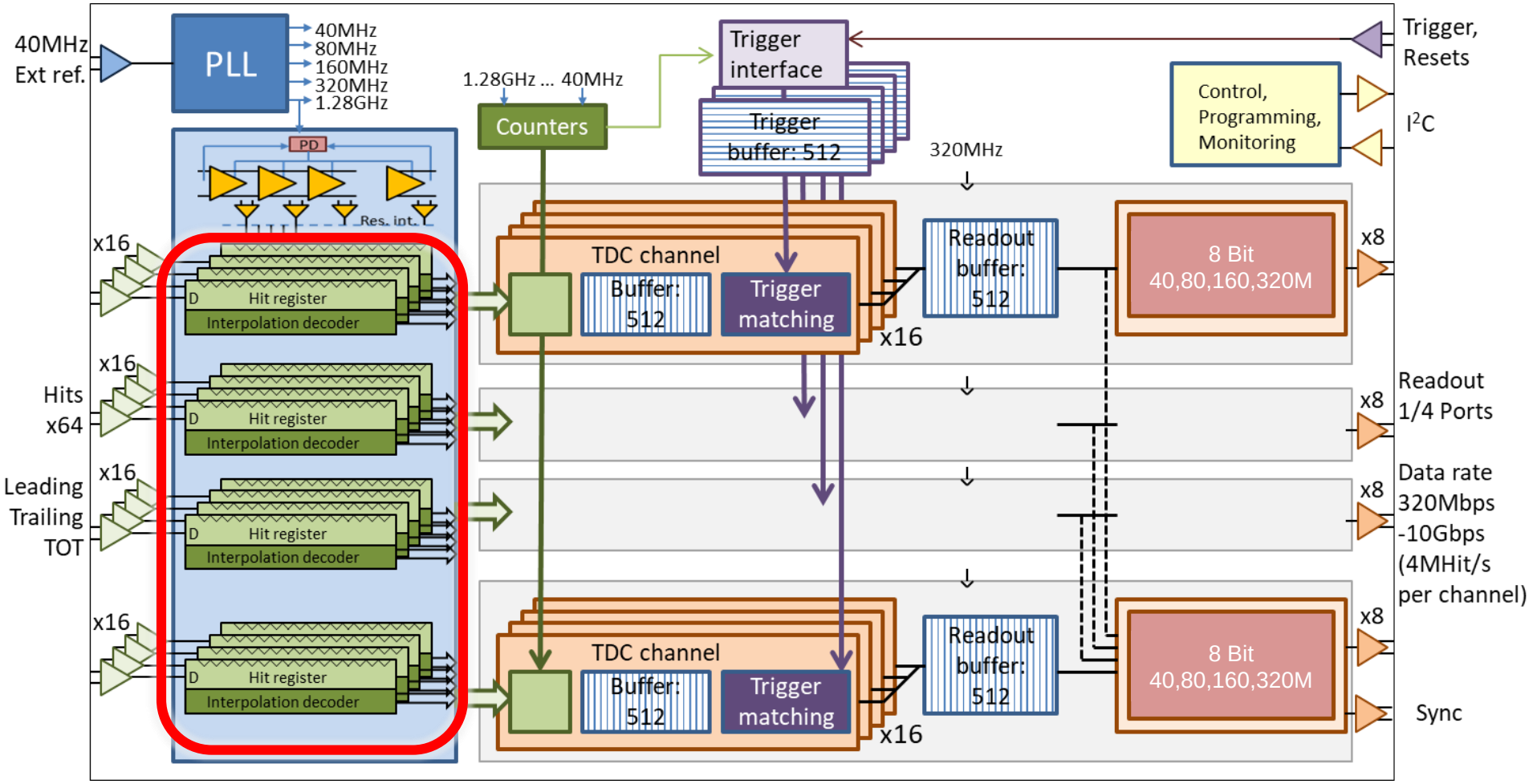




- **Resistive voltage divider**
  -> Signal slopes longer than delay, stabilized by DLL
- **RC delay** (capacitive loading)

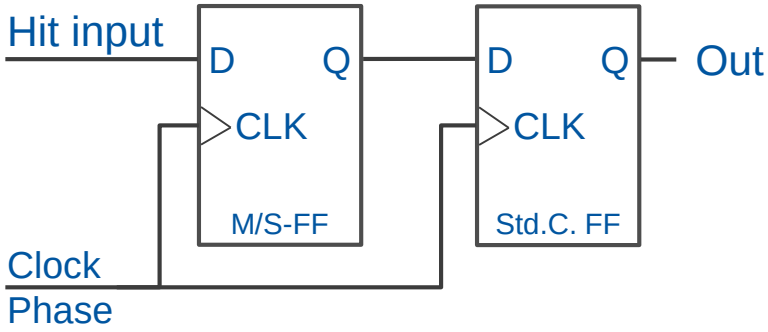
- > Small resistances, small loads
- > Simulation based optimization of resistor values

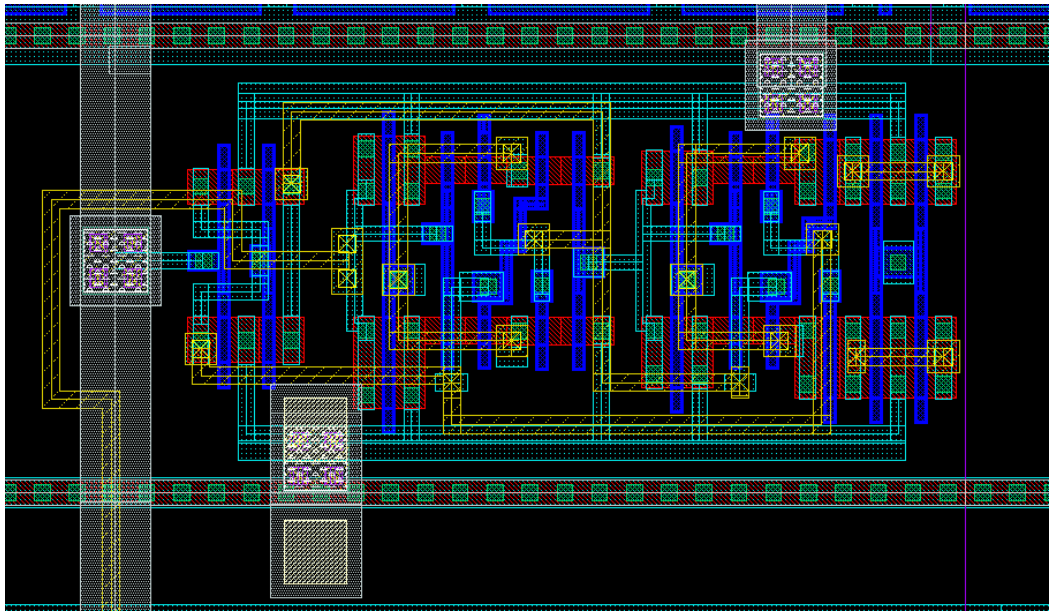
picoTDC Architecture



Capture Flip Flops

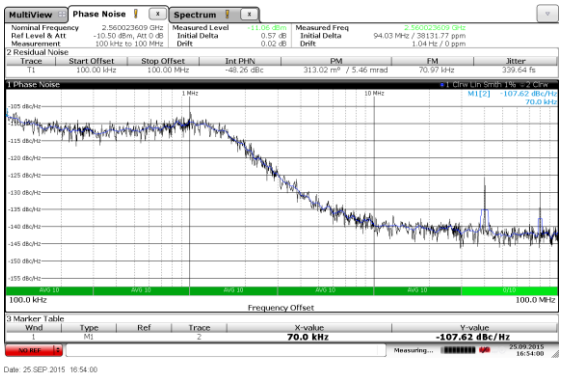
- Revisited design, timing vs. power very critical, 16k capture Flip Flops running @1.28GHz
- Optimized M/S Flip Flop followed by standard cell Flip Flop for metastability resolution
- ! Monte Carlo simulations show a mismatch of 800fs RMS, noise influence of 240fs RMS

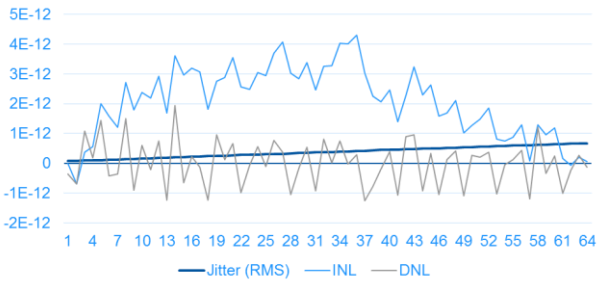


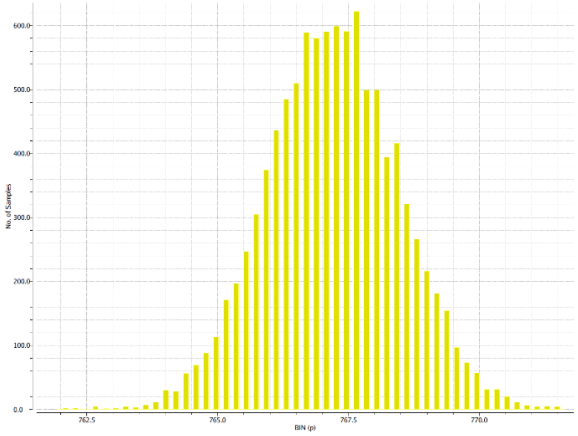


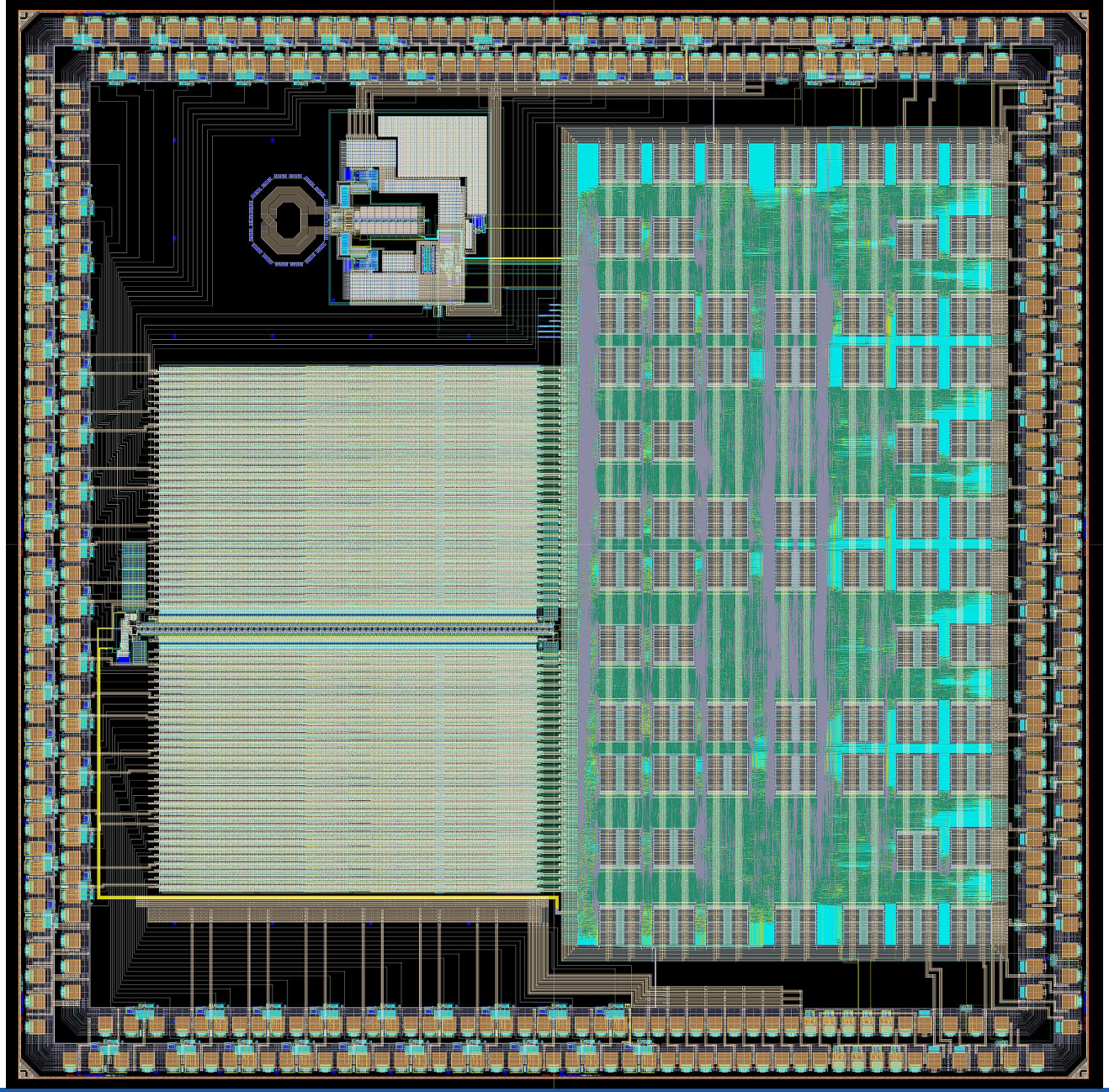
Sources of Measurement Deviation

- Bin size 3ps -> 880fs RMS
- PLL: 350fs RMS phase Jitter
- DLL: 400fs RMS phase Jitter, INL/DNL can be adjusted
- Clock Distribution: <500fs jitter
- ! Capture FFs: <1ps mismatch (DNL)
- Hit receivers: <1ps jitter
- ➢ ~1.75ps RMS total deviation
- External sources: input clock jitter, signal preprocessing









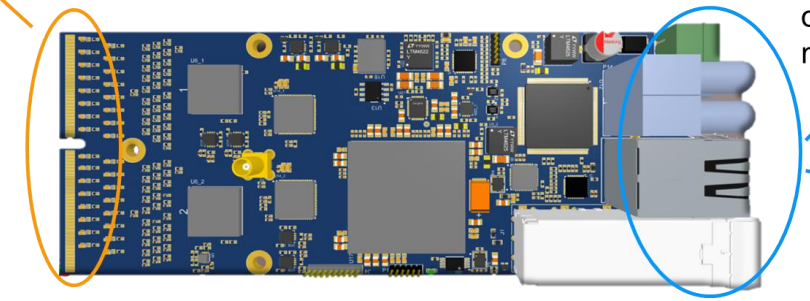
Possible CAEN Modules With picoTDC

The idea of FERS platform

Single card housing Front End ASICs, ADC and/or TDC, FPGA, I/Os, interfaces and, in some cases, detector power supply

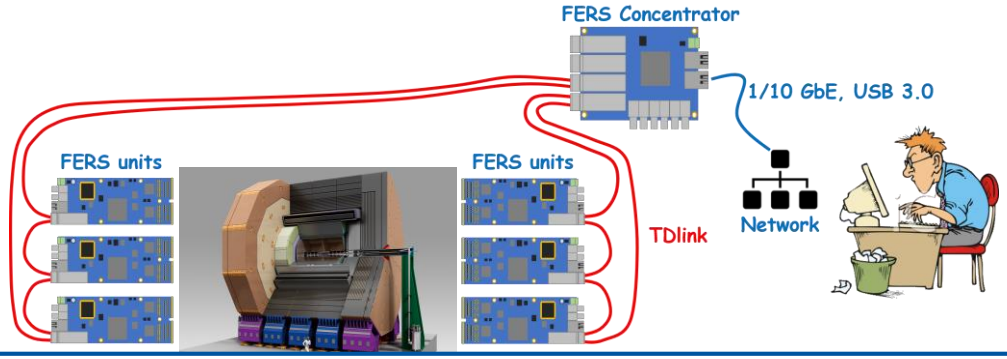
Size of ~15 x 6 cm (for the A5202)

Signals from the detectors come through 0.8 mm edge contacts mating a Samtec **HSEC8-170-01** connector



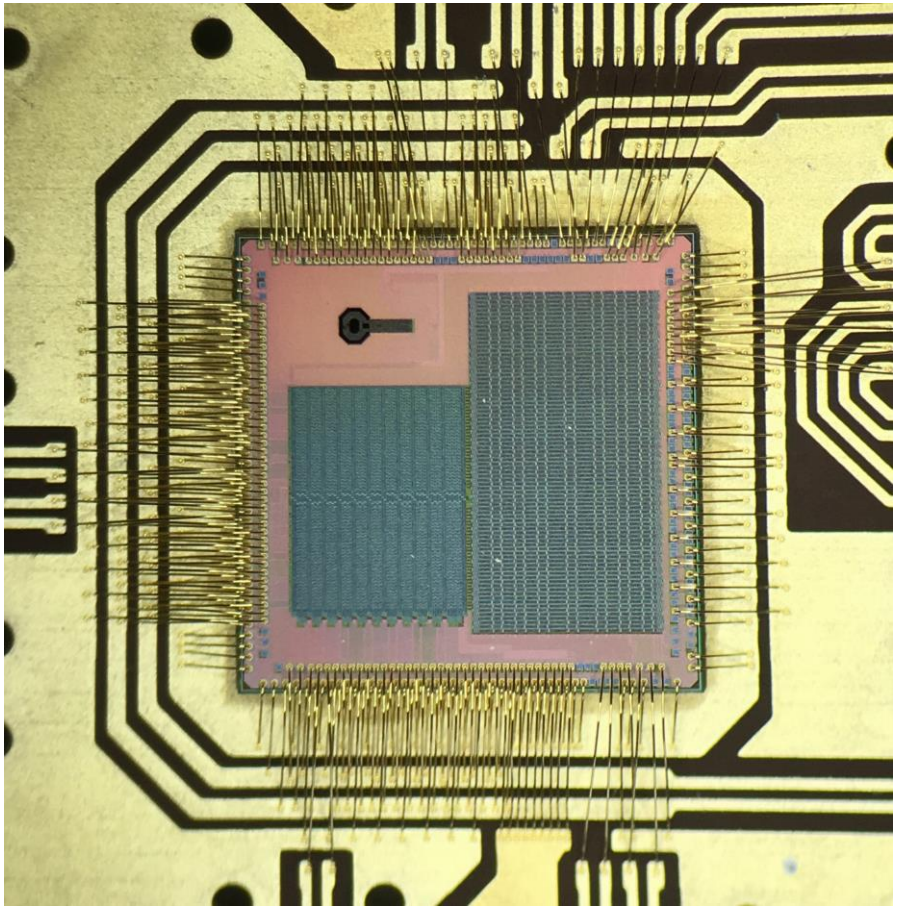
communication interfaces: **TDlink** (sync + commands + data) or **Ethernet**, USB 2.0 (data only, mainly used for evaluation)

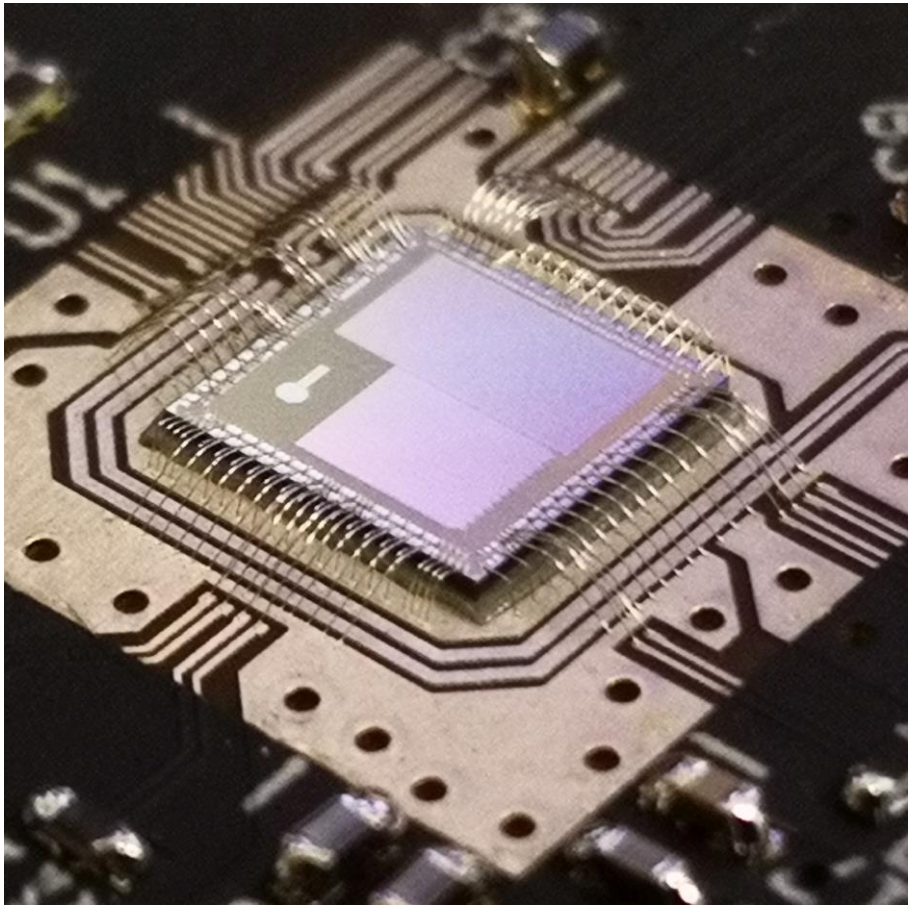
Auxiliary **I/Os** for sub-ns timing and low latency trigger distribution (alternative to TDlink)



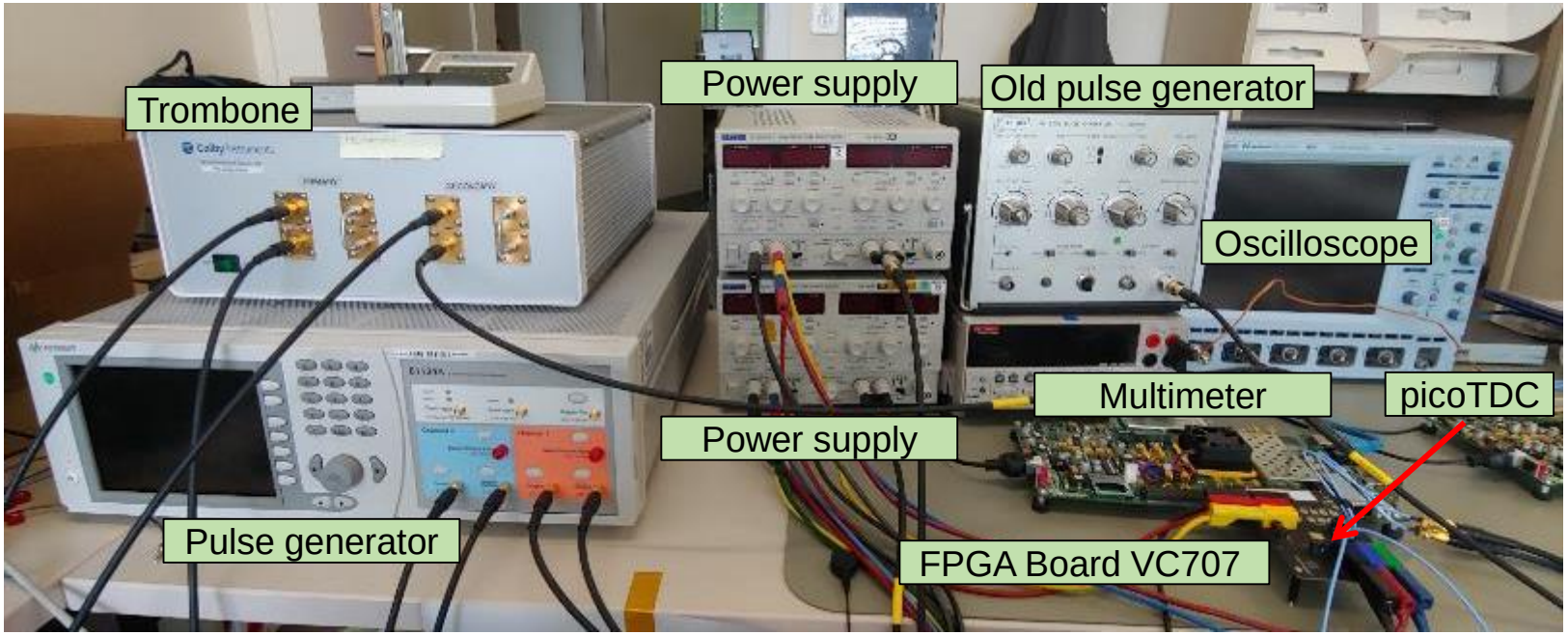
Prototype Results

picoTDC on Test Cards





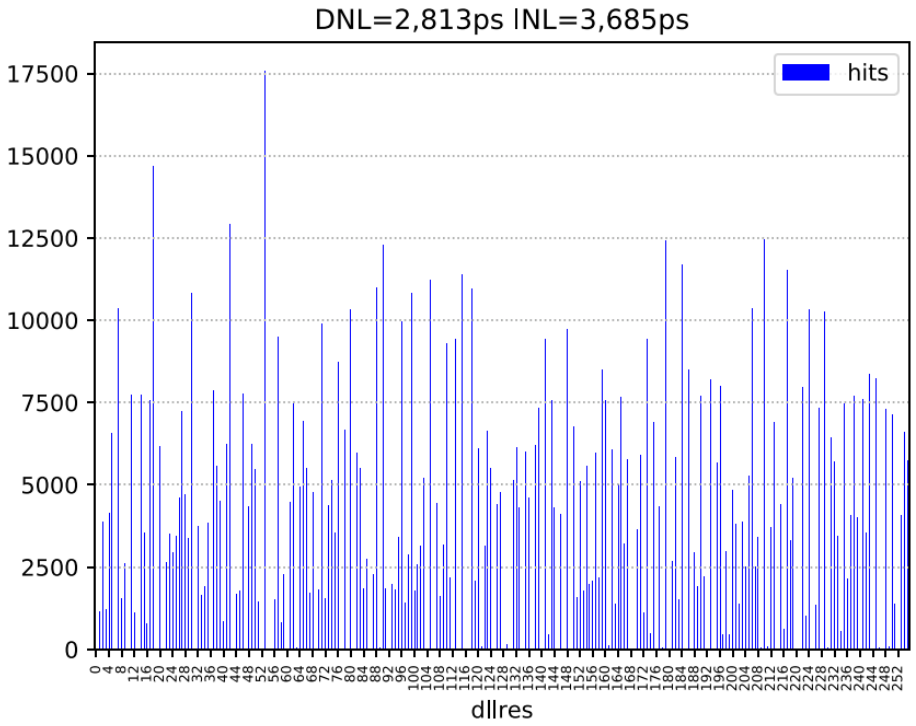
Instrumentation for Testing



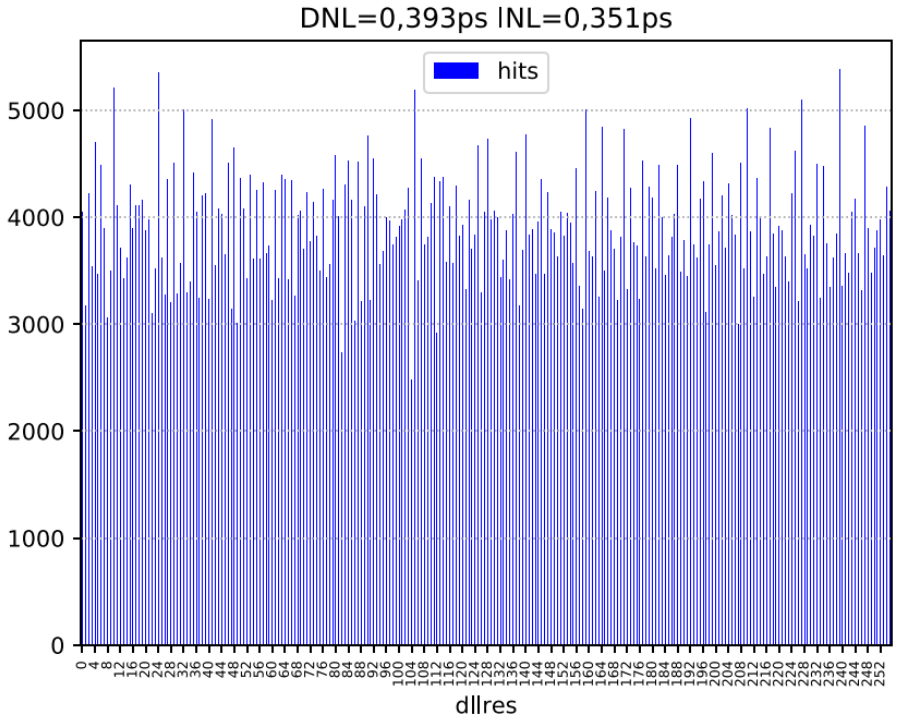
Additional tests with Silicon Labs Si5341 evaluation board for very low jitter measurements

3ps Bin Code Density Test

Not adjusted



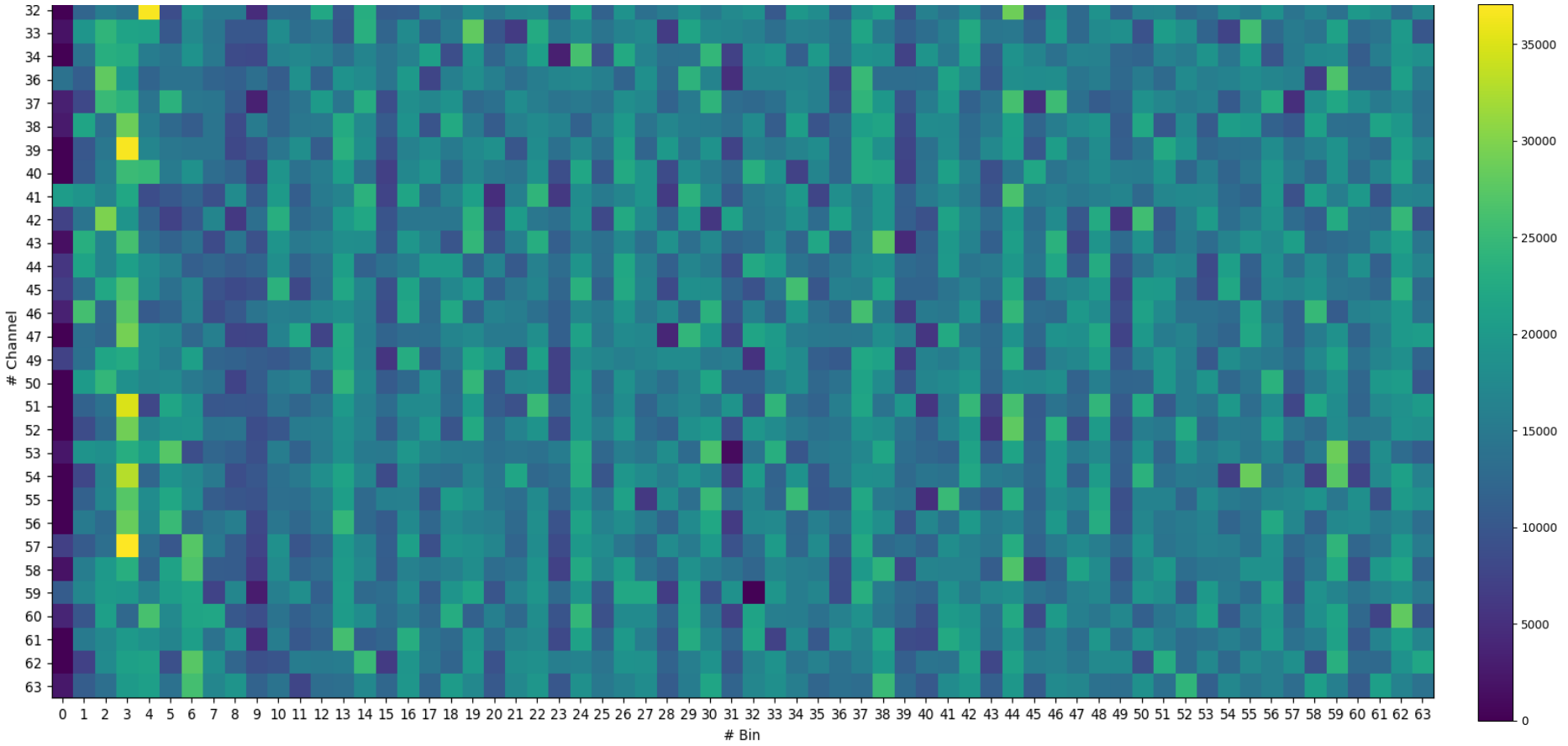
Adjusted



Code Density Test (CDT): Generate random hits uncorrelated to the reference.
-> Number of hits in each bin is equivalent to the bin size.
Adjustment is for single channel only

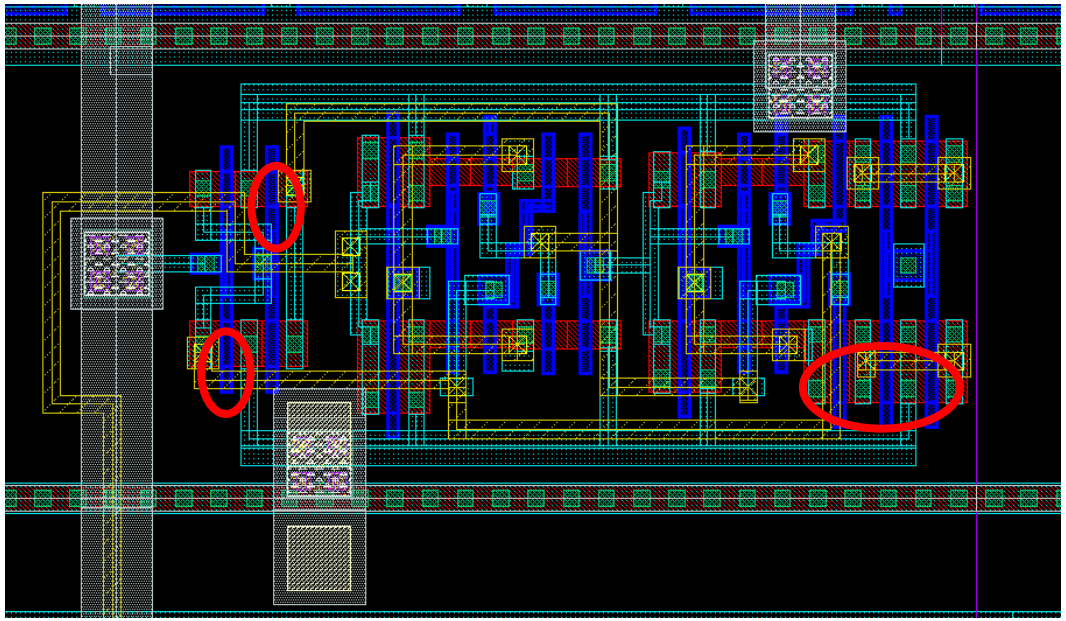
Code Density Test on Multiple Channels

Coarse time, not adjusted, channels 32-64, DNL 3.48ps, Common DNL 1.25ps



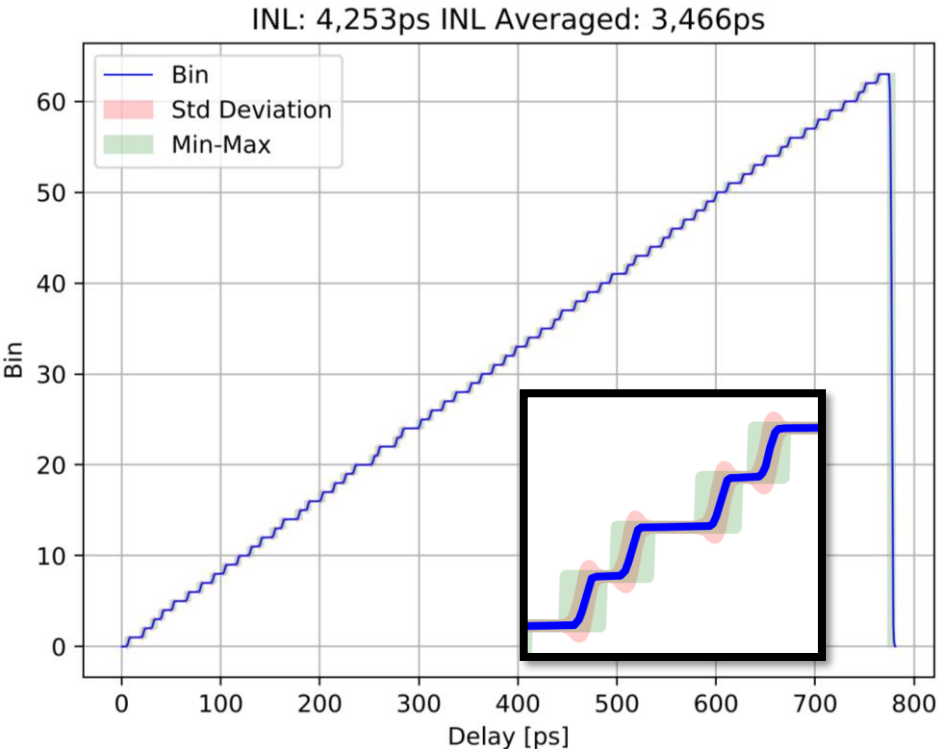
Capture FF Mismatch

- Bug in extraction of fingered transistors caused simulation showing only half of the mismatch
- Resizing of 4 transistors for production version will reduce the mismatch to expected levels, increasing the power slightly

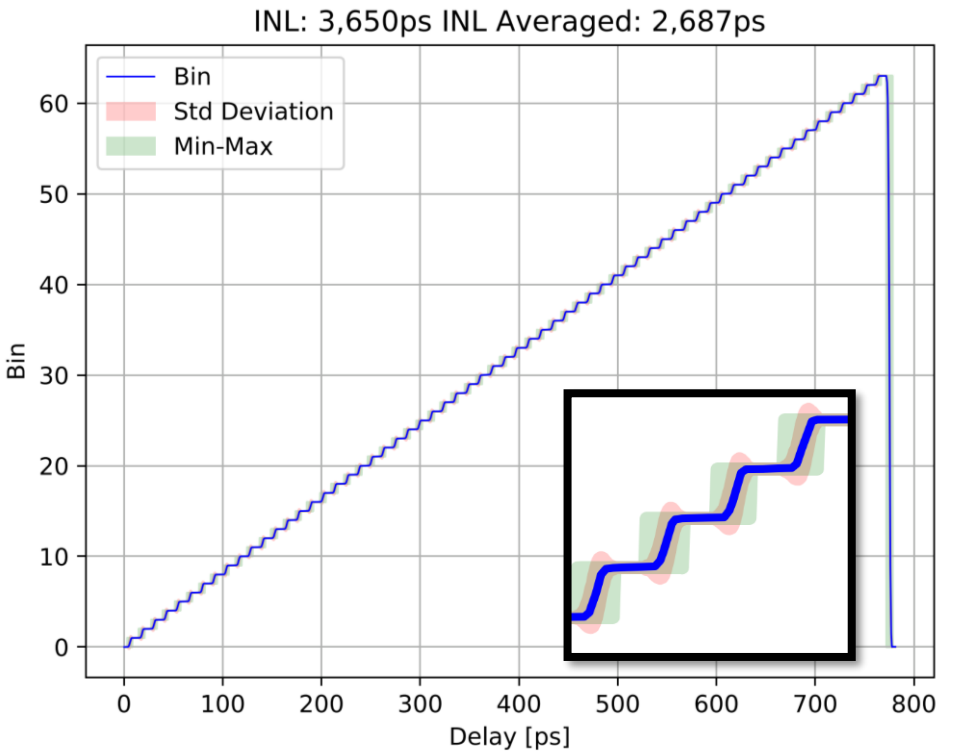


Time Sweep Measurements

Coarse mode, 12ps bin size



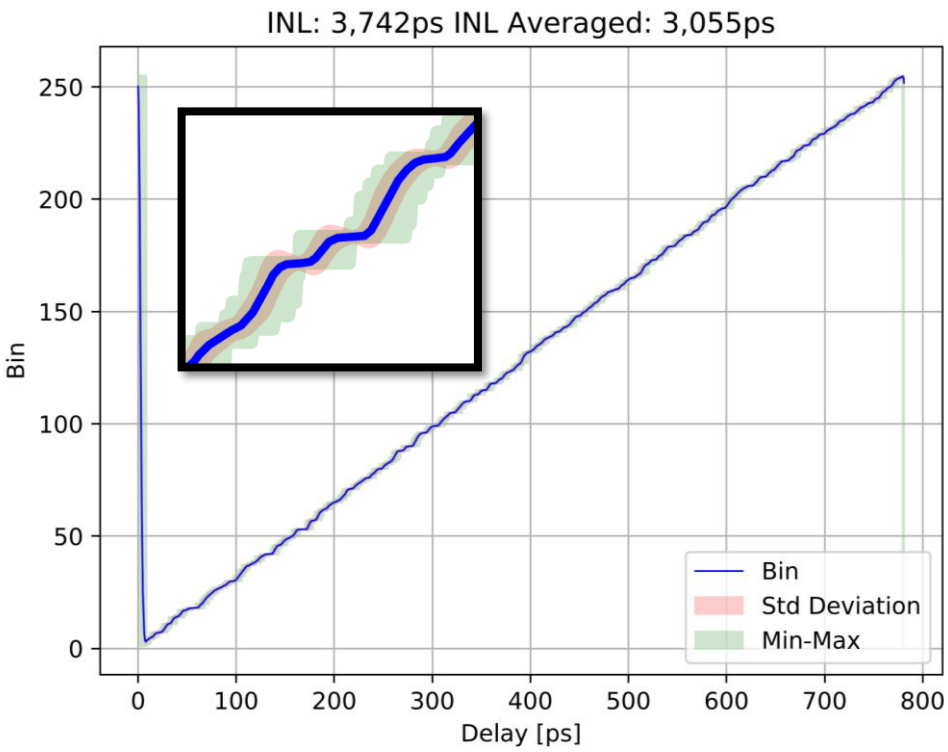
Not adjusted



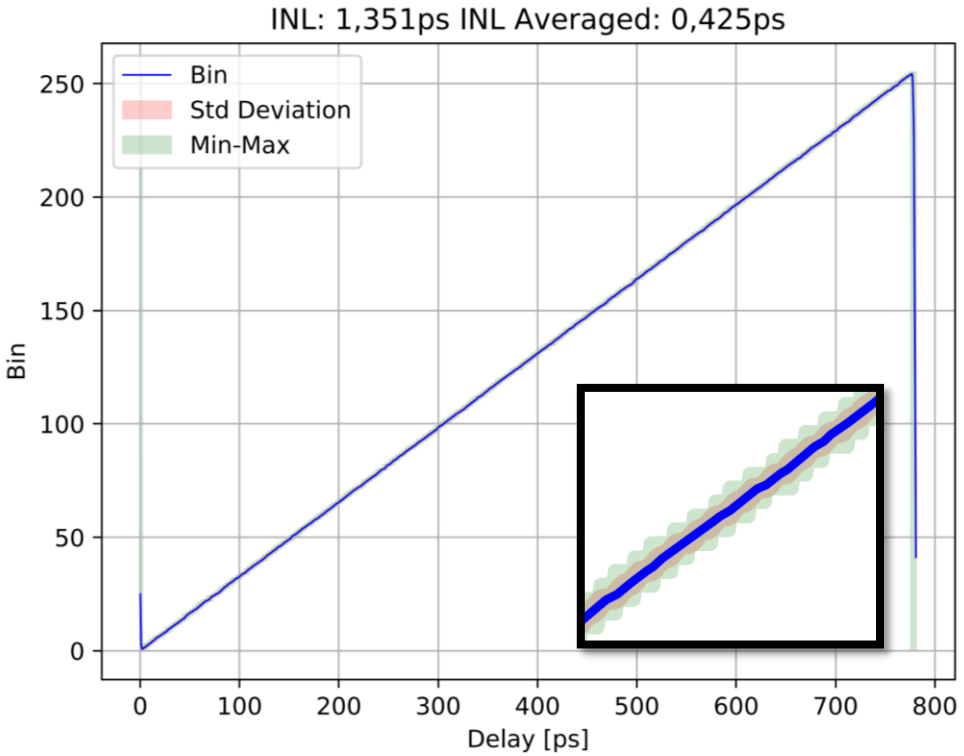
Adjusted

Time Sweep Measurements

Fine mode, 3ps bin size



Not adjusted



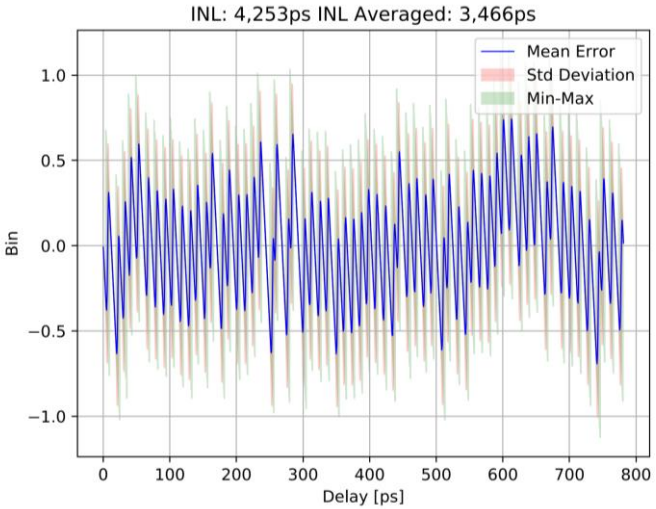
Adjusted

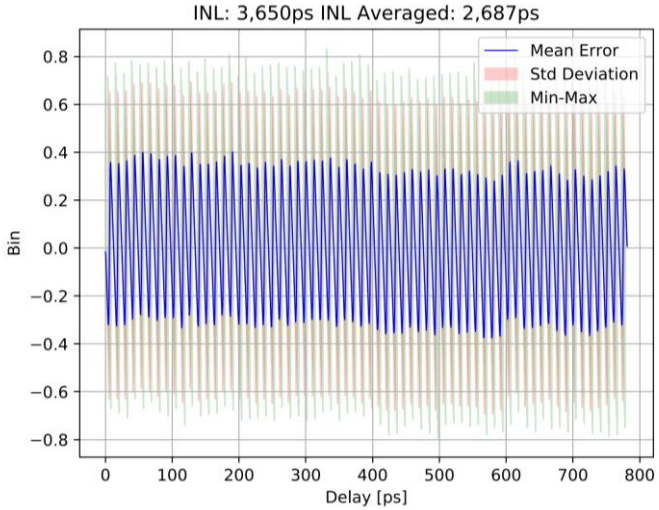
Sweep Measurements Deviation

Not adjusted

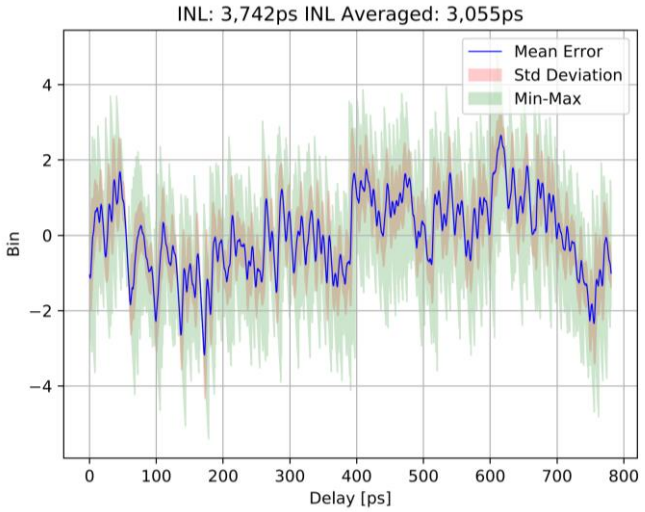
Adjusted

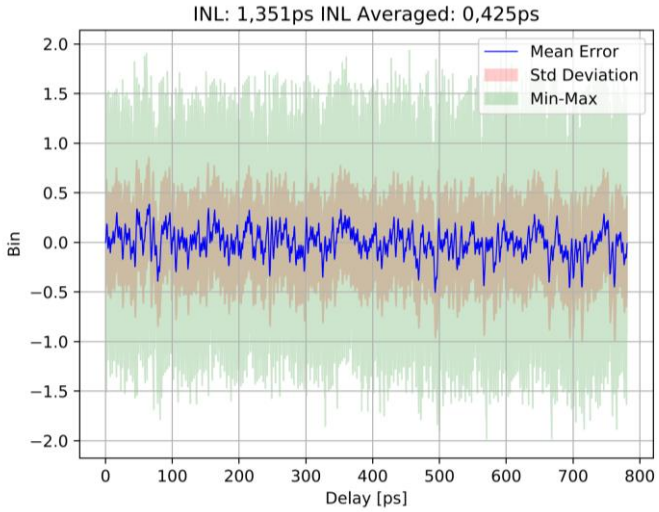
Coarse Mode
12ps Bins





Fine Mode
3ps Bins





Performance Summary

		Code Density Test		Sweep Test	
	adjusted	DNL	INL	INL	INL avg.
Coarse time	✗	2.75ps	2.97ps	4.25ps	3.47ps
	✓	0.27ps	0.29ps	3.65ps	2.69ps
Fine time	✗	2.81ps	3.68ps	3.74ps	3.06ps
	✓	0.39ps	0.35ps	1.35ps	0.43ps

CDT excludes jitter, quantization

Temperature performance	Variation limited to 1 LSB pp	28 ºC to 42 ºC	<1ps/ºC
Voltage performance	Variation limited to 7 LSB pp	1.10V to 1.30V	<0.5ps/mV
Crosstalk test	Influence limited to 2 LSB Worst case one channel vs. all		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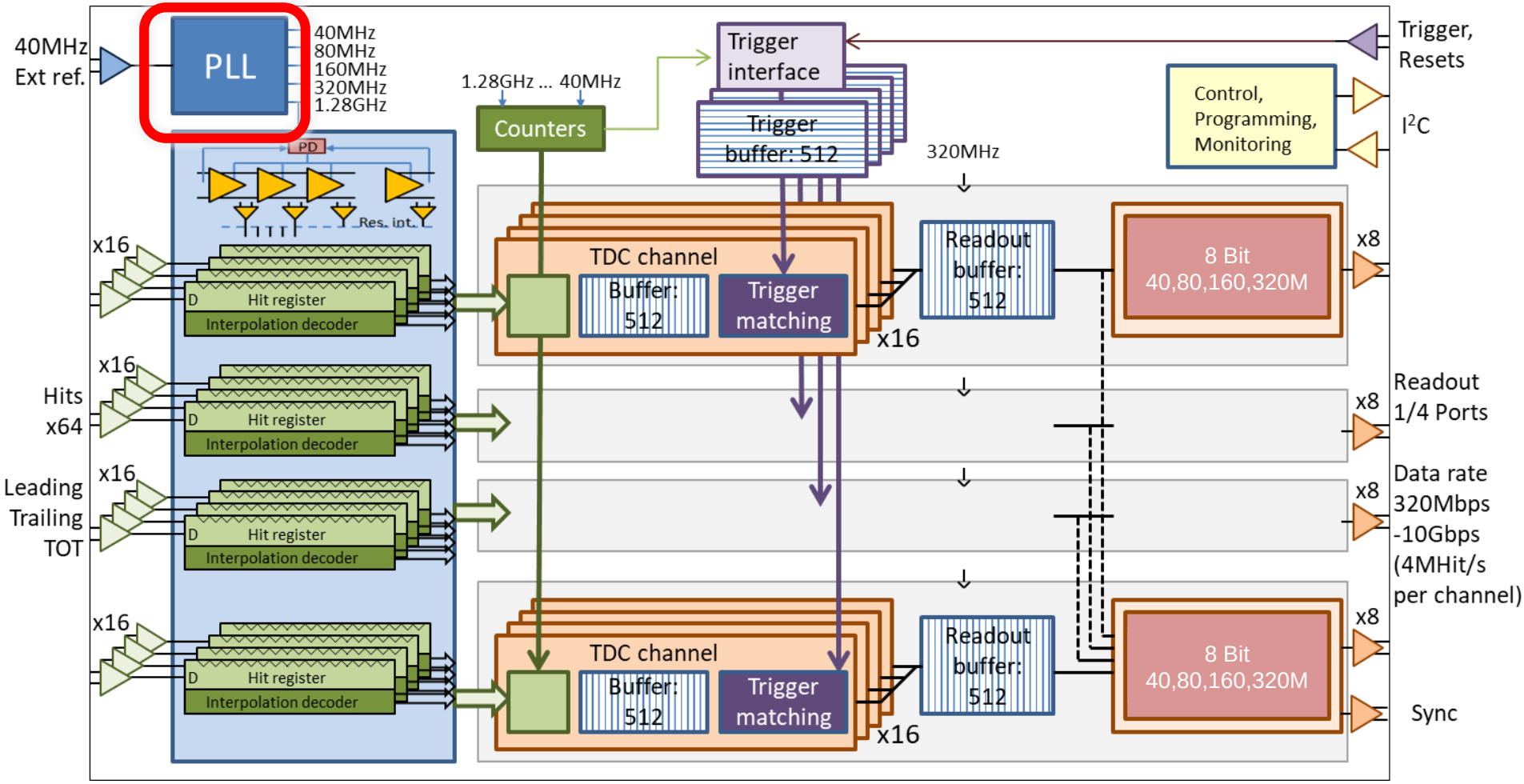
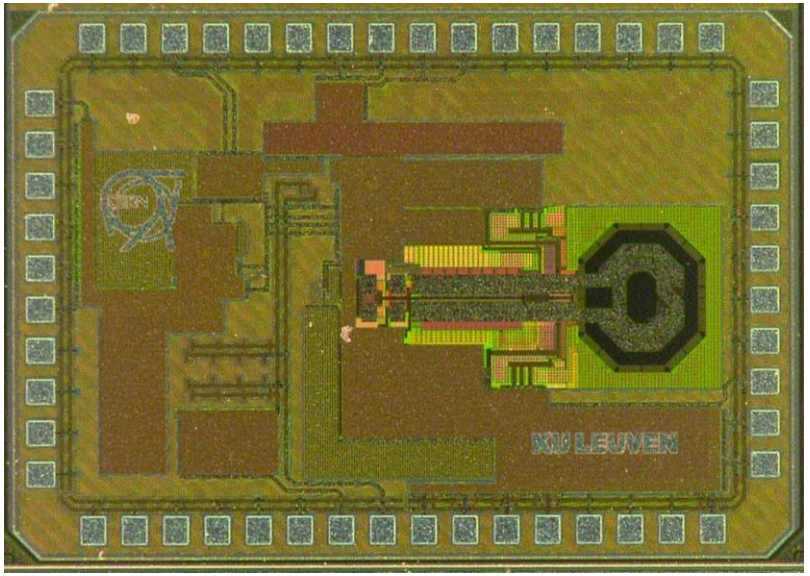
Backup Slides

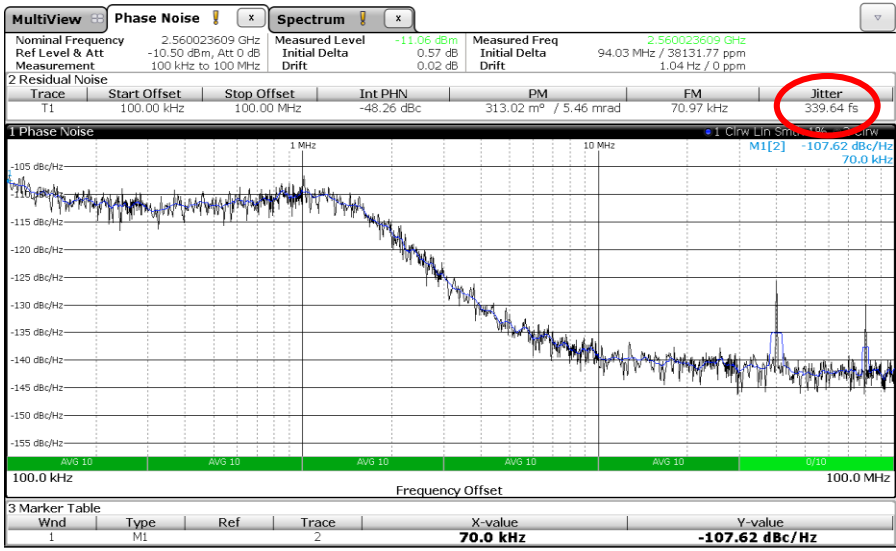
picoTDC Architecture



Low Jitter PLL

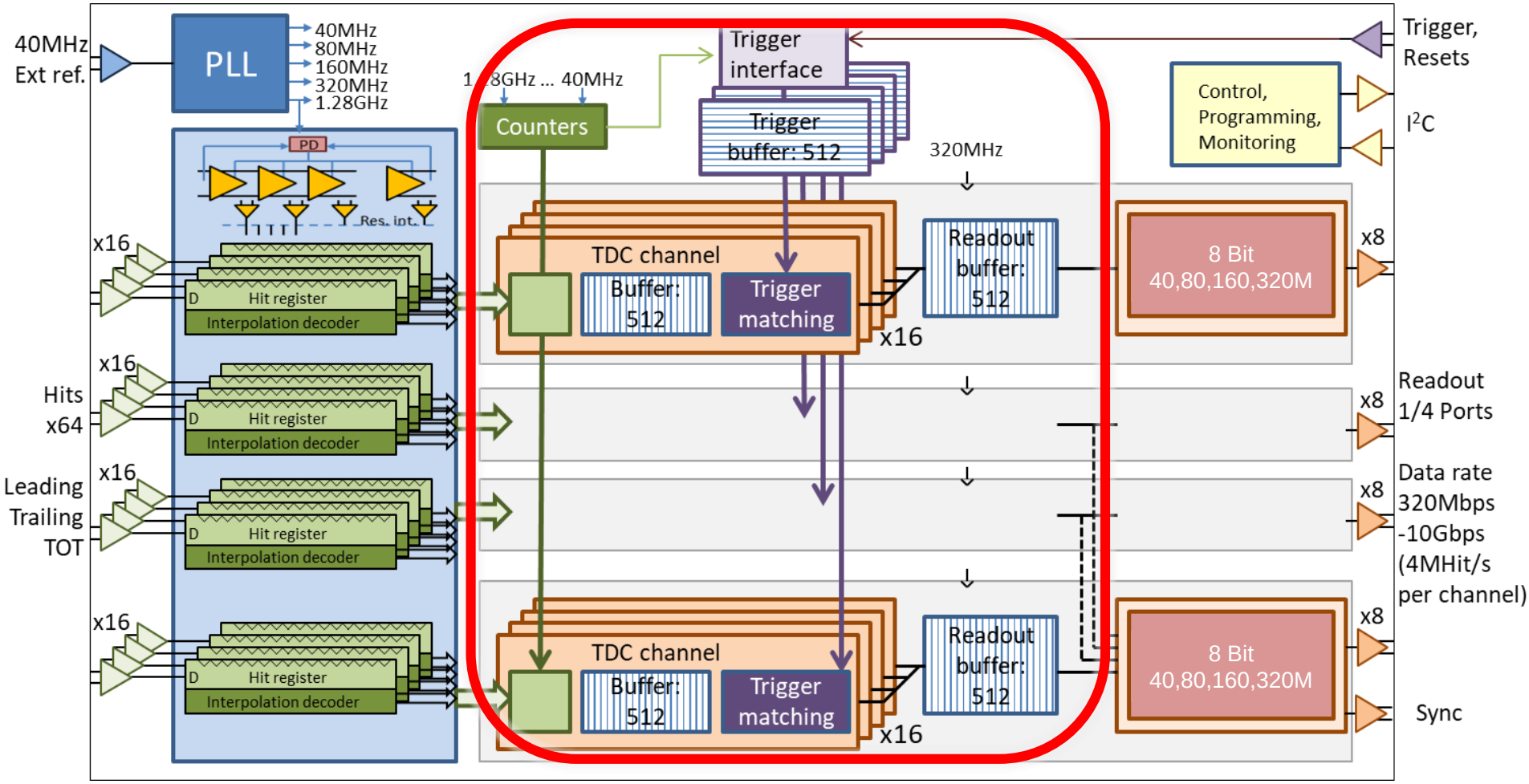
- Clock multiplication from 40MHz to 1.28 (2.56) GHz
  - Low jitter critical
  - Jitter filtering of 40MHz clock to the extent possible
    - 40MHz reference MUST be very clean
  - LC based oscillator
- Prototyped & Tested
- Measurements very promising (340fs RMS jitter)
- Designed by Jeffrey Prinzie, KU Leuven
- Talk at TWEPP 2015:
  A low jitter PLL frequency synthesizer for high resolution TDCs in 65nm CMOS technology





Phase Noise vs. Freq. Offset

picoTDC Architecture



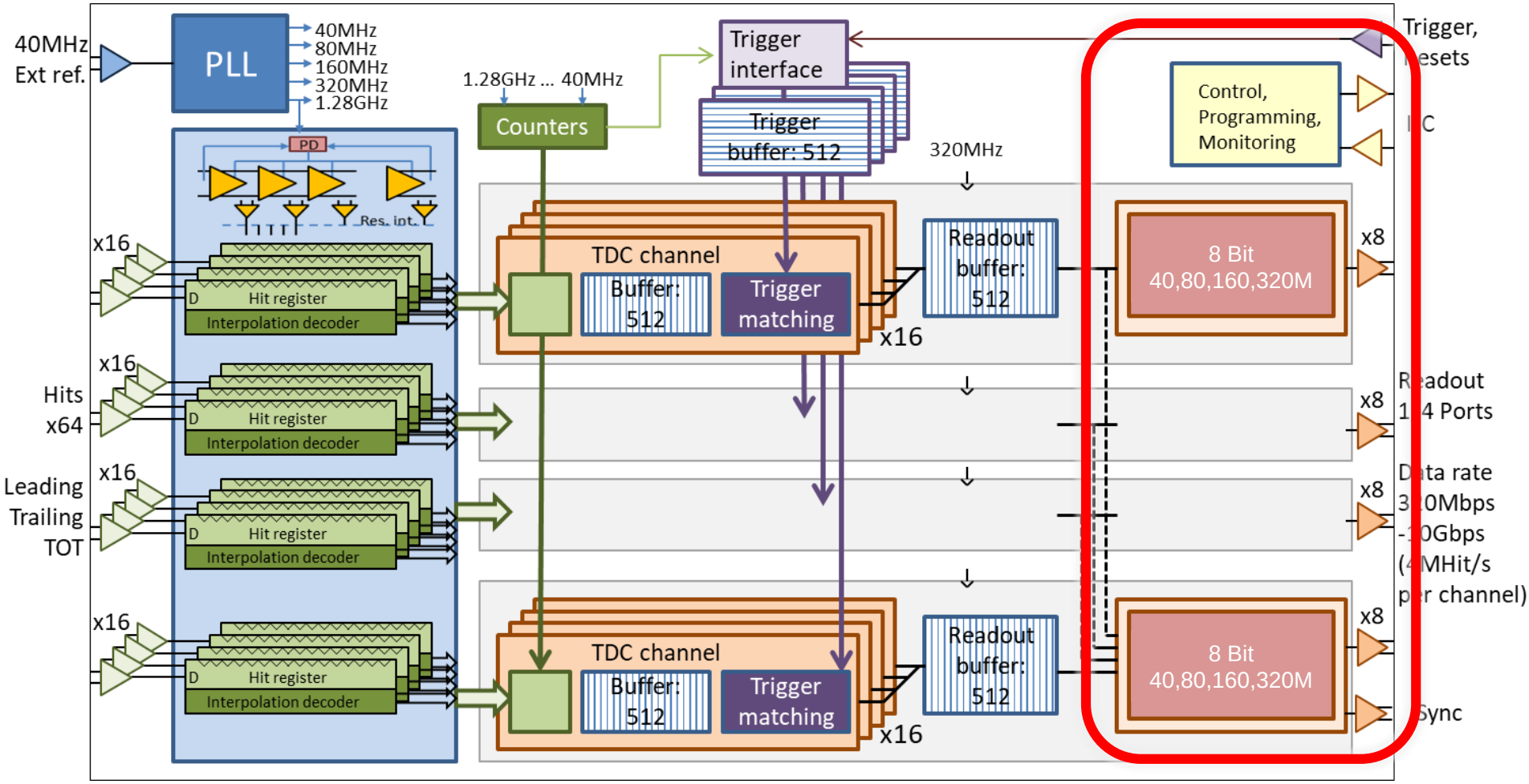
Constraints on Hit Signals

- One edge per 1.28GHz-Cycle (~0.8ns)
- Internal analog glitch filter after hit receiver
  - Filter time can be programmed to ensure 0.8ns
  - Or up to 10ns for filtering e.g. oscillations
- Small derandomizer (4 hits) for each channel running @1.28GHz
- Sustainable rate to channel buffer 320MHz, trigger matching running @320MHz for each channel separate

Logic Features

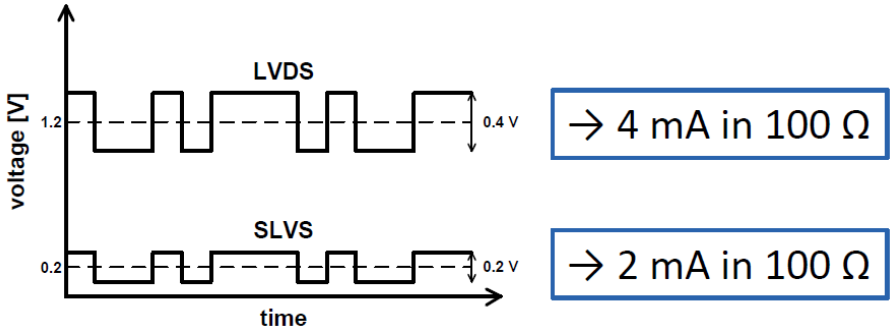
- Triggered with configurable latency and length, overlap possible, or untriggered
- Naturally overflowing counter used for calculating trigger matches, TOT etc.
- Counter with arbitrary overflow and reset for machine cycle, can be inserted in event headers when triggered

picoTDC Architecture



Electrical Interfaces

- Hits: Differential (LVDS “compatible”, common mode from 0.2V to 1.2V)
  - Highest speed (resolution) @ ~800mV common mode
- Time reference: 40MHz differential
  - Low jitter reference critical for high time resolution
- Trigger/Event-Rst/BX-Rst/Reset: Sync Yes/No
- Control/monitoring: I^2C at CMOS 1.2V-levels
- Readout: 4 readout ports of 8 differential signals
  - Common mode 0.6V, programmable current 1-5mA
  - Compatible with LpGBT and FPGAs
- Packaging: 400 BGA (1mm pitch)



Config / Control / Status Interface

- I^2C Interface, up to 1MBit/s
- 1.2V CMOS Levels
- 348 Bytes configuration / control
  - Additional 322 bytes delay adjust
- 300 Bytes status

Readout

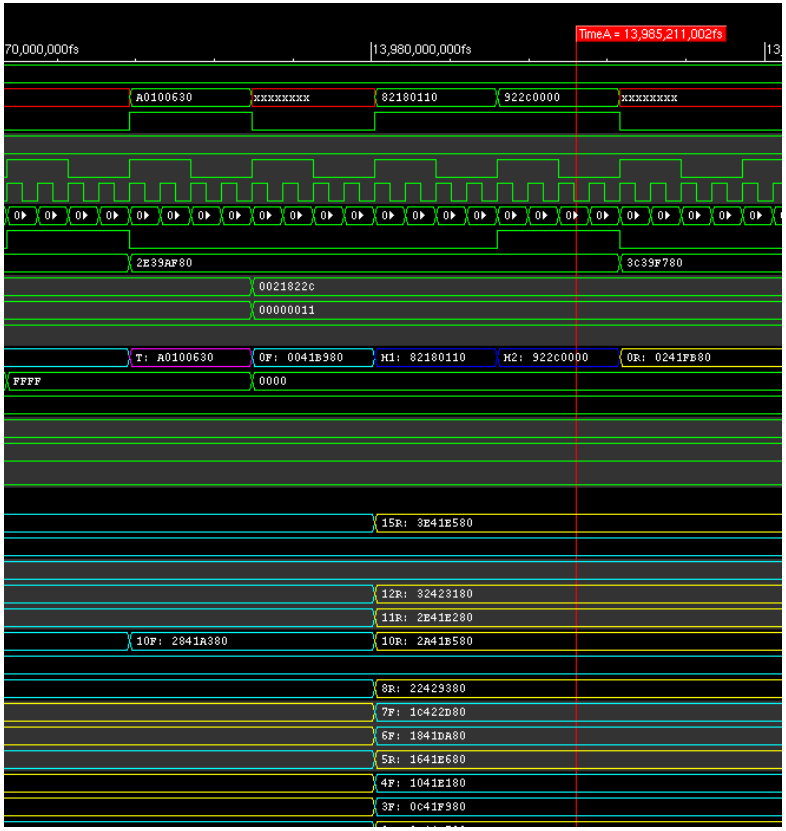
- 1 or 4 differential readout ports with 8 bits
  - 40 - 320MHz
  - Bandwidth:
    - Min 320Mbits/s (~0.15 Mhits/s per channel)
    - Max 10Gbits/s (~4 Mhits/s per channel)
- Readout data: 32 bit words
  - TDC data, headers, trailers etc.

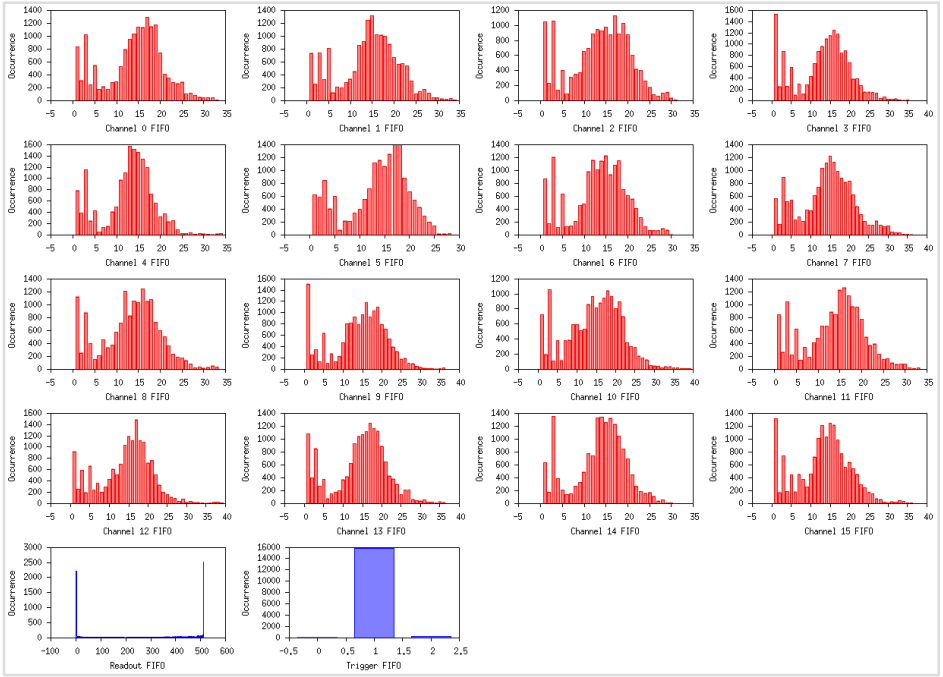
Estimated Power Consumption

Dependent on hit rate, values based on 1 MHz per channel

- High resolution, 64 channels: 1300mW
- High resolution, 32 channels: 900mW
- Low Resolution, 64 channels: 850mW
- Low Resolution, 32 channels: 550mW

Verification Environment






```
Matching trigger header:  911  27
Matching trailer:    27 101 hits
Matching trigger header:  925  28
Matching trailer:    28 107 hits
Matching trigger header:  942  29
!   23573019ps: Missing  Rising  hit at channel          1
!   23591087ps: Missing  Falling hit at channel          5
```

- Verification in SystemVerilog
- Use cases can be defined and automatically tested, visualization of buffer occupancy, lost hits etc.

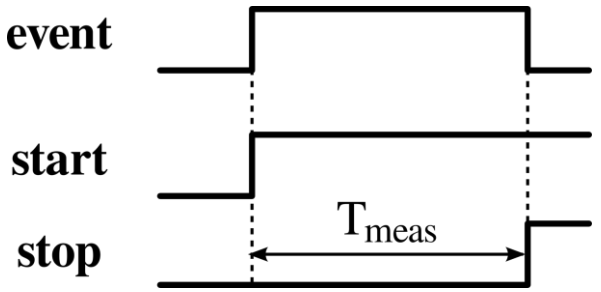
Verification Features

- Environment supports and verifies all TDC features
  - Triggered / untriggered
  - Rising / rising&falling / TOT
  - Different counter and reset settings
- Extensive test cases
  - High / low / burst hit rate
  - High / low trigger rate, overlapping triggers
- Specific use cases can be defined, verified

Measurement Scheme

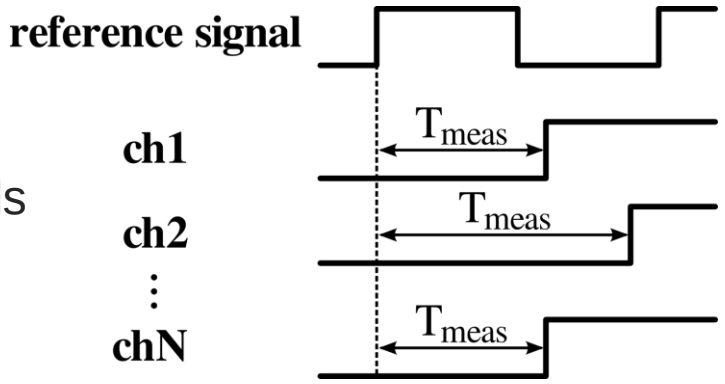
Start - Stop Measurement

- Measure relative time interval between two local events
- Small local systems and low power applications

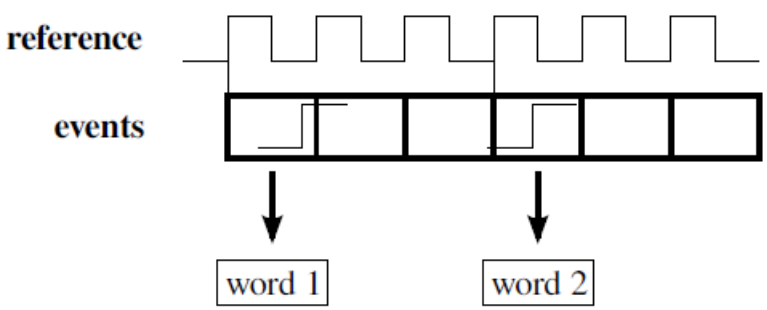


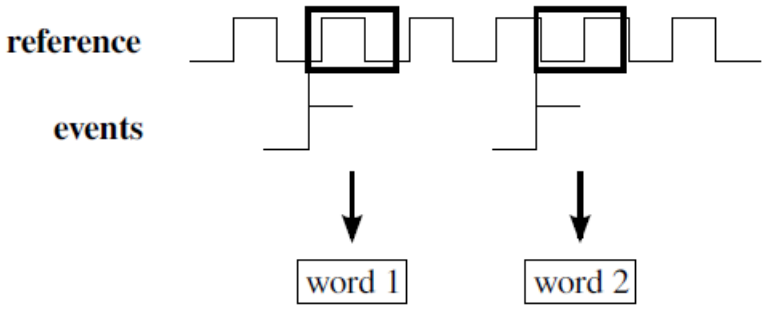
Time Tagging

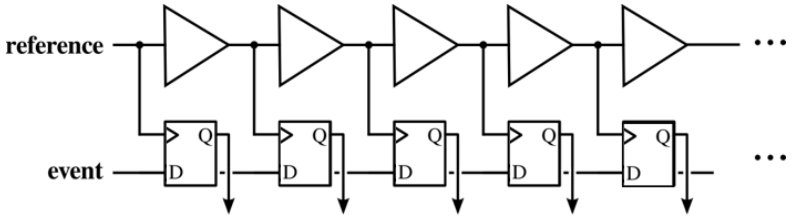
- Measure “absolute” time of an event (Relative to a time reference: clock)
- For large scale systems with many channels all synchronized to the same reference

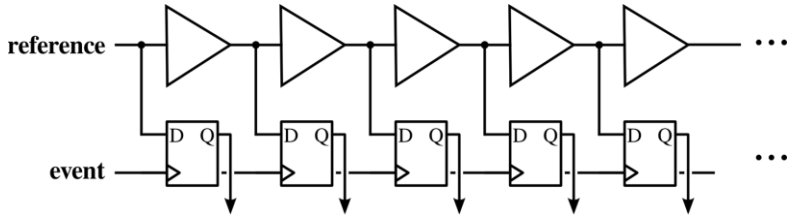


Capture Scheme





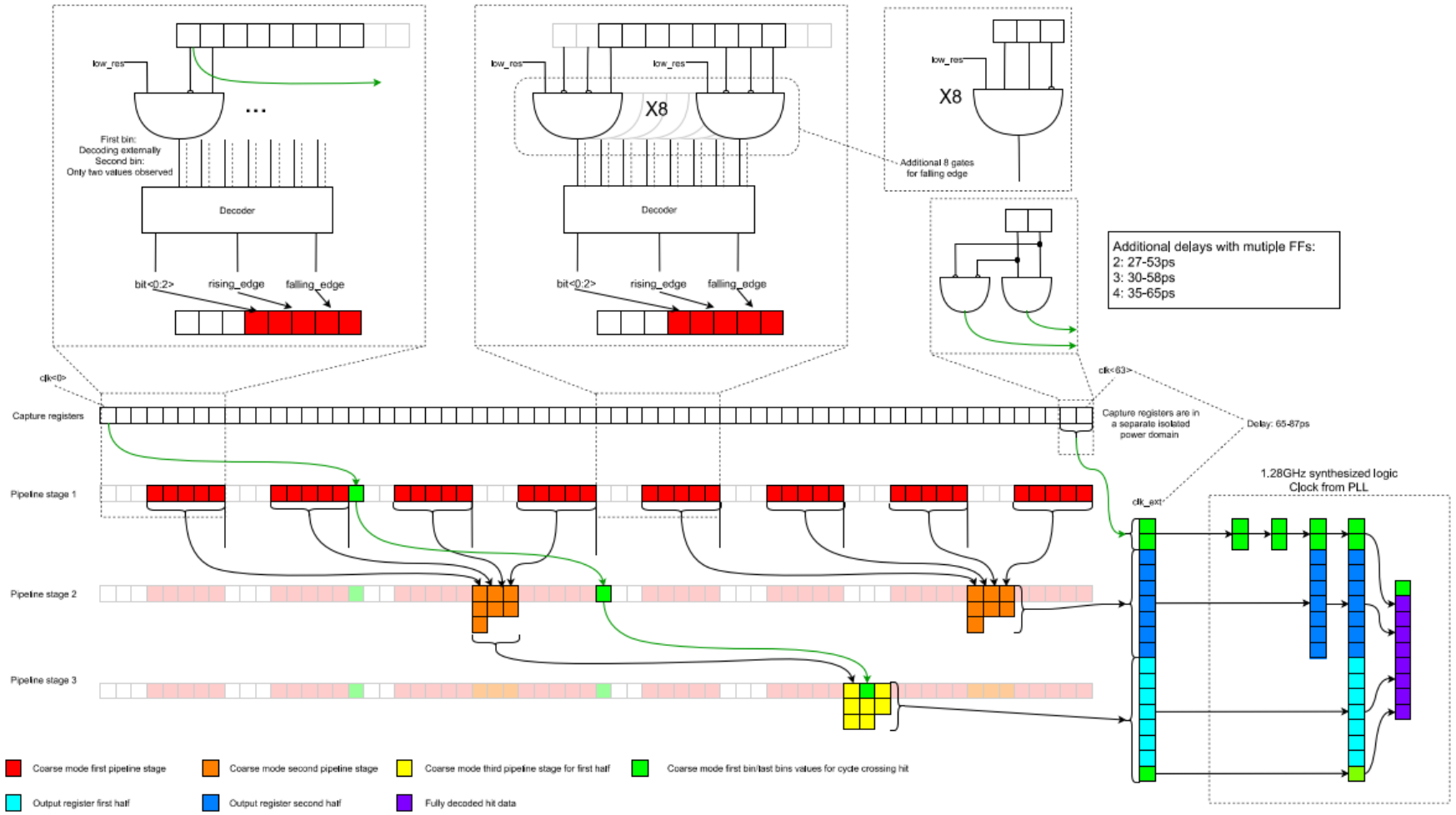




Synchronous

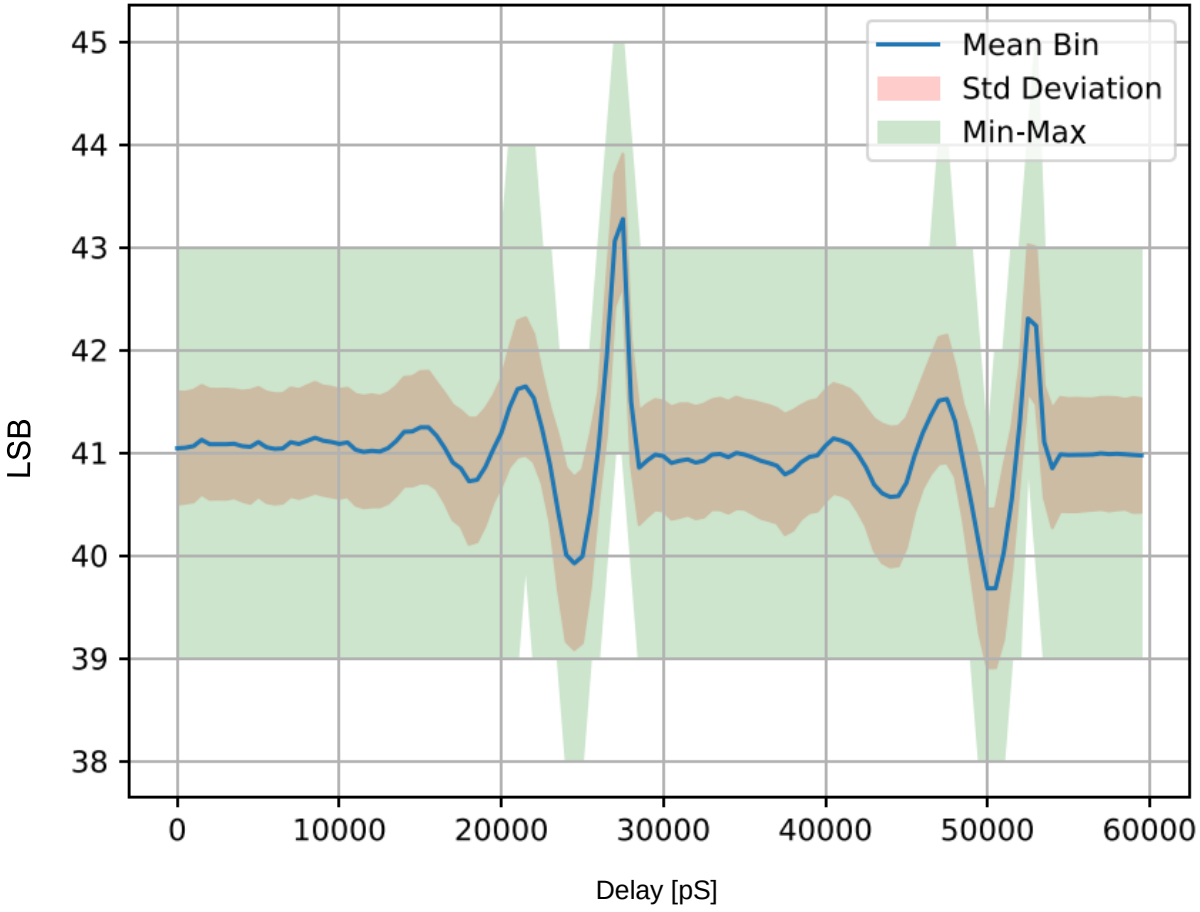
Asynchronous

Coarse Decoding in Timing Macro



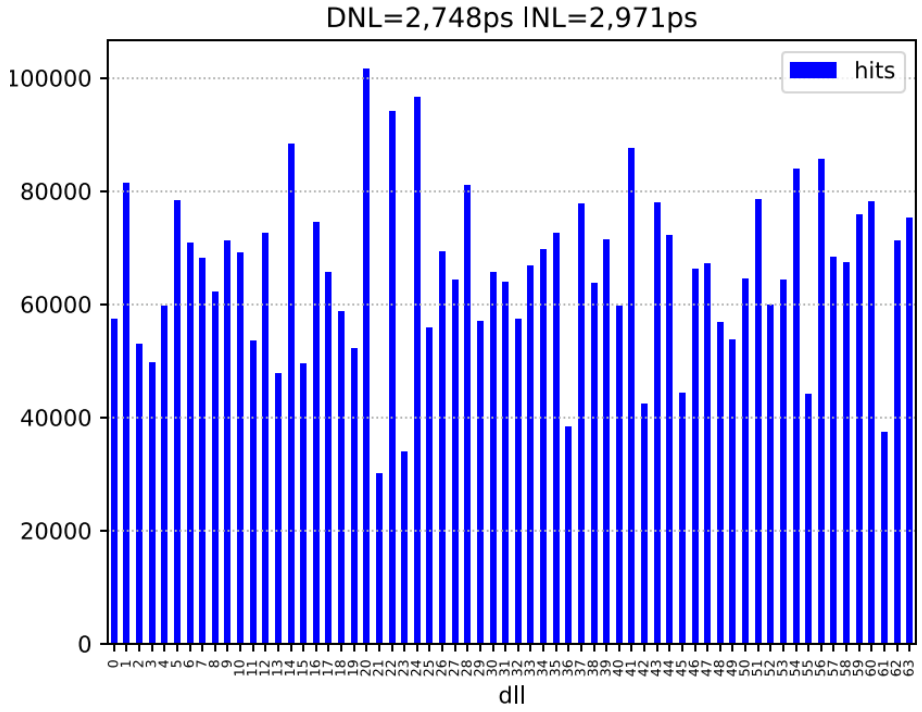
Crosstalk Test

Channel 31 vs. all channels, coarse mode, LSB 12ps

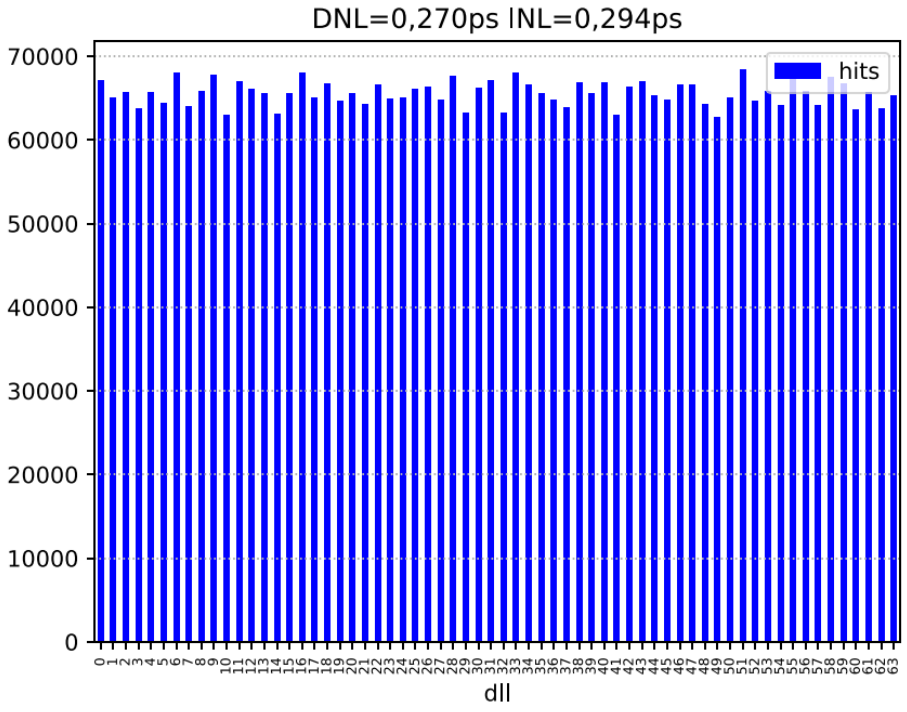


12ps Bin Code Density Test

Not adjusted



Adjusted



25ns Sweep Deviation