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picoTDC: A 3ps bin bize 64 channel TDC for HEP experiments

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We present the ASIC development and test results of the picoTDC, a 64 channel time tagging TDC with 3ps bin size. The ASIC runs from a single 40MHz reference clock, can be configured very flexible, supports hit rates of up to 320MHz per channel, internal buffering and trigger matching as well as TOT measurements. A prototype has been produced in a 65nm CMOS technology and first test results show a single-shot RMS resolution better than the bin size (3ps).

Summary

A 64 channel time tagging Time-to-Digital Converter (TDC) ASIC with 3ps bin size, the picoTDC, has been implemented, submitted and tested.
In the picoTDC, an external 40MHz reference clock is fed to a PLL generating an internal 1.28GHz reference. This reference is split into 256 phases through a 64 element DLL and a resistive interpolation resulting in the 3.05ps bin size. These clock phases then drive the capture registers of the 64 channels. To reduce the power consumption, the resistive interpolation can be disabled resulting in a bin size of 12.2ps.
The TDC can digitize one edge in each 1.28GHz clock cycle (781ps) which are then (through a small derandomizer) fed to a channel buffer which can hold 512 hits per channel. The digital logic of the ASIC (including the memories) is clocked at 320 MHZ which is thus the maximum hit rate that can be sustained from each channel to the channel buffers. The readout interface consists of four eight bit parallel interfaces with up to 320MHz data rate, resulting in a maximum readout rate of 10GBit/s or 320 million hits per second for the whole ASIC. In order to reduce the required readout bandwith, a trigger functionality is implemented to read out only the interesting hits. For applications where this is not feasible, the data can also be read out triggerless. The ASIC also supports pairing of leading and trailing edges to a TOT measurement in order to reduce the readout bandwidth.
The TDC has been prototyped in a 65nm CMOS technology. First test results show an effective single-shot RMS resolution better than the bin size (including measurement jitter), but a higher mismatch between bins than anticipated. For the submission of the final production version the mismatch will be improved.
This paper discusses the circuit architecture, its principles of operation, test results and their implications from the prototypes as well as improvements for the production version. Detailed measurements and functional tests will be available at the time of the conference.

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