A 4-Channel 10-Gbps/ch CMOS VCSEL Array Driver with on-chip Charge Pumps

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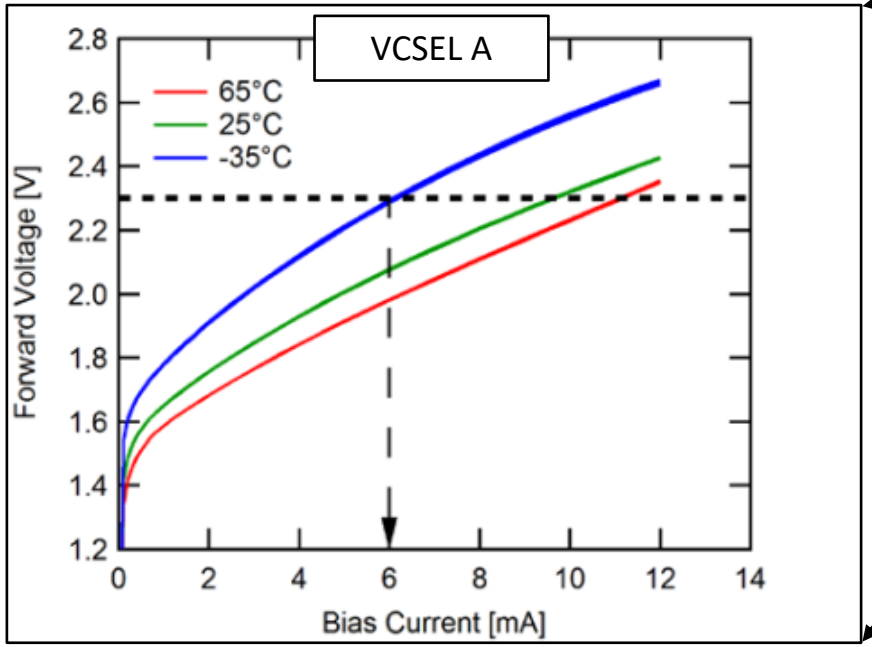
Outline

- Motivation
- Design of charge-pump VCSEL Array Driver (cpVLAD)
- Measurement results
- Summary

Motivation

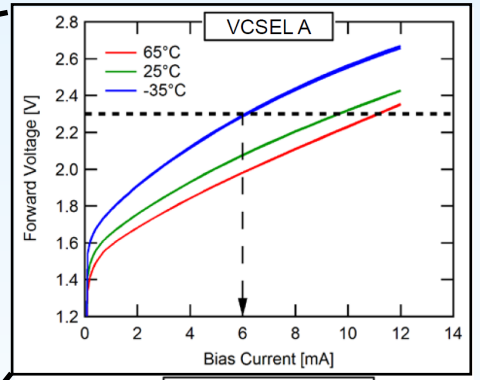
Jan Troska's presentation in TWEPP 2017: https://indico.cern.ch/event/608587/contributions/2614150/

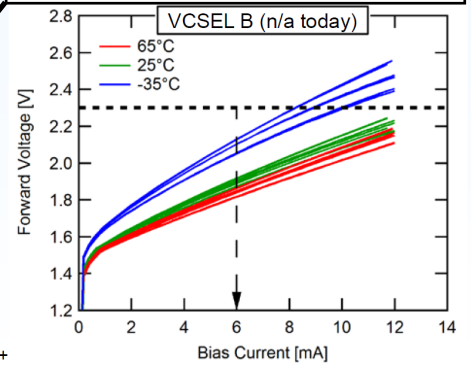
Low temperature and radiation increase the VCSEL forward voltage and compress the headroom.

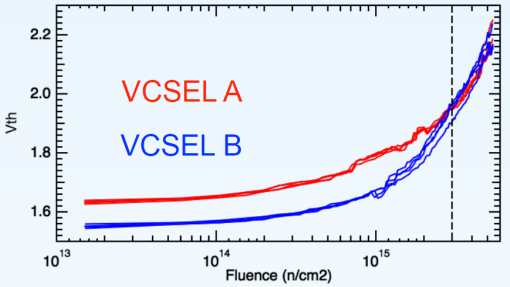


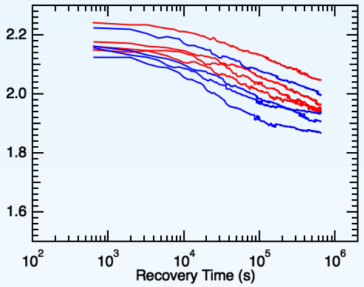
Design challenges

- Largest unique challenge comes from ensuring sufficient voltage headroom for operation of VCSELs with 65 nm CMOS driver that limits voltage rail to 2.5 V









- Going cold and irradiating the VCSEL make the situation worse
  - VCSEL forward voltage increases
- Need some voltage headroom for the driver's output transistor
- Currently validating the margin we have for operation

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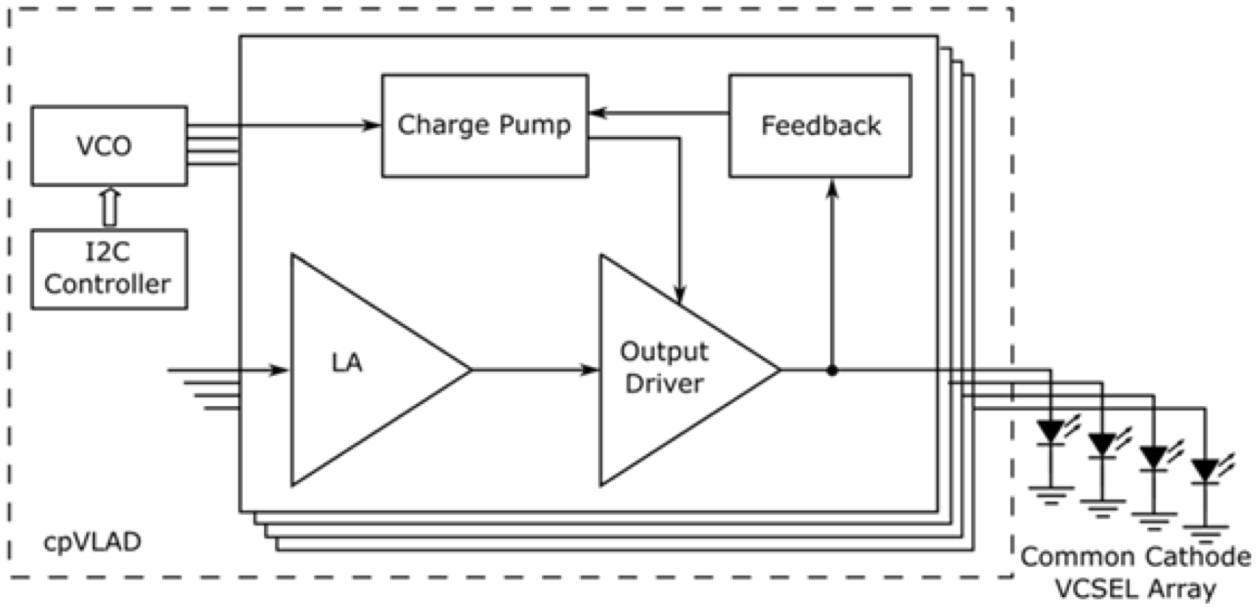
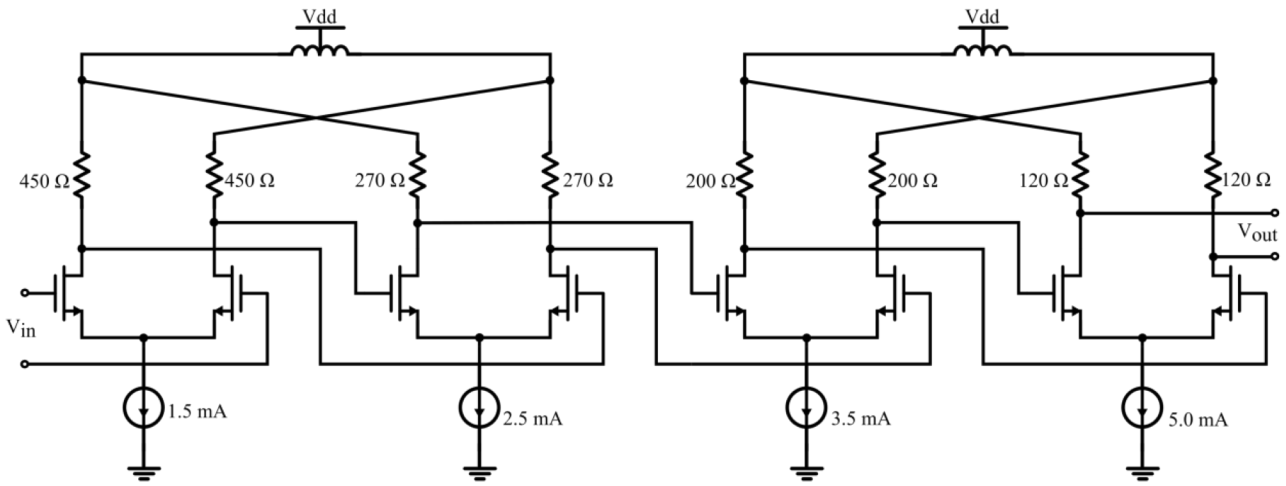
Diagram and key features

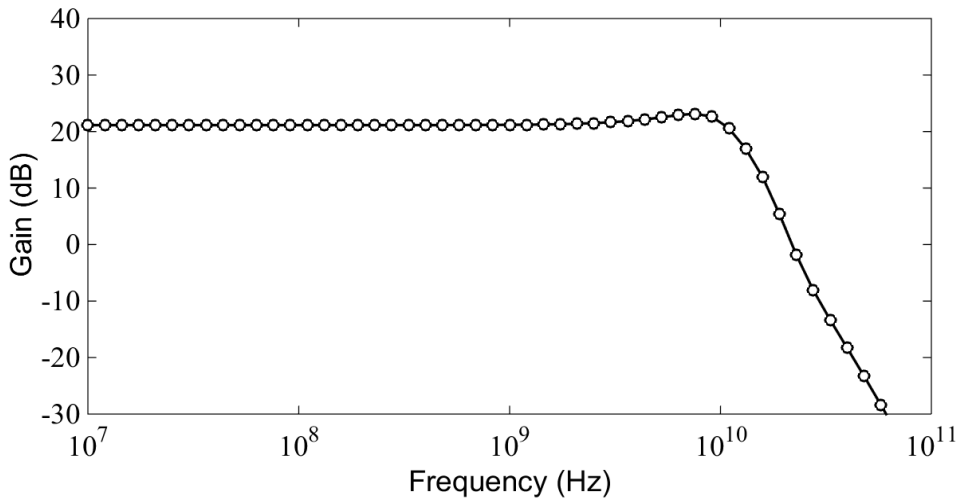
Power supplies:
1.2 V and 2.5 V



- The on-chip charge pump generates a voltage higher than 2.5 V for each output driver.
- The feedback circuit adjusts the output voltage of the charge pump so that when the forward voltage of the VCSEL diode, the CP output voltage changes accordingly.
- A shared VCO provides a clock signal for each charge pump.
- Only 1.2-V core devices are used in the whole design for radiation tolerance. Careful checks are performed to make sure no overdriving violation.

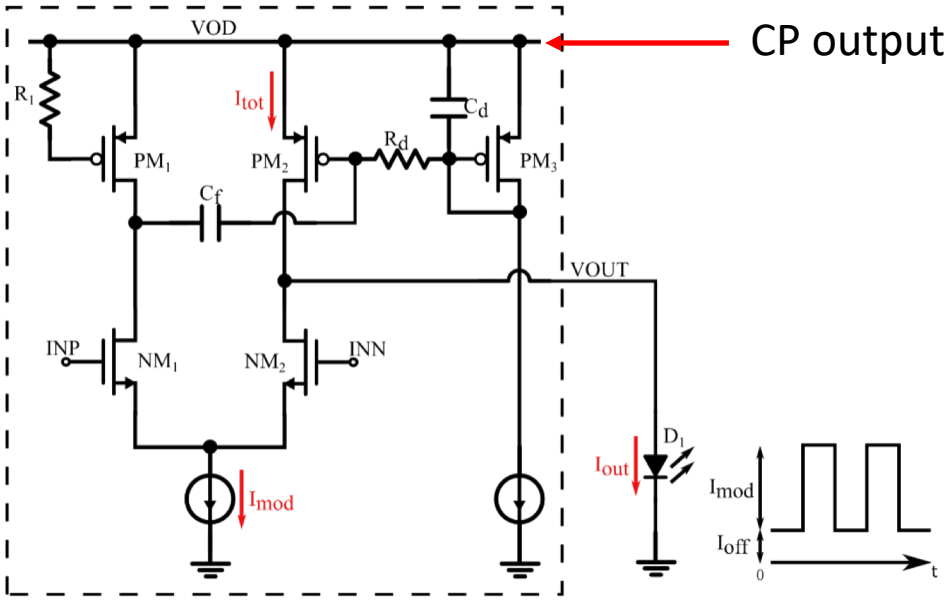
Design of limiting amplifier (LA)



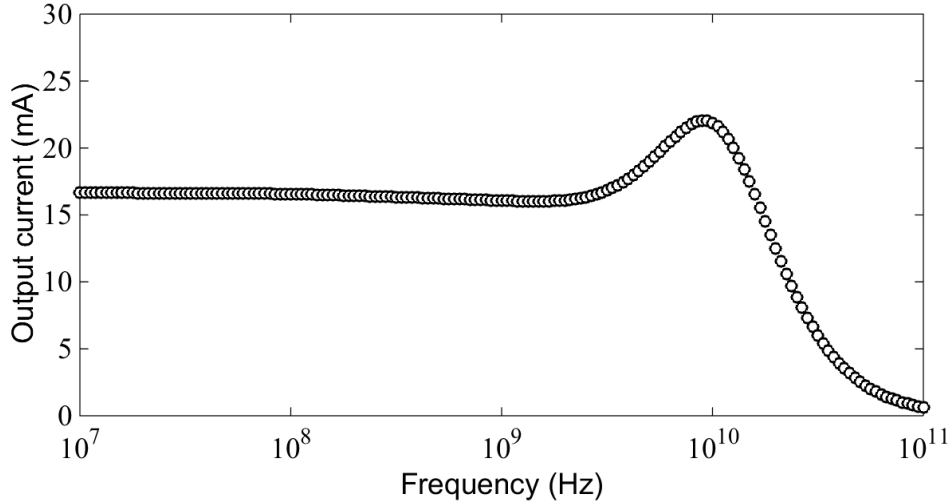


- A four-stage LA amplifies the signal amplitude from 100 mV to 800 mV (peak-peak).
- Two amplifiers share a peaking inductor to save the chip area.
- The overall LA achieves a total gain of 21.5 dB and a bandwidth of 12.0 GHz with a power consumption of 15 mW at the typical corner, 1.2 V, 27 ^{o}C.

Design of output driver



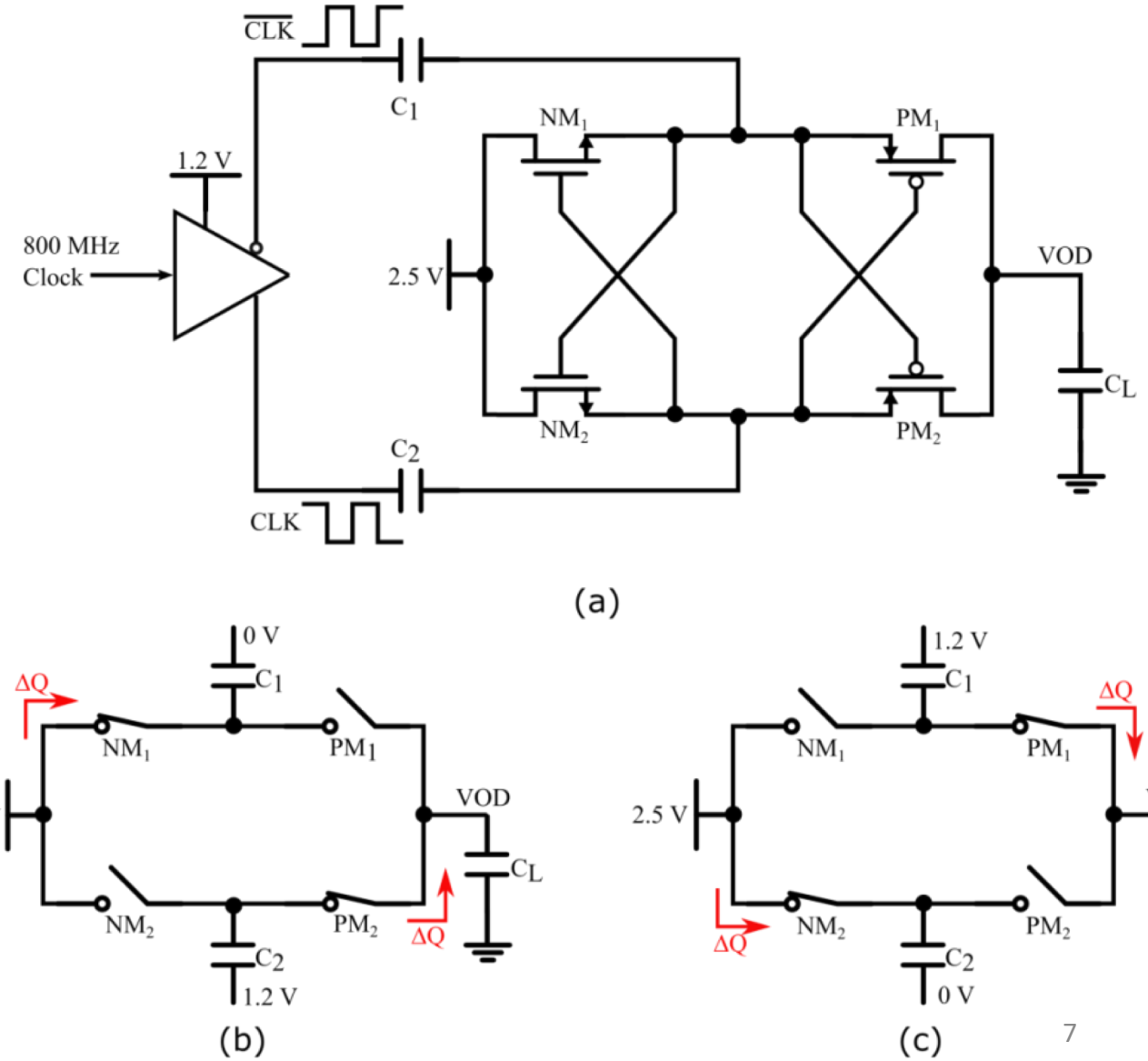
CP output voltage



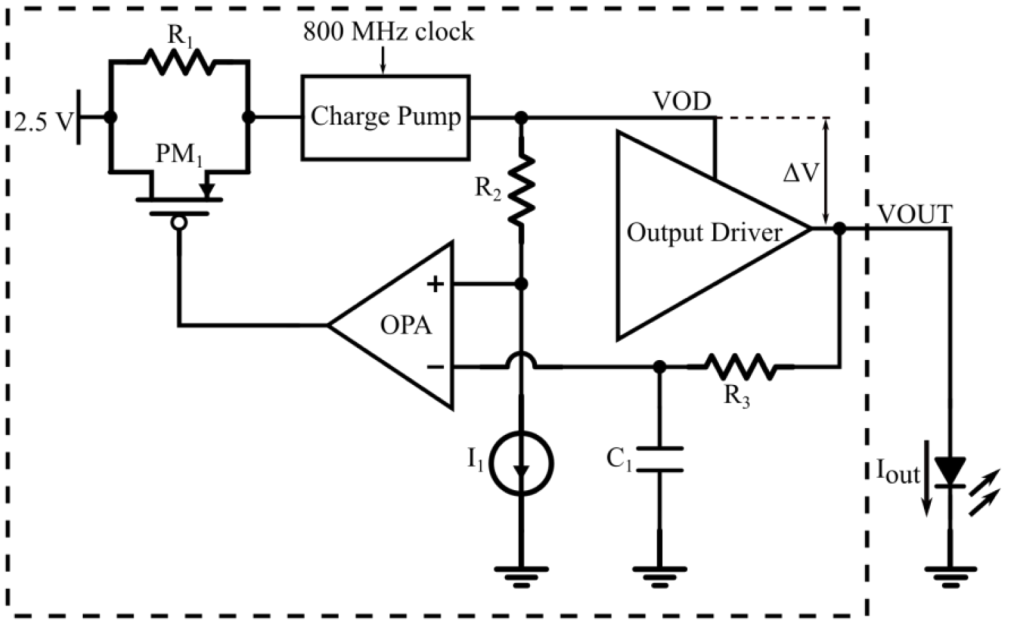
- The output driver receives the differential outputs from the LA and provides the bias current and the modulation current to the laser diode.
- The bandwidth shown in the figure is 20.3 GHz at the typical process corner, 2.5 V, 27 ^{o}C.

Design of charge pump

- The charge pump uses cross-connected NMOS and PMOS transistors driven by an 800 MHz 1.2 V clock from the VCO to boost the 2.5 V power supply to a higher voltage for the output driver.
- The 800 MHz clock comes from the VCO. The frequency is chosen to reduce capacitor area and voltage ripple.



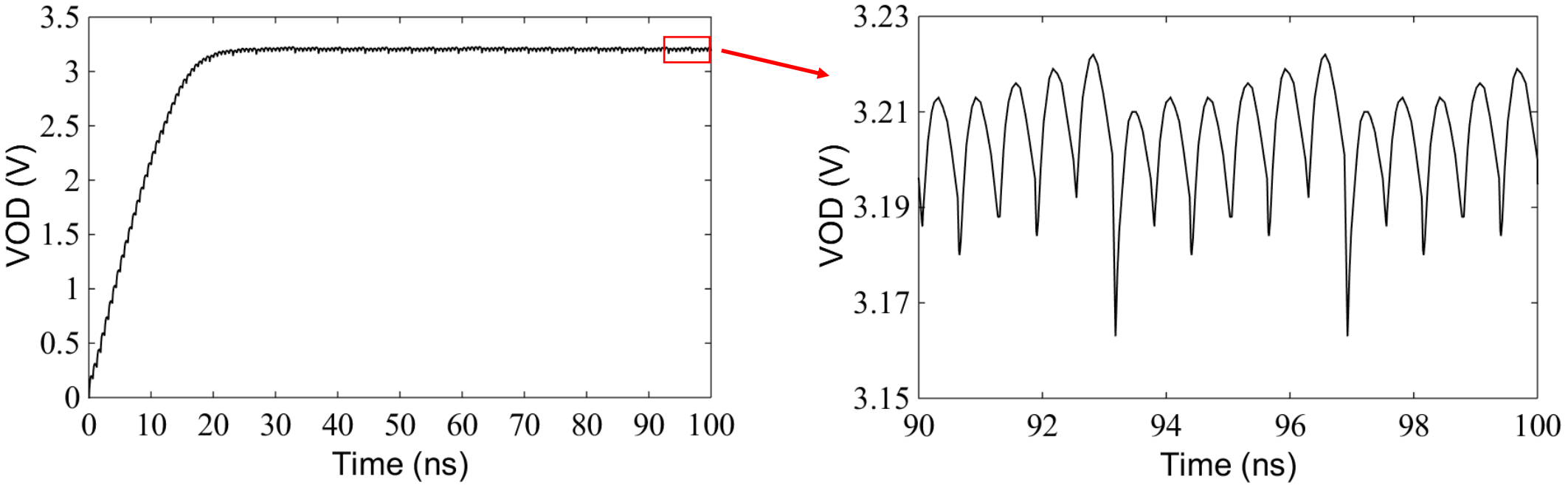
Design of feedback circuit



$\Delta V = I_1 \cdot R_2$
I_1 is programmable

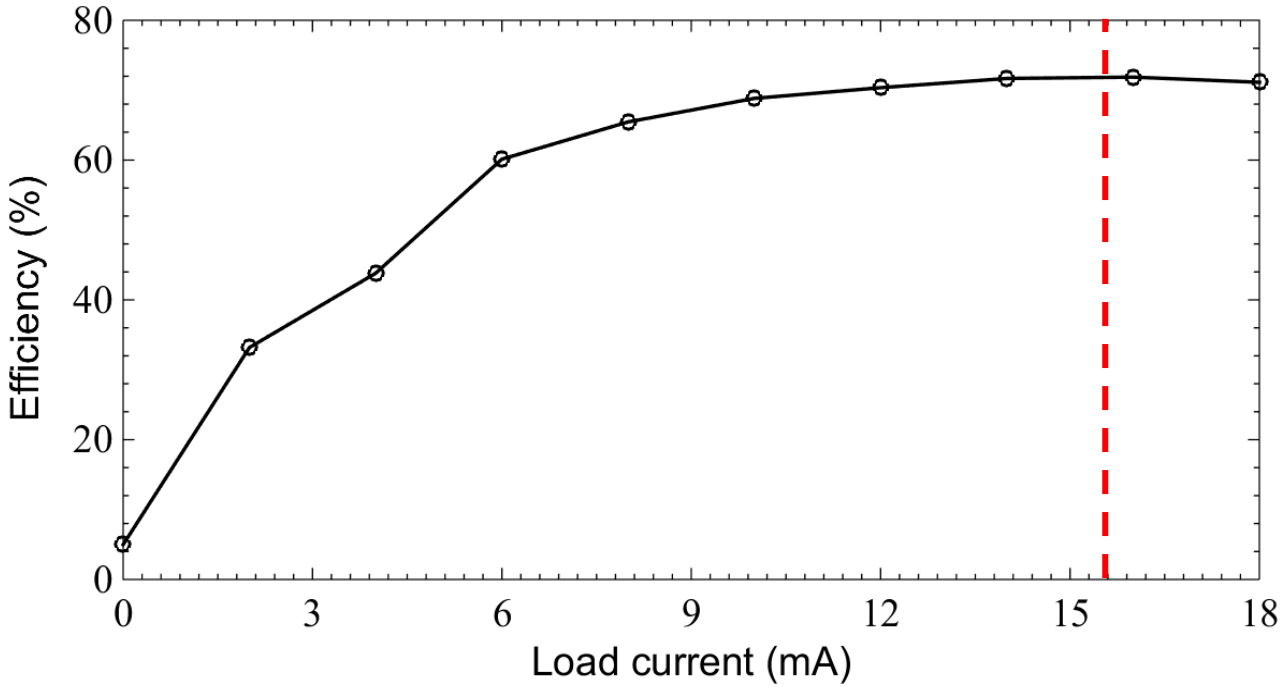
- The negative feedback circuit keeps the voltage difference between the CP output and the anode of VCSEL constant when the VCSEL forward voltage changes.
- The voltage difference is programmable.

Simulation of the charge pump power up



- In 30 ns after the power up, the output voltage of the charge pump settled to a steady voltage of about 3.2 V with a peak-to-peak ripple of 60 mV in a typical operating condition.
- An optimized combination of a load capacitor (155.4 pF) and an 800-MHz VCO frequency is chosen based on the area and process performance consideration.
- The final charge pump module takes an area of 200 um x 1000 um and is integrated into each channel of the cpVLAD.

Simulated efficiency of the charge pump

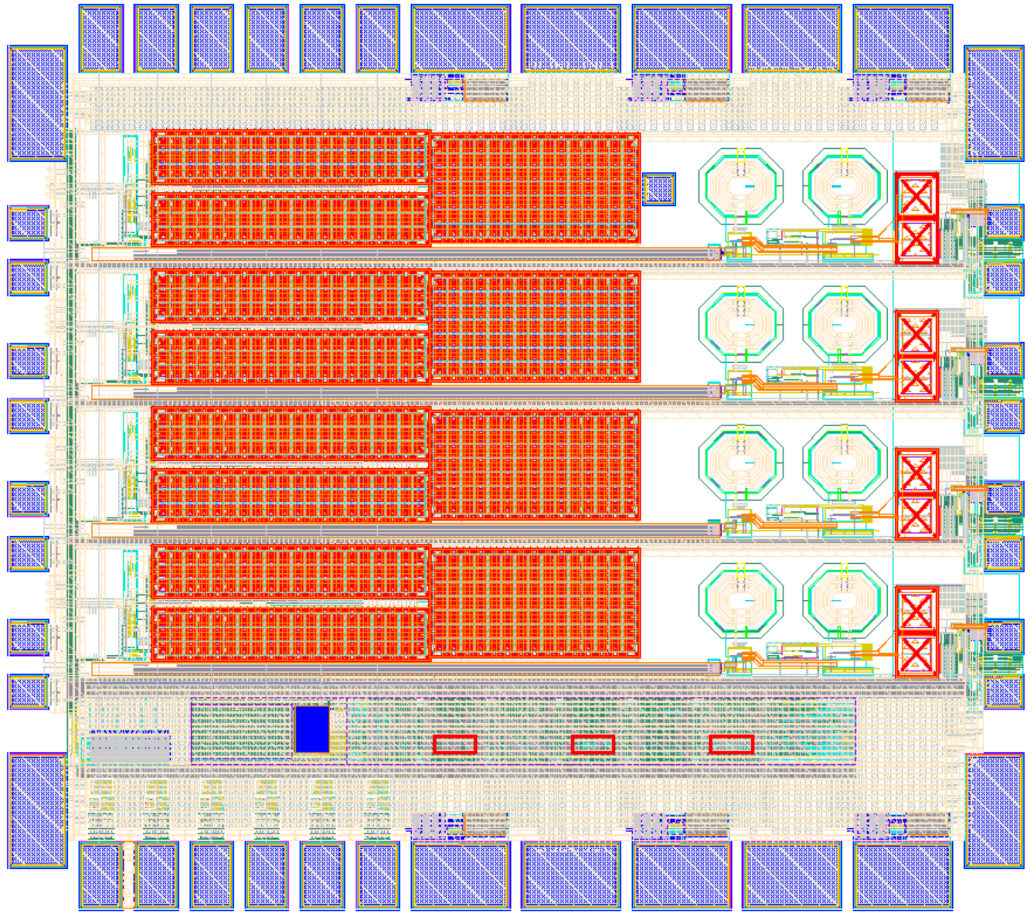


$$eff = \frac{V_{LOAD} \cdot I_{LOAD}}{VDD_{1.2V} \cdot IDD_{1.2V} + VDD_{2.5V} \cdot IDD_{2.5V}}$$

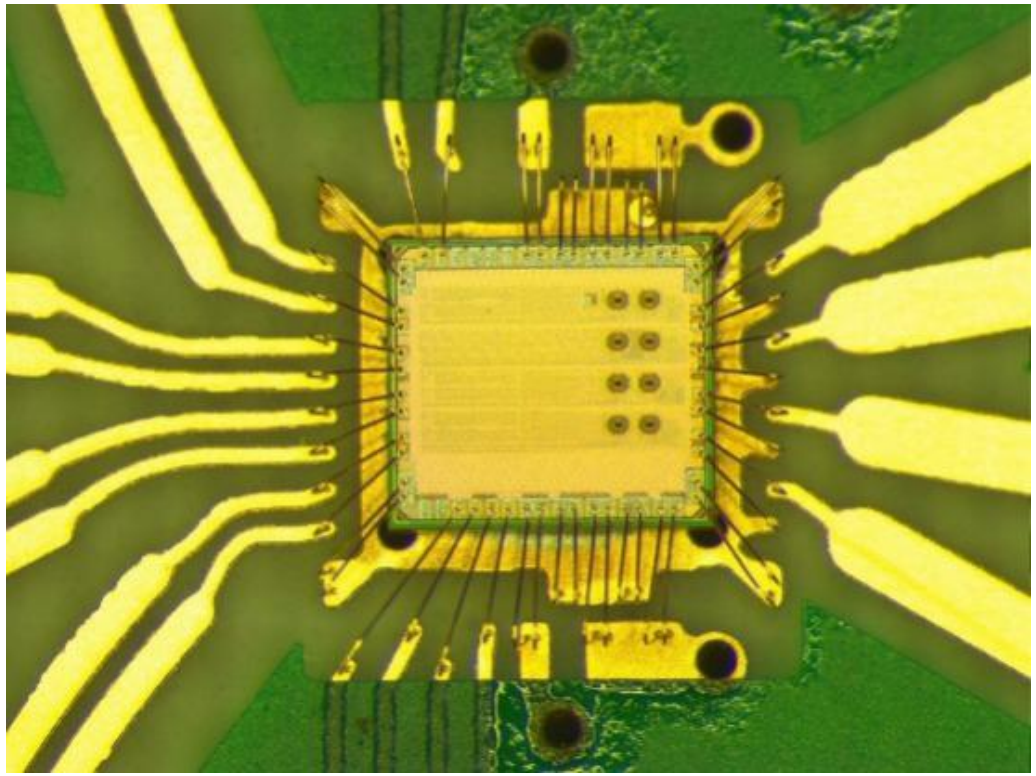
- When the load current is 16 mA, the power efficiency of the charge pump is 70.5 %.

Layout

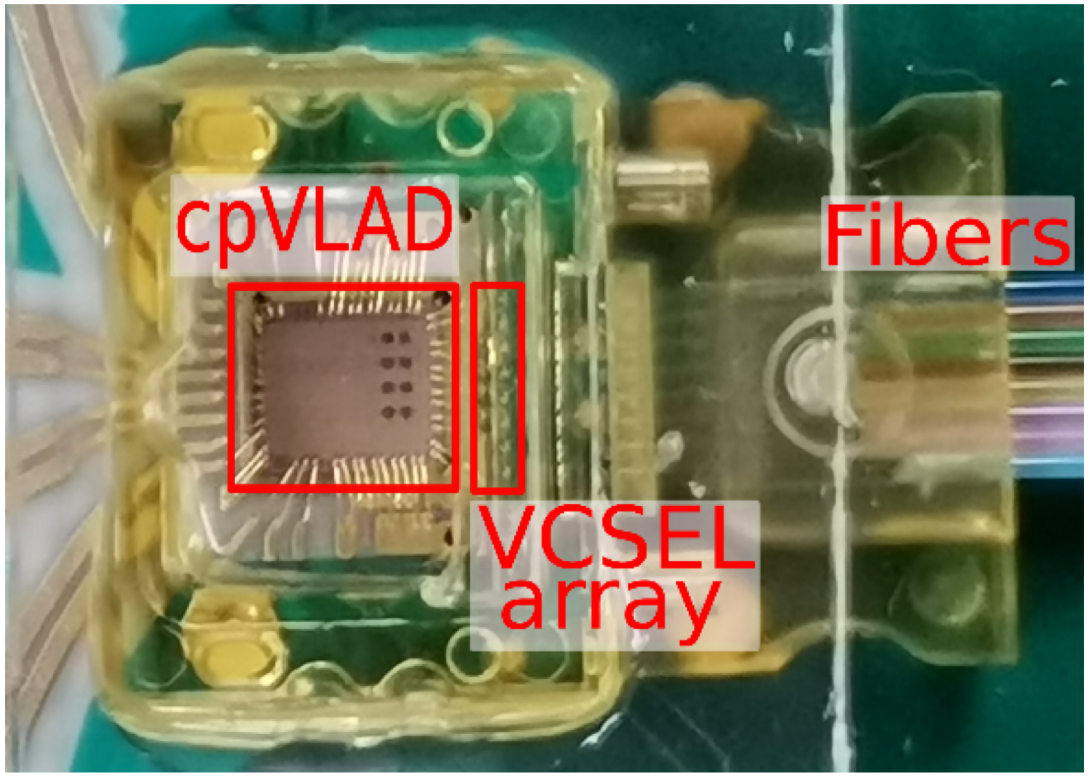
die 1.85 mm x 1.635 mm



Photographs of the cpVLAD



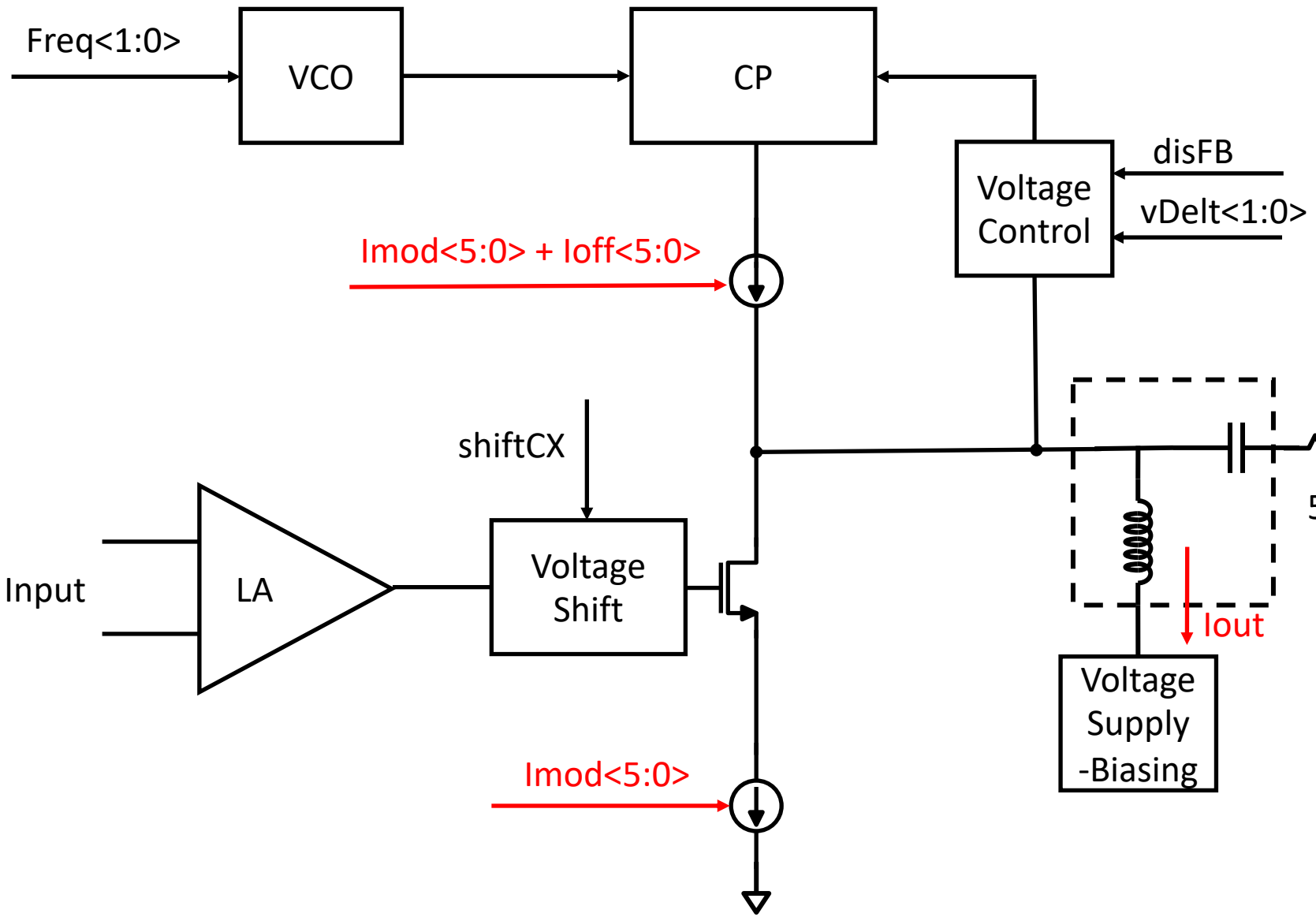
Electrical test boards



optical test boards

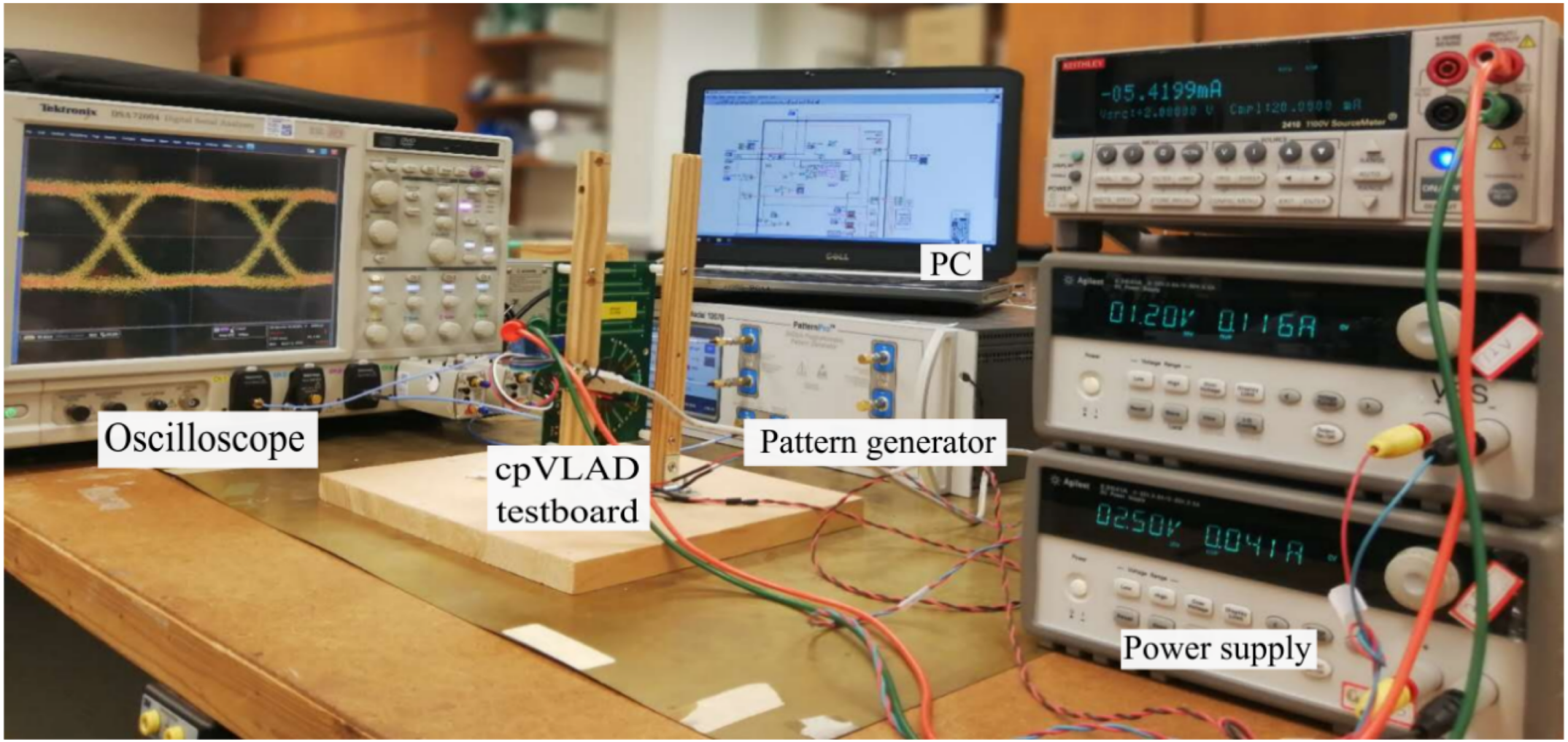
- Electrical test boards and optical test boards are assembled at CERN.

Block Diagram (ch1-3) – Electrical Test



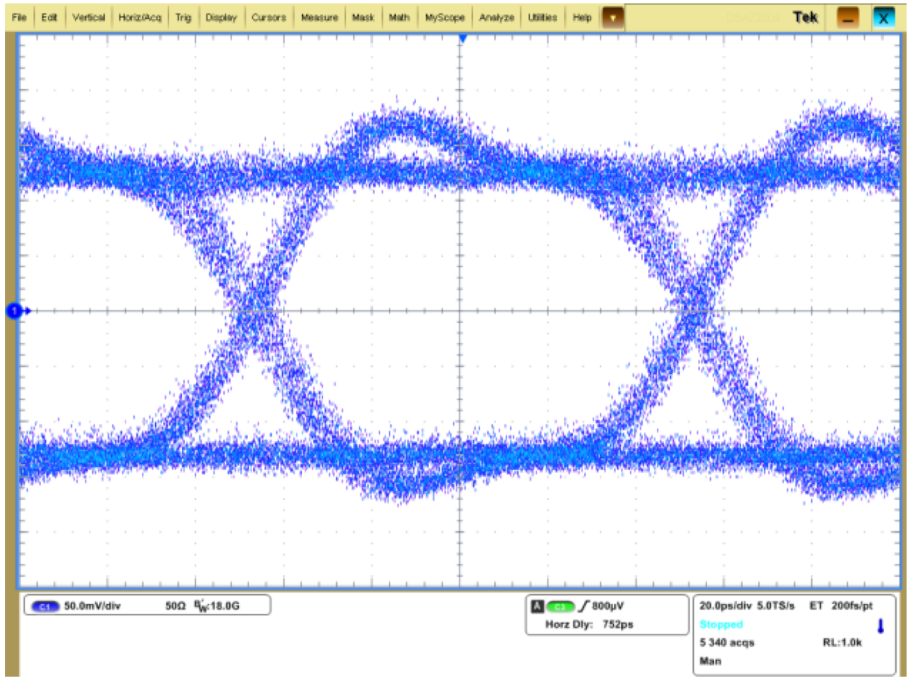
- A voltage power supply emulates the VCSEL forward voltage (Keithley 2410 is used, which can source or sink current).
- An oscilloscope is used to measure the output current over 50 Ω.

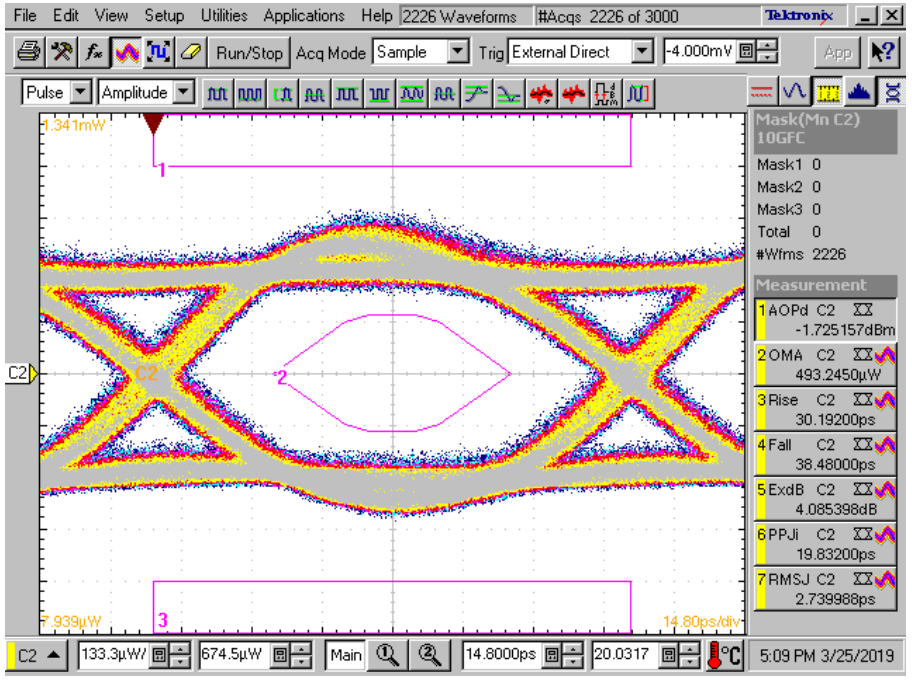
Test setup


Oscilloscope
cpVLAD
testboard
PC
Pattern generator
Power supply

Eye diagrams

Electrical



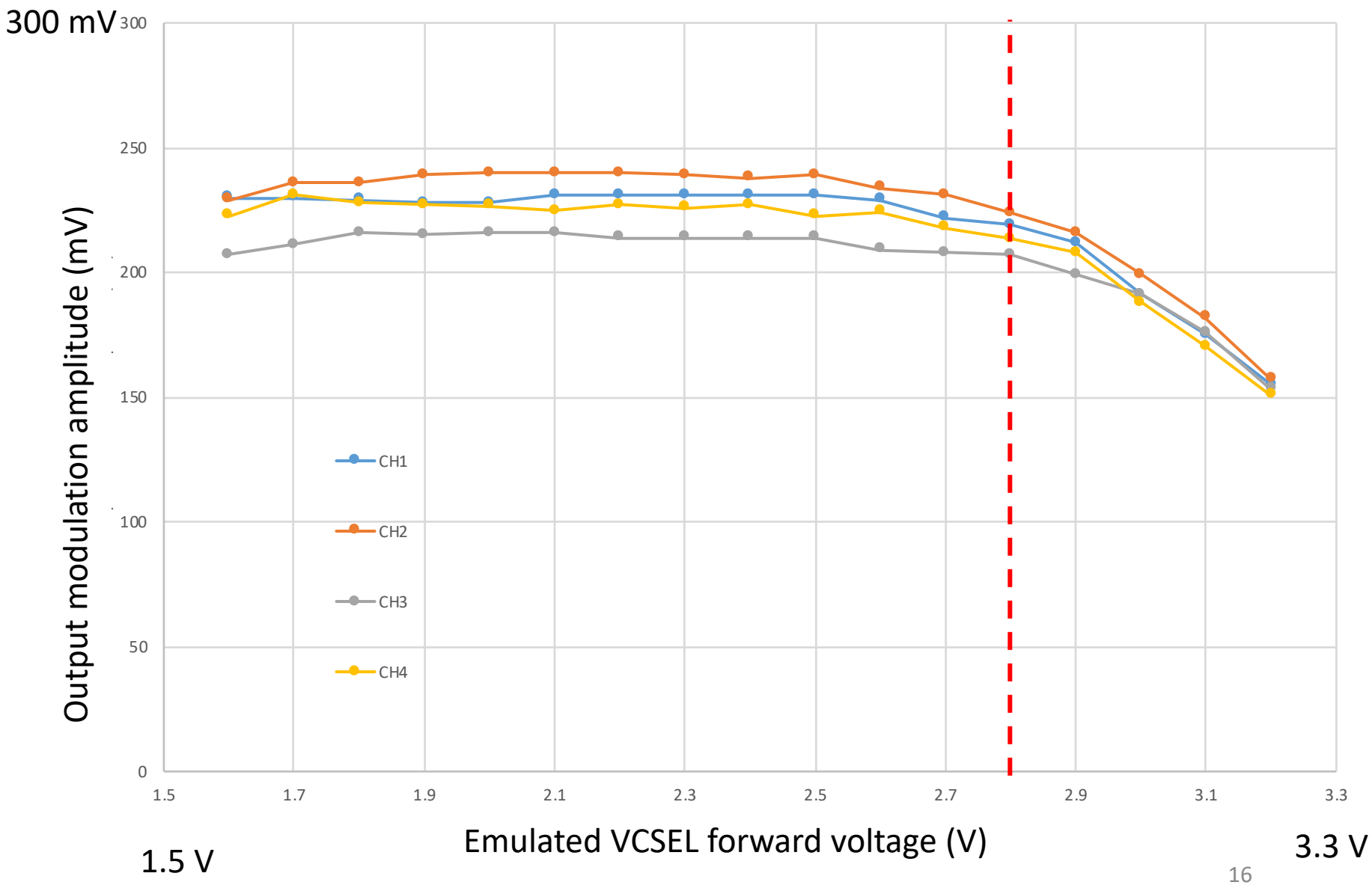


Optical

- Both the electrical and optical eye diagrams were measured at 10 Gbps with the input amplitude of single-ended 200 mV.
- The total jitter of the electrical eye diagram is 24.4 ps (peak-peak) at the Bit Error Rate (BER) of $1x10^{-12}$ with a random jitter of 0.91 ps (RMS).
- The tested average optical power (AOP) is -2.76 dBm. The optical modulation amplitude (OMA) is 373.67 µW.
- The power consumption of the cpVLAD is 79.5 mW/channel

Headroom improvement

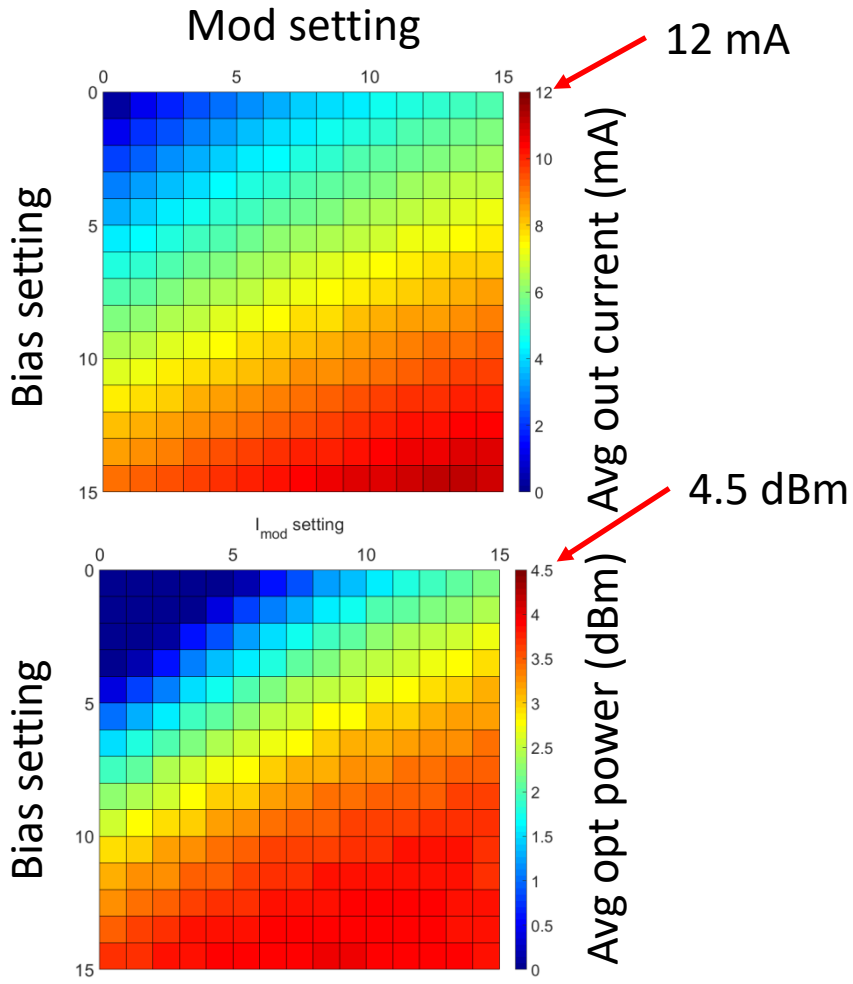
- The charge pump function was verified in the electrical test by increasing the DC voltage of the external bias-tee structure.
- The cpVLAD can survive up to 2.8 V forward voltage with a stable modulation output.

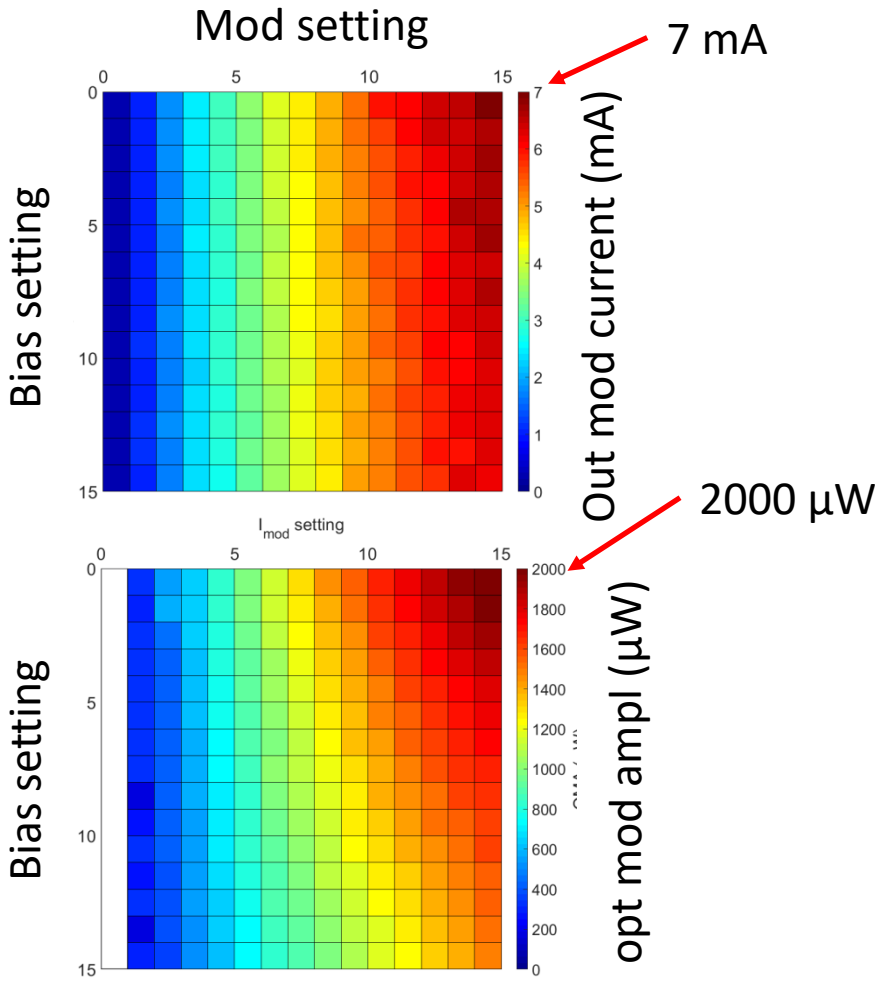


Current sweeping

Electrical board

Optical board

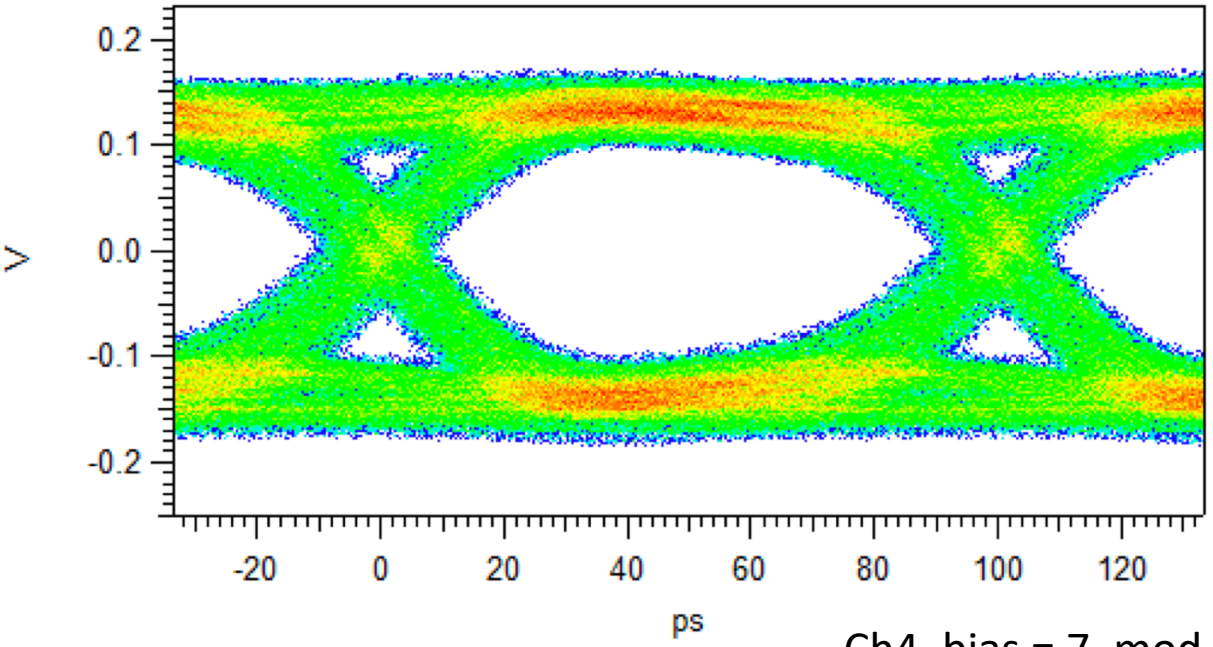




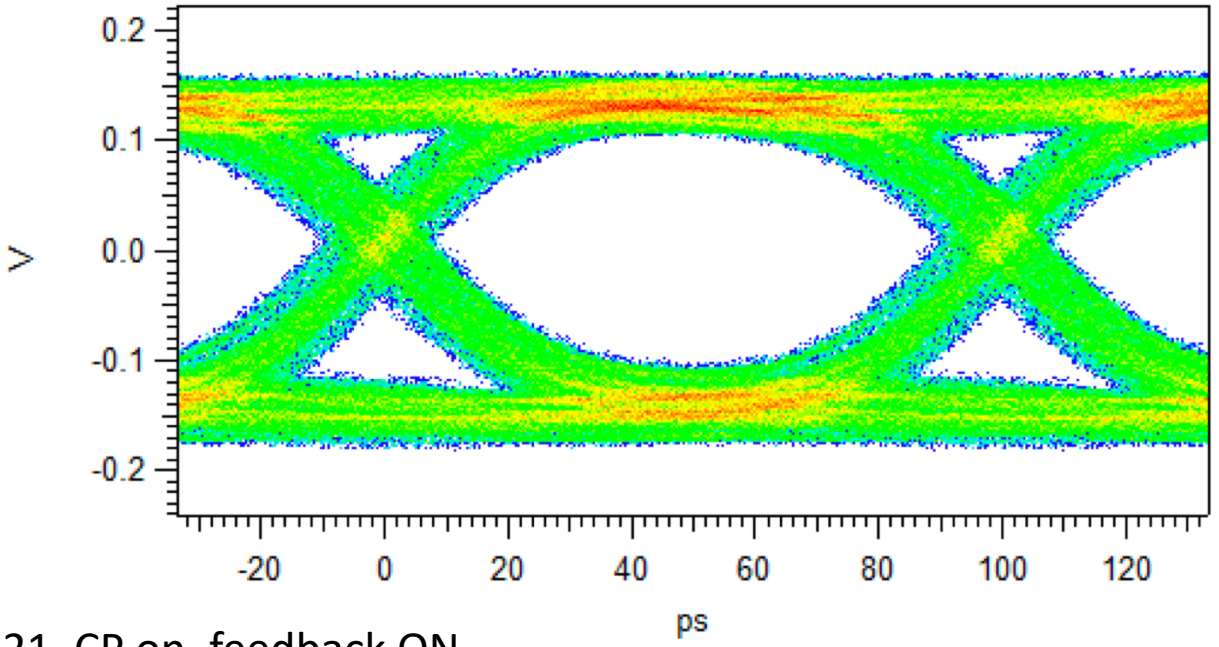
- The electrical output average current and the optical average power follow the same trend
- The electrical output modulation current correlates only the I_{mod} setting but hardly the I_{bias} setting, the OMA range at with a small I_{off} setting is less than that with a large I_{off} setting

Temperature test results

-35 °C, Vbias-tee = 2.8 V



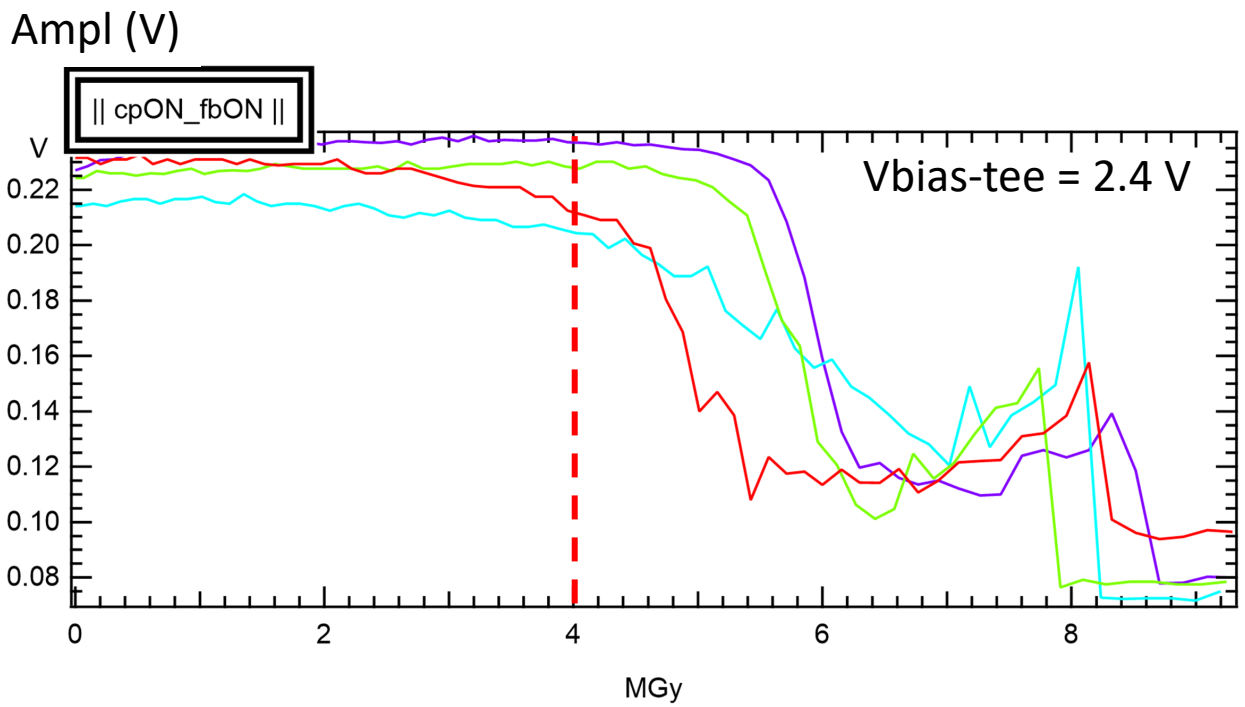
+65 °C, Vbias-tee = 1.8 V

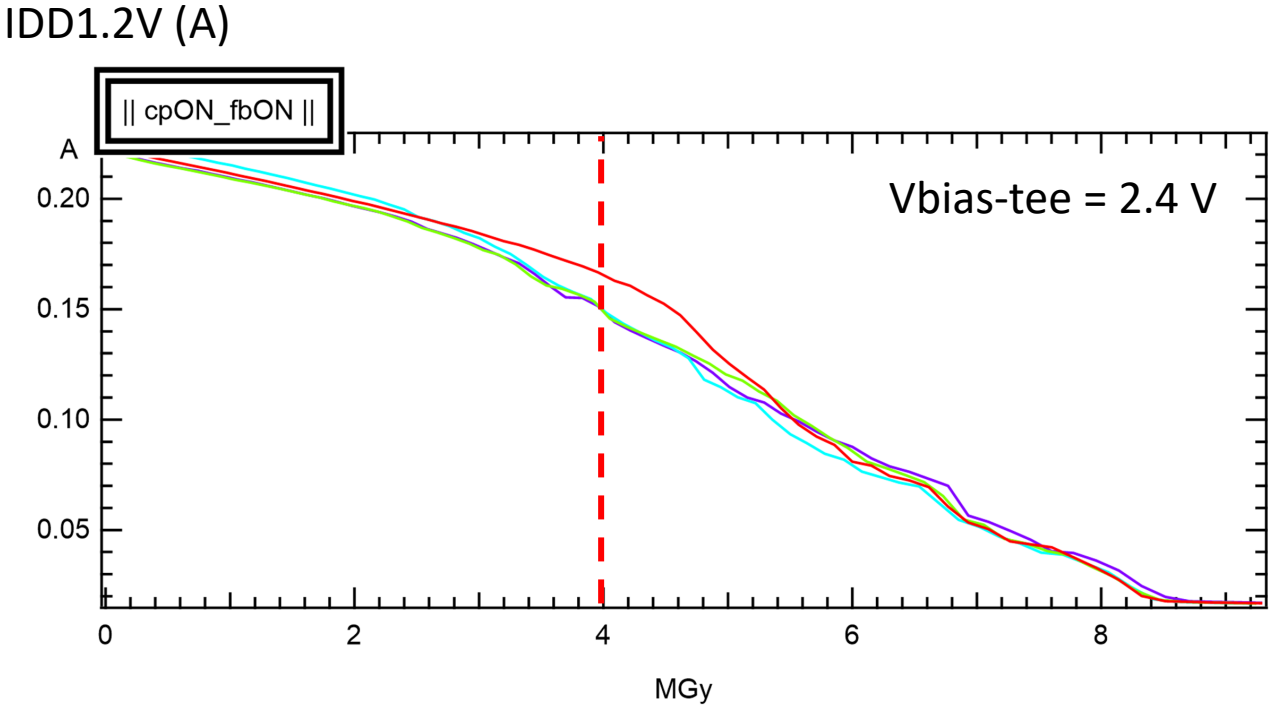


Ch4, bias = 7, mod = 21, CP on, feedback ON

- The ambient temperature of the VL+ is specified to be from -35 °C to +65 °C.
- The cpVLAD has been verified that the cpVLAD can operate in the whole temperature range.

Irradiation test results





- Irradiated in x rays while powered on
  - One electrical test board, 69 hours, total dose 9 MGy, dose rate 130 kGy/h
  - One optical test board, 90 hours, total dose 6.3 MGy, dose rate of 70 kGy/h
- cpVLAD functioned properly in 4 MGy.

Summary

- A four-channel 10-Gbps/ch VCSEL array driver ASIC, cpVLAD, with on-chip charge pumps has been designed and prototyped in a 65-nm CMOS technology.
- With 1.2 V and 2.5 V supply voltages, cpVLAD functions with an emulated VCSEL forward voltage of up to 2.8V with the power consumption of 79.5 mW/channel.
- cpVLAD has been tested for operating in the temperature range of from -35 ^{o}C to +65 ^{o}C.
- cpVLAD has been verified for up to 4 MGy.