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A 4-Channel 10-Gbps/ch CMOS VCSEL Array Driver with on-chip Charge Pumps

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We present the design and test results of a 4-channel 10-Gbps/ch Vertical-Cavity Surface-Emitting Laser (VCSEL) array driver, the cpVLAD, with on-chip charge pumps to extend the biasing headroom for the VCSEL's needs for low temperature operation and mitigation of the radiation effects. The cpVLAD was fabricated in a 65-nm CMOS technology. The test results show that the cpVLAD is capable of driving VCSELs with forward bias voltages as high as 2.8 V. The power consumption of the cpVLAD is 94 mW/ch. Further optical tests and irradiation tests will be carried out and reported at the workshop.

Summary

The cpVLAD, a 4 x 10 Gbps VCSEL array driver, has been designed to address the limited headroom available for driving VCSELs using only the 2.5 V power rail available in 65 nm CMOS technology with radiation-tolerant requirements. The VCSEL forward voltage increases with low temperature and radiation dose, reducing the voltage headroom. The cpVLAD has on-chip charge pumps, which increases the driving stage power supply without the need for additional powering schemes in HL-LHC experiments. The cpVLAD has been prototyped in a 65 nm CMOS technology using a pad-frame that makes it compatible with the current VTRx+ design, thus allowing the possibility of using it in cases that require additional margin for operating in very high radiation environments.

The cpVLAD has four independent channels. All channels share a Voltage Controlled Oscillator (VCO) and an Inter-Integrated Circuit (I2C) slave. Each channel consists of a limiting amplifier (LA), an output driver, and a charge pump. The LA has a four-stage structure with two center-tapped shared inductors. The output driver is a differential to single-ended topology. The charge pump utilizes cross-connected NMOS and PMOS transistors driven by an 800 MHz 1.2 V clock from the VCO to boost the 2.5 V power supply to a higher voltage for the output driver. The feedback circuit automatically adjusts the output voltage of the charge pump according to the forward voltage of the VCSEL diode. Each channel of the cpVLAD provides a bias current and a modulation current in the range of 0 to 6.8 mA and 0 to 13.6 mA, respectively. The chip size is 1.85 mm x 1.65 mm.

Electrical tests have been conducted. The measurement results show that the maximum DC output current exceeds 12 mA. The driver is still functional at 10 Gbps even when the forward voltage of the VCSEL diode is as high as 2.8 V. The total jitter is 26.6 ps (P-P for a bit error rate of 1E-12) with a random jitter of 1.1 ps (RMS) and a deterministic jitter of 14.8 ps (P-P). The rise time and the fall time are 31 ps and 32 ps, respectively. The power consumption is 94 mW/ch. A full set of optical and irradiating test results will be presented at the workshop.

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