A Clock and Data Recovery Circuit for the ATLAS/CMS HL-LHC Pixel Front End Chip in 65 nm CMOS Technology

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HL-LHC Upgrade & the RD53 FE Chip

- **HL-LHC phase-II upgrade** → unprecedented requirements in terms of **radiation tolerance** and **hit rate capability**

- **A new readout FE chip** for the ATLAS/CMS pixel detector is required to be developed

- **RD53 collaboration** → Joint effort between ATLAS and CMS, 24 institutions from Europe and USA

- **TSMC 65nm technology**: Logic density, TID tolerance
- **RD53A** demonstrator chip submitted at Aug. 2017 and has been successfully characterized
  - Three front-ends, two R/O architectures
- **RD53B** (pre-production chip) submission: Sep. 2019

<table>
<thead>
<tr>
<th></th>
<th>LHC</th>
<th>HL-LHC (RD53)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fluence</strong></td>
<td>$2 \times 10^{15}$ n$_{eq}$/cm$^2$</td>
<td>$2 \times 10^{16}$ n$_{eq}$/cm$^2$</td>
</tr>
<tr>
<td><strong>Hit Rate</strong></td>
<td>400 MHz/cm$^2$</td>
<td>up to 3 GHz/cm$^2$</td>
</tr>
<tr>
<td><strong>Pixel Size</strong></td>
<td>50 x 250 μm$^2$</td>
<td>50 x 50 μm$^2$</td>
</tr>
<tr>
<td><strong>Readout Rate</strong></td>
<td>320 Mb/s</td>
<td>5.12 Gb/s</td>
</tr>
<tr>
<td><strong>Ion. Dose Tolerance</strong></td>
<td>100 - 200 Mrad</td>
<td>500 Mrad</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>130 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td><strong>Transistor Count</strong></td>
<td>87 M</td>
<td>500 M - 1 G</td>
</tr>
</tbody>
</table>

The RD53A chip bonded on the SSC PCB

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Motivation & Specifications

- A CDR/PLL is essential to the operation of the pixel readout electronics (RD53)
  - **Frequency synthesis**: A low frequency reference clock (160 MHz) is multiplied
  - The **high speed clock** drives the output data link (1.28 Gb/s per lane), 4 lanes
  - All the clock signals that control the on-chip digital logic are produced by division

- Avoid using two separate command and clock lines
  - **Reduced** number of pins, cables, mass
  - Easier system-level implementation

- **Clock and Data Recovery (CDR)**
  - Phase and frequency are locked to the random command data stream (160 Mb/s)
  - The command bits are resynchronized to the divided by 8 (recovered) clock
A new version of the CDR has been designed for the RD53B readout chip.

Two main issues were discovered:
- Locking is not always successful (clock-gating PD)
- Jitter performance should be improved

RD53A CDR (P. Rymaszewski, TWEPP 2016) has been successfully integrated into RD53A and characterized.

Motivation & Specifications

Jitter Specifications
- Command input to RD53B (160 Mbps)
  - Expected jitter: \( J_{\text{rms}} \leq 5 \) ps
  - Will be increased by distortion and ISI from the low mass cable
- RD53B data output (1.28 Gbps)
  - LPGBT automatic mode: \( J_{\text{rms}} \leq 10 \) ps, \( J_{\text{pk-pk}} \leq 60 \) ps
  - LPGBT manual mode: \( J_{\text{rms}} \leq 40 \) ps, \( J_{\text{pk-pk}} \leq 200 \) ps

RD53A output example
PRBS5 CMD IN with 2ps \( J_{\text{rms}} \)

\[ 18 \text{ ps rms} \]
\[ 134 \text{ ps p-p} \]
- **Robust and reliable locking mechanism**
  - PLL startup ➔ switch to CDR operation
  - Bang-bang alexander PD + Rotational FD

- **Stable and good quality link: Low jitter**
  - Loop optimization using behavioral models with extracted block parameters

- **Tolerance to TID effects**
  - Large MOSFET devices, increased biasing currents (VCO)
  - Simulation using radiation models

- **Tolerance to SEE effects**
  - TMR divider, counter and configuration
  - Bang-Bang loop (reduced PD and CP sensitivity)
• **Startup in PLL mode** to reach the nominal frequency of 1.28 GHz
• The command input should be the **training pattern**: 01010101…
• After a predefined time set by a counter, **automatically switch to CDR mode**
• The BB alexander phase detector will lock the phase and resynchronize the input commands
RD53B CDR Blocks: PD + FD

- Standard PFD is used in PLL mode
- Alexander Bang-Bang PD in CDR mode
- 12TR LVT library to increase tolerance to TID

- Rotational FD using quadrature divided clock, “Inactive” during normal locked state
- Pull in range: ±25% of input frequency

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• **Differential ring-oscillator** with tunable gain
• Delay cell structure with positive feedback for jitter reduction
• Default gain: 1.5 GHz/V, period Jitter $J_c = 430\text{fs}$

![VCO Tuning Curves](image1)

![Jitter Power Spectrum](image2)

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• **Synchronous divider** with multiple outputs
• Only the last stage contributes to jitter: simulated $J_{ee} = 117.5$ fs
• Triplicated logic (DFF & combinational gates, voter)
• Modified 12 track LVT library to increase TID tolerance
• Area: **1mm x 0.25mm**, designed with **RD53B floorplan** in mind
• 300pF metal filter capacitor, M1 – M5, M6 grid on top for shielding
• Each block is placed in a **separate deep n-well** with common PSUB to reduce substrate noise effects
• In RD53B 2mm x 0.3mm is dedicated for CDR, extra space filled with decoupling
• A dedicated test chip (2x2 mm²) was built to characterize the RD53B CDR performance, submitted 08/18
• The environment, data path and supporting blocks are as close as possible to RD53B. It includes:
  • LVDS command receiver
  • Serializer, PRBS generator & CML GTX fast data link cable driver
  • Bandgap, biasing DAC’s
  • Triplicated SPI configuration
• RD53A CDR is also included for performance comparison
RD53B CDR Characterization

- Measurement setup based on BDAQ53 DAQ
  - BDAQ53 FPGA board with Kintex7 FPGA
  - Carrier PCB optimized for signal integrity
  - Customized firmware, software based on Basil, Python

- First measurements conducted to verify the VCO tuning range and power consumption
- Very good agreement with simulation (slight shift due to temperature)

VCO tuning curve measurement

<table>
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<tr>
<th>Sample number</th>
<th>Power [mW]</th>
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<tbody>
<tr>
<td>1</td>
<td>7.2</td>
</tr>
<tr>
<td>2</td>
<td>7.2</td>
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<tr>
<td>Simulation</td>
<td>6 (just CDR)</td>
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RD53B CDR Characterization: Startup

- **Startup reliability** was measured by power cycling and repeating the startup procedure (100 iterations)
- Different temperature, power supply conditions
- No issues observed, the RD53B CDR is capable of successfully locking down to 0.9V power supply voltage (1.2V nominal)

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<tr>
<th>Temp.</th>
<th>Sample number</th>
<th>VDD [V]</th>
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<tr>
<td></td>
<td></td>
<td>0.8</td>
</tr>
<tr>
<td>Room</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Room</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>-20 °C</td>
<td>2</td>
<td>0</td>
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</table>
RD53B CDR Characterization: Jitter

- Command Input: 160 Mb/s training pattern (0101...) (5ps $J_{rms}$)
- Output: VCO CLK/2 (640 MHz)
- 1m SMA cables

- Command Input: 160 Mbps PRBS5 (5ps $J_{rms}$)
- Output: 1.28 Gb/s PRBS15
- 1m SMA cables

\[ J_{RMS} = 5 \text{ ps} \]
\[ J_{P-P} = 40 \text{ ps} \]

\[ J_{RMS} = 6.7 \text{ ps} \]
\[ J_{P-P} = 57 \text{ ps} \]
RD53B CDR Characterization: Jitter

Jitter Power Spectrum

**Transient noise simulation**

100000 periods = 78.125\(\mu\)s

**CMD IN** = PRBS 5

\(I_{CP} = 1\mu A, R_{FL} = 400\Omega, J_{IN-RMS} = 5ps\)

**CDR53B Verilog-A model:**

\(J_{RMS} \approx 5.5\) ps, \(J_{P-P} \approx 40ps\)

**Measurement:**

\(J_{RMS} \approx 7\) ps, \(J_{P-P} \approx 54ps\)
RD53B CDR Characterization: TID

- Bonn X-ray machine
- DUT kept at -14 °C
- Chip 4 cm away from tube
- X-ray tube biased with 40 kV
- Using Al filter

**X-ray Irradiation Plan**

<table>
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<tr>
<th>Step duration [h]</th>
<th>Dose rate [Mrad/h]</th>
<th>TID after step [Mrad]</th>
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<td>15</td>
<td>0.25</td>
<td>3.76</td>
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<tr>
<td>2</td>
<td>1.9</td>
<td>7.4</td>
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<tr>
<td>127</td>
<td>4.6</td>
<td>591</td>
</tr>
<tr>
<td>10.5</td>
<td>0.8</td>
<td>600</td>
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One loop takes approx. 40 minutes, repeats infinitely (power consumption, temperatures, etc. measured several times in loop)

- VCO
  - Tuning curves
  - Nominal Vctrl
  - Open loop performance
- CP
  - CP DAC sweep
  - CP at nominal conditions
- Jitter
  - Loopback duty cycle vs. crossover
  - Jitter analysis of few cases
- CML
  - CML tap 0 DAC sweep
- Startup
  - Startup (VCO freq. + CMD recovery) at different VDD

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RD53B CDR Characterization: TID

- For each TID step, startup reliability and locking behavior was evaluated
- Different power supply voltages were applied, total number of power cycles per VDD voltage: 2220
- For higher TID rates, the minimum supply voltage that guarantees locking is increased due to the VCO tuning curve shift
- Even at 600 Mrad the RD53B CDR was able to startup with 100% success down to 1V power supply voltage

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<tr>
<th>TID [Mrad]</th>
<th>0.8</th>
<th>0.85</th>
<th>0.9</th>
<th>0.95</th>
<th>1.0</th>
<th>1.05</th>
<th>1.1</th>
<th>1.15</th>
<th>1.2</th>
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<tbody>
<tr>
<td>0 – 0.26</td>
<td>0</td>
<td>100</td>
<td>100</td>
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<td>0.26 – 193</td>
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<td>100</td>
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<td>100</td>
<td>100</td>
<td>100</td>
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<td>100</td>
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<tr>
<td>193 – 591</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>591 – 600</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

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• The VCO gets “slower” with radiation damage, higher VCTRL is required and gain is degrades by 6-10%
• Even at 600 Mrad there is adequate VCTRL headroom (720mV @ 1.28GHz)
• The radiation model used in the design process predicted an even higher shift

• The output 1.28 Gb/s PRBS15 data stream jitter ($J_{pp}$) was measured for PRBS5 command input with 5ps $J_{rms}$
• A 13% increase was observed that is mainly attributed to duty cycle distortion caused by CMOS pre-driver of the CML stage
**Summary:**

- **A CDR circuit** was designed for the RD53B ATLAS/CMS phase-II upgrade pixel readout chip.
- **A dedicated test chip** was developed for the CDR testing and **full characterization** has been performed.
- **Robust locking** mechanism, no issues observed.
- **Good jitter performance** (reduced to 1/3 of RD53A’s CDR jitter).
- **Circuit is fully functional** after irradiation to 600 Mrad.

**Outlook:**

- **SEE sensitivity tests** with heavy ions and laser pulse injection were recently performed.
- Minor design improvements are being implemented.
- The overall performance is satisfying and the **CDR is integrated in the RD53B layout**.

SEE robustness simulation of various CDR blocks carried out by Fernando Muñoz and Fernando Márquez (University of Sevilla).

Special thanks to P. Moreira, P. Leitao, S. Kulis and F. Faccio (CERN) for their valuable advice.
Thank you!
Backup
• Jitter considerations in the design of the CDR:
  • Second order (usually) loop characterized by its bandwidth (BW) and damping ratio (β)
    • For $F < F_c$, input jitter is transferred to the output (tracking)
    • For $F > F_c$, the VCO jitter will accumulate (“free running”)
  • Jitter peaking must be avoided by designing for maximum phase margin (optimal β)
  • For high input DJ slope overload must be avoided
  • The filter resistance must not contribute significant thermal noise
  • For bang-bang loops the frequency “step” must be considered

Phase Noise PSD

Input Jitter

Total jitter

Input jitter only
Closed loop

VCO jitter only
Closed loop

VCO jitter
Open Loop

Frequency (Hz)
- **Standard drain switching CP.** The input current is divided by 4 (because for CDR53B BB loop low currents are needed)
- **Unity gain buffer added** to reduce dynamic glitches when the UPB and DN switches are off (current steering)
- Simple class-A current mirror differential pair buffer, 1GHz BW, power consumption = 0.7mW
- **UP and DN pulse feedthrough cancellation** transistors added
- Programmable low pass filter
- The resistor selection range is 50Ω to 1KΩ with 50Ω steps, ONE-HOT encoding

- 75fF capacitor at VCTRL (parasitics) forms a second pole to filter high frequency noise
- Possibility to override VC (VCTRL) by an external voltage (for VCO gain measurement)
• Duty cycle distortion causes a “dead zone” inside which the loop does not correct
• Deviation from 50% duty cycle (in ps) is added directly to the pk-pk output Jitter
• Example of simulation with PRBS-5 input, 62.5ps HIGH-LOW level duration difference (equivalent to 0.5% DCD)
- Impact of duty cycle distortion (DCD)
- 62.5ps (equivalent of 0.5% duty cycle distortion)
- PRBS-5 input
- Lower loop gain (BW) by using single edge

**Jitter Power Spectrum**

- Dual edge 62.5ps DCD
- Dual edge no DCD
- Single edge 62.5ps DCD

**Dual edge no DCD:** $J_{RMS} \approx 4.3\,\text{ps}, J_{P-P} \approx 38.5\,\text{ps}$
**Dual edge 62.5ps DCD:** $J_{RMS} \approx 15.7\,\text{ps}, J_{P-P} \approx 100\,\text{ps}$
**Single edge 62.5ps DCD:** $J_{RMS} \approx 5.2\,\text{ps}, J_{P-P} \approx 46\,\text{ps}$
• Verilog-A simulation, PRBS-5 input with variable random jitter
• A significant portion of the input jitter can be filtered: Depends on the CDR BW and the input jitter spectral content
- Startup counter default CNT MAX set to 30 000
- CNT MAX can be reduced to speed up startup (e.g. 10 000)

<table>
<thead>
<tr>
<th>CNT MAX</th>
<th>Lock success rate [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDD [V]</td>
</tr>
<tr>
<td></td>
<td>0.9</td>
</tr>
<tr>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td>1 000</td>
<td>0</td>
</tr>
<tr>
<td>3 000</td>
<td>0</td>
</tr>
<tr>
<td>5 000</td>
<td>0</td>
</tr>
<tr>
<td>7 000</td>
<td>0</td>
</tr>
<tr>
<td>10 000</td>
<td>100</td>
</tr>
<tr>
<td>15 000</td>
<td>100</td>
</tr>
<tr>
<td>20 000</td>
<td>100</td>
</tr>
<tr>
<td>30 000</td>
<td>100</td>
</tr>
</tbody>
</table>
- Injected **one** frequency at a time
- For each signal amplitude was adjusted to produce **-15 dBmV** spike in chip’s VDD spectrum
- Gain degradation 6% - 10% (depending on gain setting)
- Nominal Vctrl increased
- $J_{PP}$ increased 13%
- Circuit fully functional after irradiation
Tolerance against Single Event Effects (SEE) was measured using heavy ions at the Louvain-la-neuve HIF facility for a total of 8 hours testing (4 hours of measurements). All available ion types in the “heavy penetration” cocktail were used, angled measurements with lighter ions. Each measurement had flux $\approx 6.5 \cdot 10^3 \frac{\text{particles}}{\text{s} \cdot \text{cm}^2}$ (not max. available), approx. 10 minutes long. No cooling, temperature $\approx 23^\circ\text{C}$.

### Heavy Ion Cocktail

<table>
<thead>
<tr>
<th>Ion</th>
<th>M/Q</th>
<th>Energy on device [MeV]</th>
<th>Range on device [μm]</th>
<th>LET on device [MeV/(mg/cm²)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{12}\text{C}^{4+}$</td>
<td>3.25</td>
<td>131</td>
<td>269.3</td>
<td>1.3</td>
</tr>
<tr>
<td>$^{28}\text{Ne}^{7+}$</td>
<td>3.14</td>
<td>238</td>
<td>202</td>
<td>3.3</td>
</tr>
<tr>
<td>$^{27}\text{Al}^{8+}$</td>
<td>3.37</td>
<td>250</td>
<td>131.2</td>
<td>5.7</td>
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<tr>
<td>$^{36}\text{Ar}^{11+}$</td>
<td>3.27</td>
<td>353</td>
<td>114.0</td>
<td>9.9</td>
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<tr>
<td>$^{57}\text{Cr}^{16+}$</td>
<td>3.31</td>
<td>505</td>
<td>105.5</td>
<td>16.1</td>
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<tr>
<td>$^{58}\text{Ni}^{18+}$</td>
<td>3.22</td>
<td>582</td>
<td>100.5</td>
<td>20.4</td>
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<td>$^{84}\text{Kr}^{25+}$</td>
<td>3.35</td>
<td>769</td>
<td>94.2</td>
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<tr>
<td>$^{108}\text{Rh}^{21+}$</td>
<td>3.32</td>
<td>957</td>
<td>87.3</td>
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<tr>
<td>$^{124}\text{Xe}^{35+}$</td>
<td>3.54</td>
<td>995</td>
<td>73.1</td>
<td>62.5</td>
</tr>
</tbody>
</table>

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The calculated cross section $\sigma = \frac{N_{\text{events}}}{\text{Fluence}}$ versus the LET of each ion was used to construct the Weibull curve.

Separate Weibull curves for different event classes and error capture method (oscilloscope, FPGA).

Weibull fit parameters were used by Federico Faccio to estimate event cross section in HL-LHC environment.

Error rate: $f_{\text{ERR}} = \sigma \cdot \Phi_{\text{hadrons} \geq 20 \text{ MeV}}$

$\Phi_{\text{hadrons} \geq 20 \text{ MeV}} = 4 \cdot 10^8 \frac{\text{particles}}{\text{cm}^2 \cdot \text{s}}$

![Weibull curve graph](image)

M. Huhtinen, F. Faccio, “Computational method to estimate Single Event Upset rates in an accelerator environment”
- 6m Twinax 34 AWG

- Flex L3 A X-BSF
  - ~ 1 m from shortest end
  - Note: 0.5 m expected for ATLAS

- Measurements done with CDR53B chip
  - Same CML driver design as RD53A

S-parameters extracted by TDR:
- Flex ~ -8 dB @ 640 MHz
- Twinax ~ -10.6 dB @ 640 MHz
- Twinax+Flex ~ -18.9 dB @ 640 MHz
5 ps rms jitter

2-tap PE
- tap0 = 1000
- tap1 = 400

Jitter: 218 ps (p-p), 33 ps (stddev)
- Value close to uplink measurement
- Jitter above LpGBT specification
- Vertical eye opening ≈ 120 mV
- Many non-idealities not included

Jitter: 102 ps (p-p), 16 ps (stddev)
- Large amount of DDJ filtered by the CDR
- VCO clock jitter is much less than input jitter

TIE: 419 ps (p-p)
TIE: 556.4 ps (p-p)

DCD caused by the LVDS RX

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### RD53B ATLAS Chip Development Timeline

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</tbody>
</table>

### ATLAS Chip Development Timeline

- **RD53B ATLAS chip on final stages of development**
- **ASIC design review help on 06/05/19 @ CERN**
  
  [https://indico.cern.ch/event/801498/](https://indico.cern.ch/event/801498/)

- **ATLAS final design review will take place at 13/09/19**
• **One common design framework**: called RD53B

• **One common design team**

• Two submissions of the RD53B design with different matrix sizes

• The matrix size is a parameter in the design, controlling how many identical Pixel Cores are arrayed in x and y → same netlist

• All the common and specific requirements implemented in a unique architecture → no difference in the chip bottom or in the core design

• The specific requirements will be enabled/disabled by chip configuration and/or hard-wired setting

<table>
<thead>
<tr>
<th></th>
<th>ATLAS</th>
<th>CMS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pixel array size</strong></td>
<td>20x19.2 mm² (400 x 384)</td>
<td>21.6x16.8 mm² (432 x 336)</td>
</tr>
<tr>
<td><strong>Trigger</strong></td>
<td>1 level: 1MHz, 10us</td>
<td>1 level: 750 kHz, 12 us</td>
</tr>
<tr>
<td></td>
<td>2 level: L0: 4MHz, 10us, L1: 600KHz, 25us</td>
<td></td>
</tr>
<tr>
<td><strong>Distance to the beam</strong></td>
<td>r = 4 cm</td>
<td>r = 3 cm</td>
</tr>
<tr>
<td><strong>Hit rate</strong></td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

**ATLAS/CMS main differences in requirements**