Contribution ID: **138** Type: **Oral**

A Clock and Data Recovery Circuit for the ALTAS/CMS HL-LHC Pixel Front End Chip in 65 nm CMOS Technology

Tuesday, September 3, 2019 11:30 AM (25 minutes)

A Clock-Data Recovery (CDR) circuit has been developed to be integrated in the RD53B front end chip for the HL-LHC upgrade of the ATLAS/CMS pixel detector. The 160 Mb/s input data stream is recovered and used to synthesize the 1.28 GHz clock that drives the high speed output link. Robust locking is guaranteed by starting up in PLL mode and afterwards automatically switching to CDR operation. Full characterization was performed with the aid of a dedicated test chip. Less than 60 ps p-p jitter was measured while the circuit remains fully functional after a TID of 600 Mrad.

Summary

In order to cope with the unprecedented requirements of the HL-LHC in terms of output bandwidth and radiation tolerance, a clock-data recovery (CDR) circuit has been designed in 65 nm CMOS technology and was integrated in the RD53A demonstrator chip for the phase II upgrade of the ATLAS/CMS pixel detector. This chip has been produced and successfully tested. To increase locking reliability and reduce jitter, an improved CDR has been designed for the RD53B chip. The 160 Mb/s input command stream is recovered and used to synthesize all the necessary clock signals for the RD53B chip including the 1.28 Ghz clock that drives the high speed output link.

Since the CDR is a timing-critical block, it must incorporate a robust locking mechanism and output jitter < 200 ps p-p. Furthermore it has to withstand up to 500 Mrad total ionizing dose (TID) and be tolerant to single event effects (SEE). Locking is guaranteed by starting up in PLL mode, providing a training pattern to a phase frequency detector (PFD) and afterwards automatically switching to CDR operation by a counter with appropriate preset value. The CDR loop utilizes an Alexander phase detector (PD) which is aided by a rotational frequency detector (FD). A low noise charge pump drives the low pass filter which consists of a 300pF metal-metal capacitor and programmable resistance up to $1\ k\Omega$. A unity gain buffer is used to reduce the charge sharing effect during the switching phase. The voltage controlled oscillator (VCO) consists of a three stage differential ring oscillator with gain equal to 1.5 GHz/V. It has been designed for low period jitter of $J_c = 450\,fs$ which is essential to increase input jitter tolerance. The feedback loop is completed by a fully triplicated divider with synchronous architecture. The PFD, PD and FD were designed using a customized low threshold library with increased transistor size for TID robustness. To accelerate the closed loop jitter optimization, each block was simulated separately and the extracted parameters were used to construct behavioral models. The closed loop parameters were than tuned for maximum phase margin and optimum loop bandwidth of $\approx 5\ MHz$.

A dedicated test chip was designed to characterize the CDR circuit. The necessary support blocks (bias generators, serializer, cable driver, etc.) were imported from RD53A chip library. The chip was irradiated with X-rays up to 600 Mrad while being cooled down to -14^oC. Locking was always successful down to a power supply voltage of 0.9V, with 1.2V nominal value. Less than 60 ps p-p jitter was measured while providing input data with 5 ps RMS jitter. After irradiation to a TID of 600 Mrad, the jitter increased by only 13\% caused mostly by duty cycle distortion at the output. SEE robustness was tested with a heavy ion beam and the results are currently analyzed and will also be presented.

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Session Classification: ASIC

Track Classification: ASIC