The lpGBT PLL and CDR

Architecture, Performance and SEE Robustness

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Topical Workshop on Electronics for Particle Physics

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ljCDR – clock generator inside the lpGBT

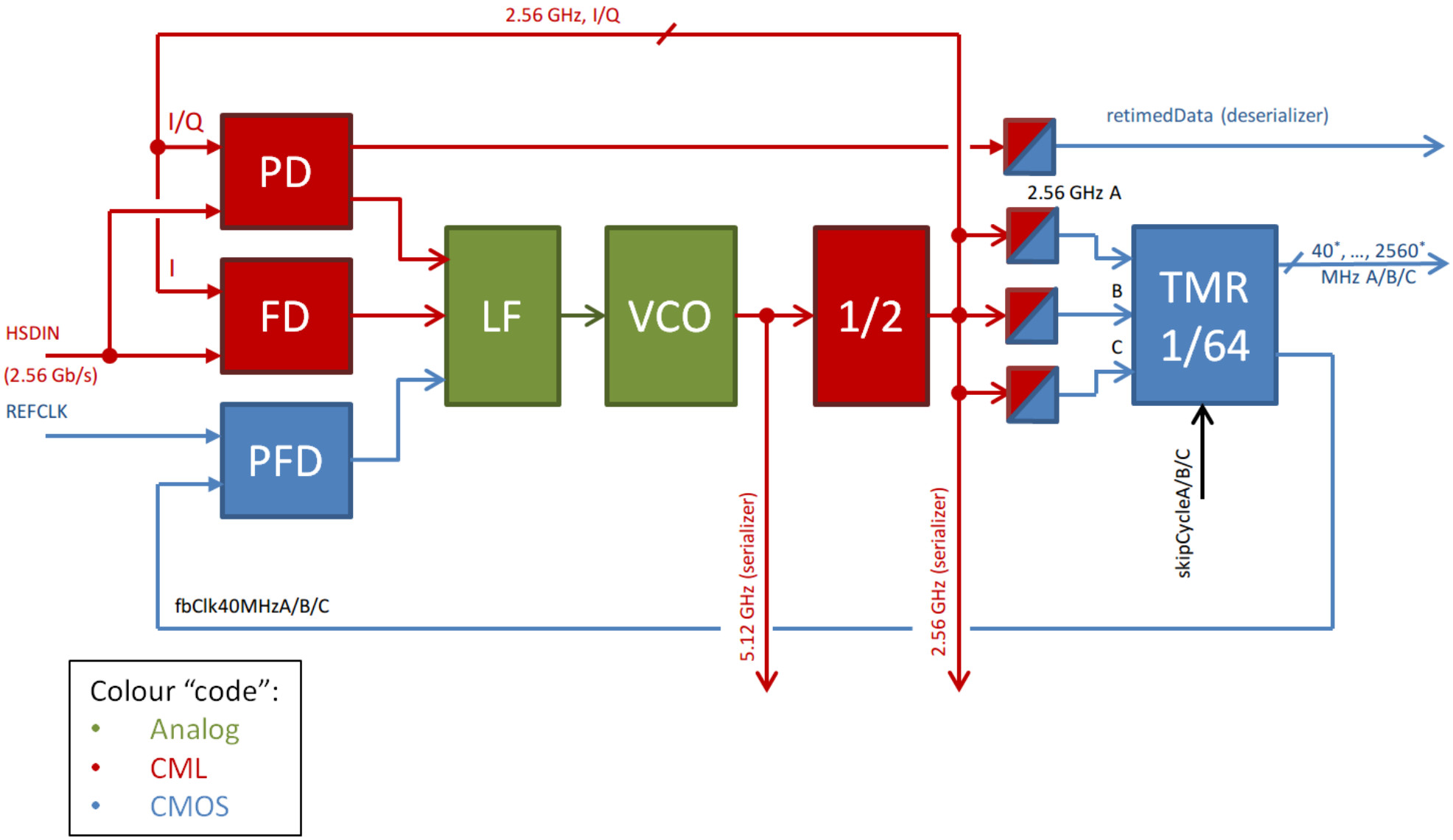
- lpGBT is a building block for radiation tolerant…
  - DAQ links (reliable data transmission)
  - Trigger + clock links (constant and deterministic latency)
  - Experiment control links (bidirectional communications)
- ljCDR as clock synthesis circuit must provide
  - 2.56 Gb/s Downlink CDR
  - 40 MHz PLL
  - 5.12 GHz clock for uplink serializer
  - Low jitter, fixed-latency clocks (40 – 1280 MHz, below 5 ps rms jitter)
- Design for radiation environments
  - Total Ionizing Dose (TID) tolerance: 200 Mrad
  - Low SEE susceptibility, SEU protection
  - … for 1.2 V ± 10 % supply voltage between -20 and 100°C

Circuit Specifications

- Two main modes of operation
  - PLL operation: 40 MHz reference clock, no downlink data
  - CDR operation: downlink data (2.56 Gb/s) provides data and timing reference
- Fixed and deterministic latency achieved by use of
  - Synchronous counter as feedback divider (phase alignment between individual frequencies)
  - Alignment of internal 40 MHz clock and uplink frame to downlink frame
- Programmable loop characteristics (charge pumps, loop filter)
- Radiation hardened by design
  - Triple Modular Redundancy (TMR) for digital circuits
  - Large transistors / ELT used in radiation-sensitive analog blocks
  - Use of PLL/CDR hardening techniques from earlier studies [1]

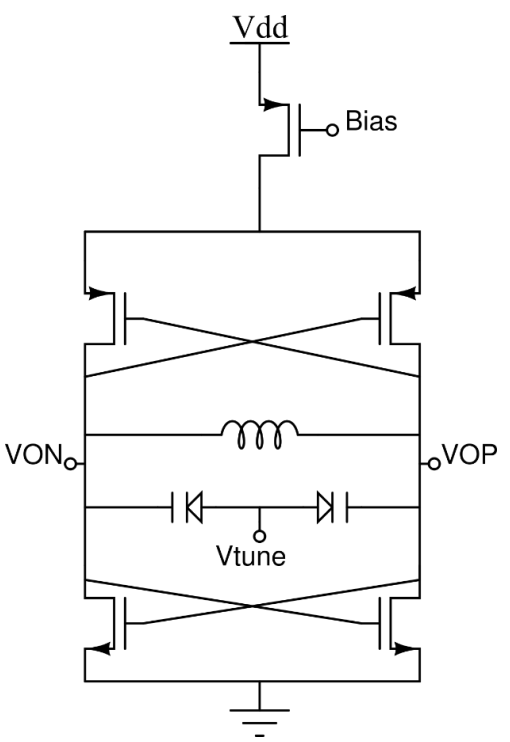
[1] J. Prinzie et. al: A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOSs

Circuit Architecture

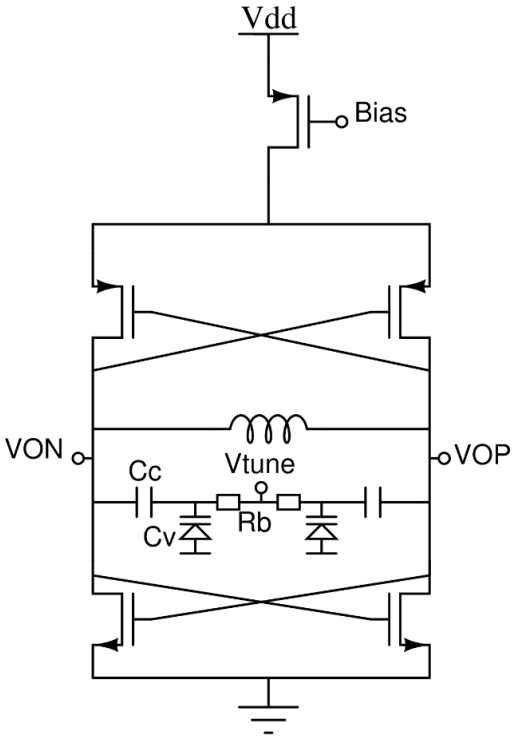


Radiation Hardened LC-VCO [1]

- Traditional LC-VCO tuning topology
  - Moscap varactors for tuning placed in separate n-well
  - Junction between n-well and p-substrate
  - Sensitive to charge collection
  - Large cross-section
- Improved tuning topology
  - Sensitive varactor n-well can be grounded
  - Prevents charge collection
  - Disadvantage: introduces low-frequency pole
  - Has to be compensated by feed-forward path



Traditional

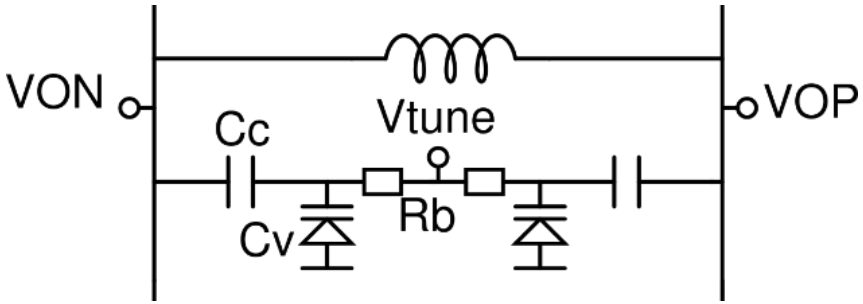


Improved

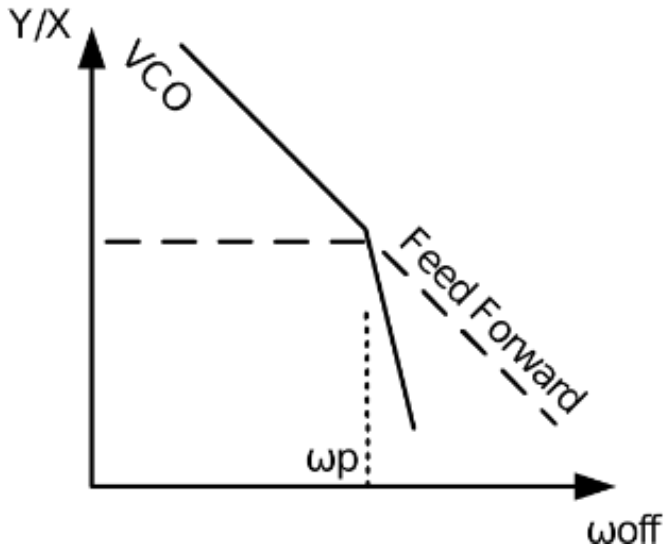
[1] J. Prinzie et. al: A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOSs

CDR High-Speed Feed-Forward Path (1/2)

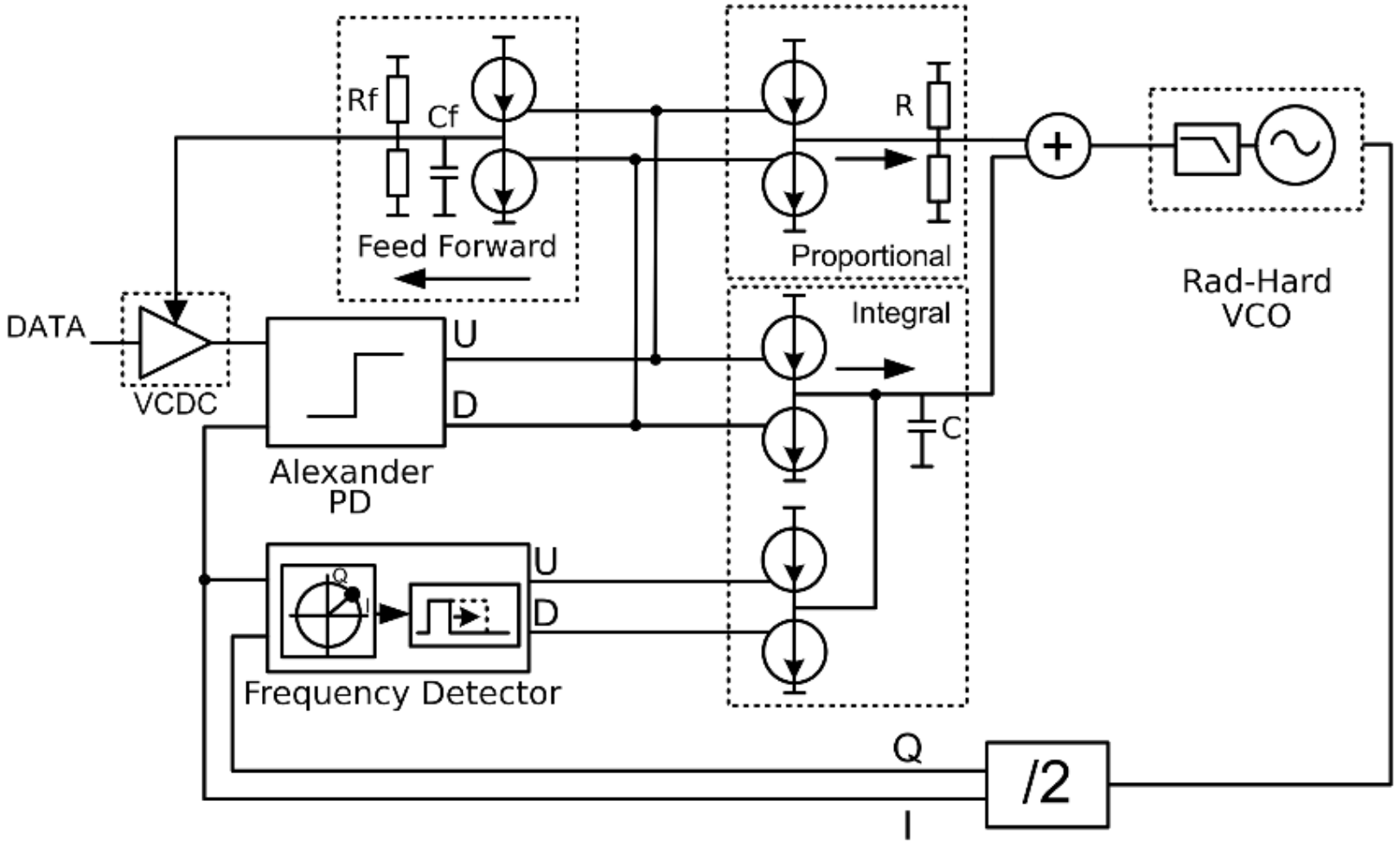
- Low-frequency pole
  - $f_{-3dB} = 1/(2\,\pi\,R_b(C_v + C_c))$
  - With design values: $f_{-3dB} = 23\ MHz$
  - Too low for high-bandwidth CDR operation!
  - Result: phase overshoot, limit cycle jitter



- High-frequency feed-forward correction
  - Lossy high-speed integrator
  - Corrections applied to phase detector input
  - Voltage-Controled Delay Cell (VCDC) at data input
  - Integrator corner frequency aligned with VCO pole

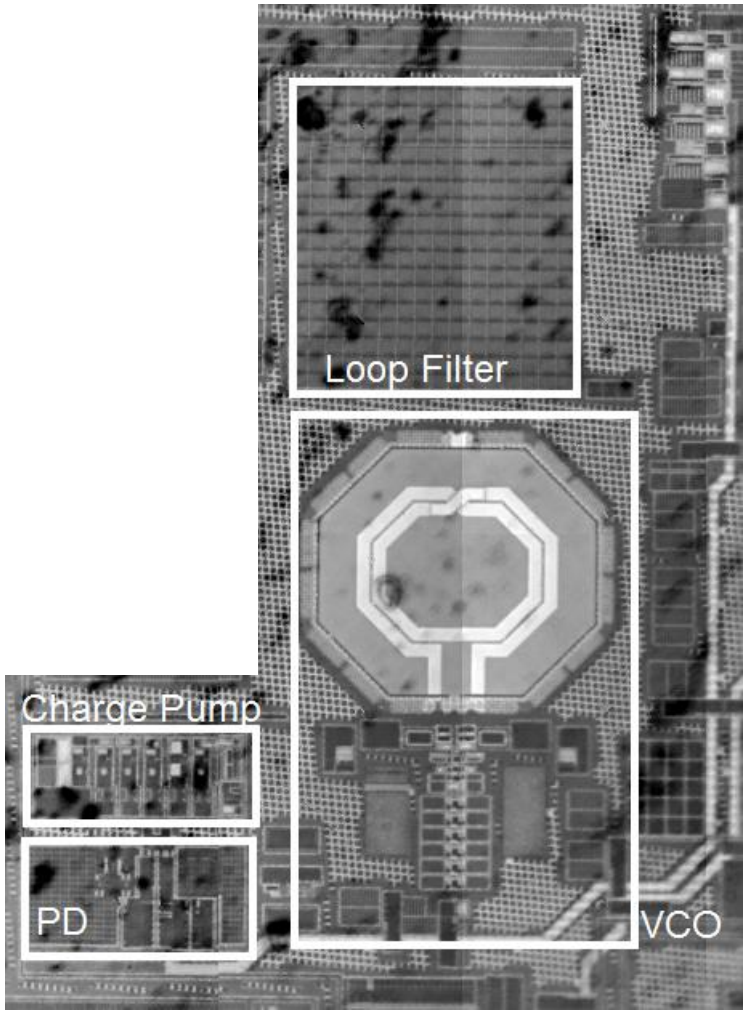


CDR High-Speed Feed-Forward Path (2/2)



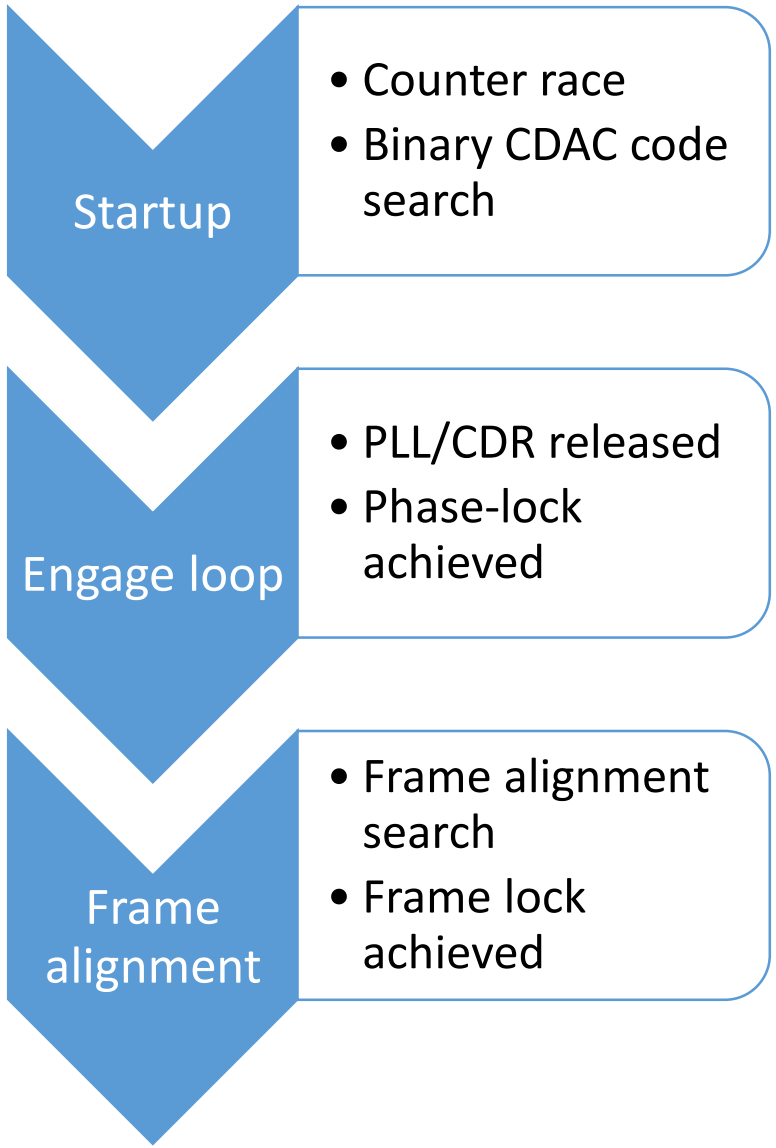
Implementation

- VCO, Loop Filter, Charge Pumps, Feed Forward
  - Full custom design of analog components
- Feedback Divider
  - First stage divide-by-two implemented in Current-Mode Logic (CML)
    - High speed allows full TMR at 5.12 GHz
  - Following Divide-by-64 implemented in CMOS
    - Custom 18-track High-Speed ELT library
    - Fully characterized for use in digital Place & Route flow
    - Fast enough to implement full TMR at 2.56 GHz
    - Skip-Cycle functionality for frame alignment
    - All divided clocks resampled using 2.56 GHz clock



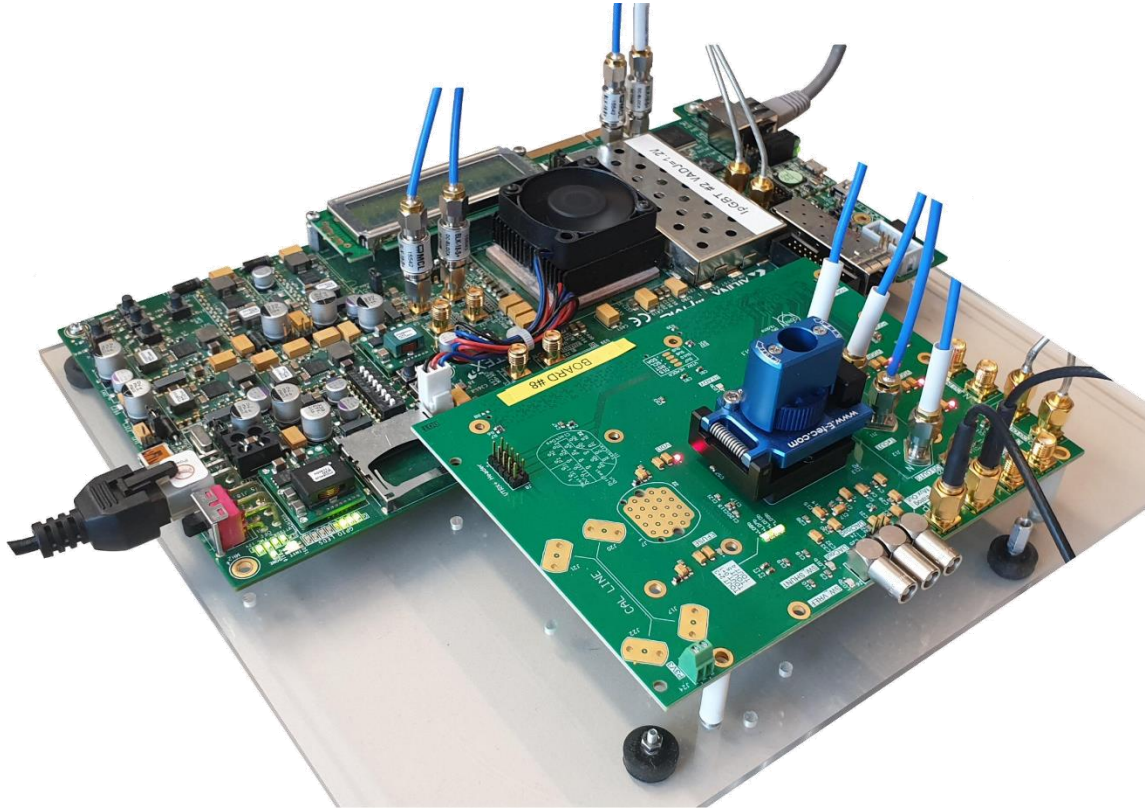
Circuit Startup

- VCO includes capacitor DAC (CDAC) to center tuning curve
- CDR/PLL initialized by Power-Up State Machine (PUSM) after ASIC configuration
- Binary search for optimal CDAC setting is performed with fixed V_{Tune}
  - PLL mode: counter race between reference clock and VCO/128
  - CDR mode: 2.56Gb/s input data divided by 16, creates (jittery) 40 MHz
- Afterwards, PLL/CDR engaged and locks
- In CDR mode, frame alignment is performed by skipping divider clock cycles @ 2.56 GHz



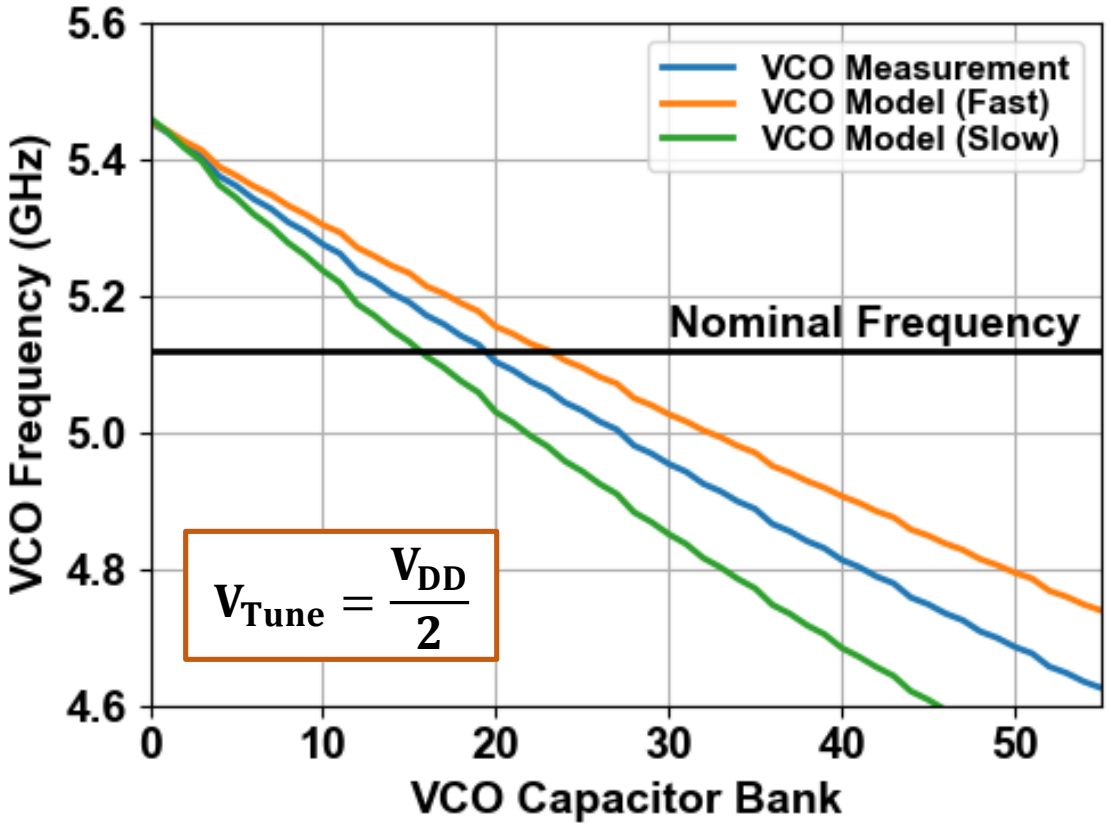
Circuit Testing

- ljCDR block prototyped as part of the first lpGBT submission
- Thorough testing to evaluate circuit performance
  - Room-temperature performance testing
    - VCO characterization
    - Loop dynamics measurements
  - Environmental testing (Thermal cycling)
  - Single-Event Effects testing
    - Heavy Ion
    - Laser Testing
  - Total Ionizing Dose (TID) testing
    - X-ray radiation



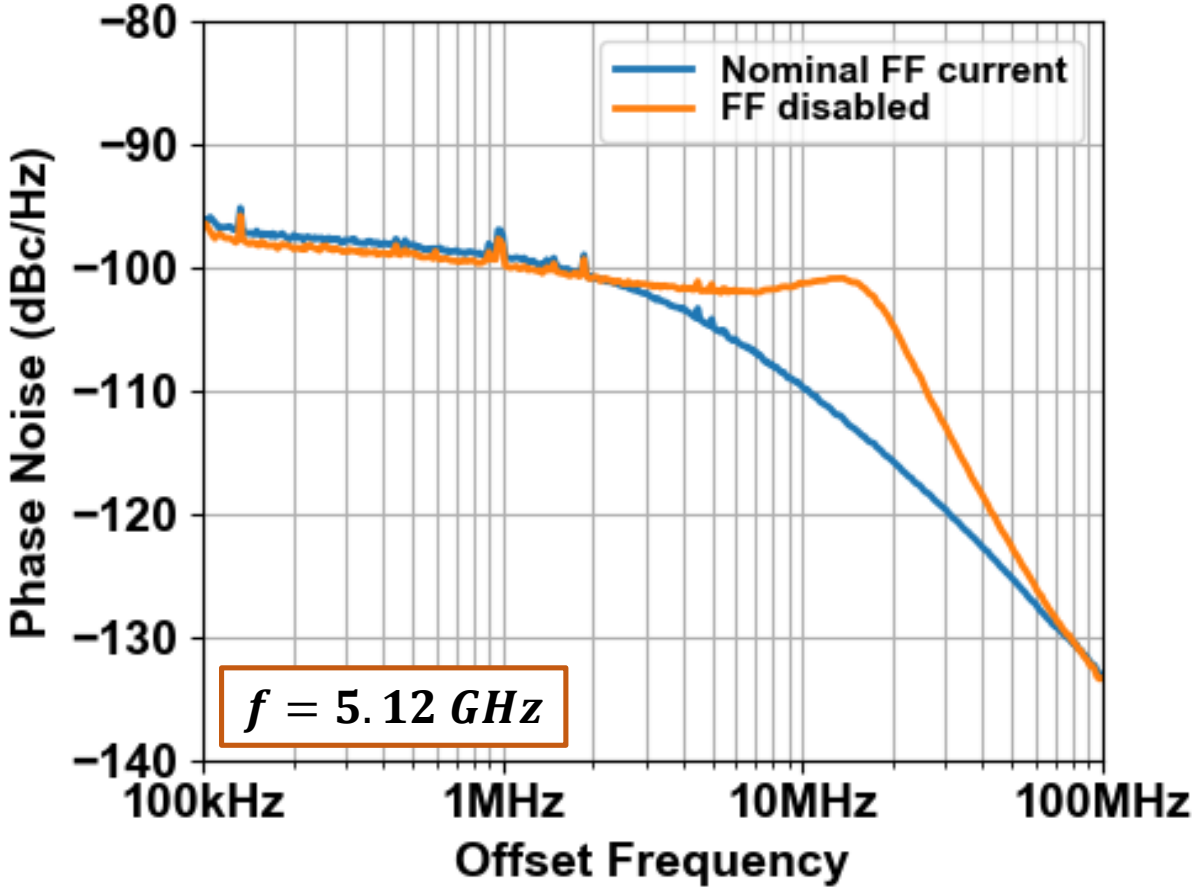
Circuit Performance (1/4)

- VCO Open Loop Frequency
  - 56 CDAC settings available
  - Design is well-centered (around CDAC=20)
  - Very good agreement with simulations
- Open loop phase noise
  - VCO jitter: 350 fs (100 kHz – 100 MHz)
  - No supply-related spurious found



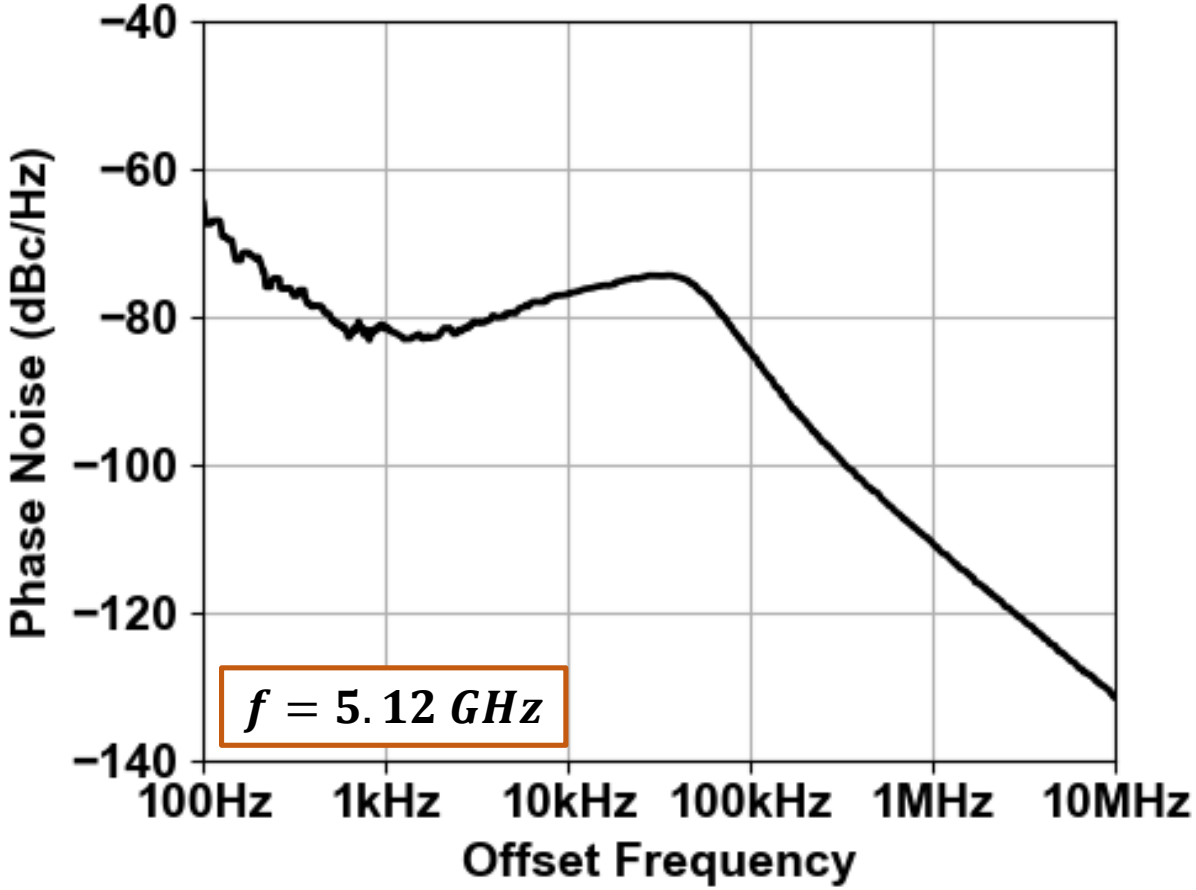
Circuit Performance (2/4)

- CDR phase noise
  - Integrated Jitter: 1.6 ps rms (100 Hz – 10 MHz)
  - 10 MHz typically interesting bandwidth of interest for front-ends
  - Feed-forward compensation scheme very effective
  - Close-in noise dominated by FPGA PLL



Circuit Performance (3/4)

- PLL phase noise
  - Integrated Jitter: 1.3 ps rms (100 Hz – 10 MHz)
  - Very low jitter reference clock (Si5344)
  - Lower jitter bounded by maximum loop bandwidth



Circuit Performance (4/4)

- Jitter performance increasingly important for detectors
- Specification: random jitter <5 ps rms

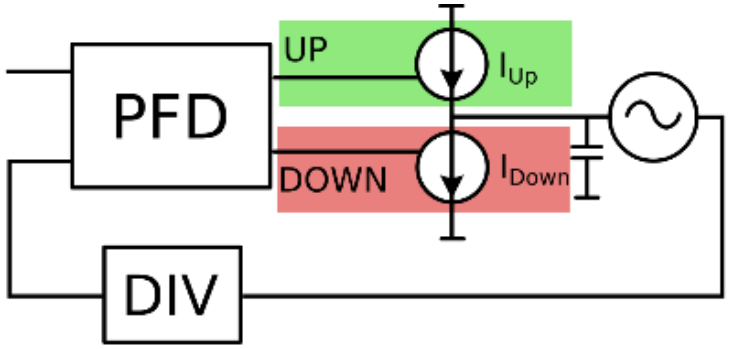
- Test results
  - PLL mode: <1 ps rms
  - CDR mode: <2 ps rms

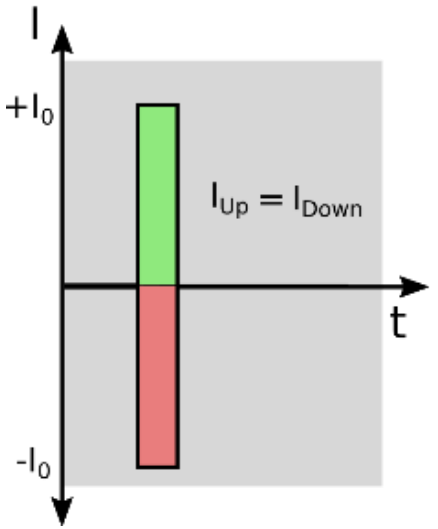
- Loop programmability
  - Charge pump currents and loop resistors can be altered as expected
  - Allows application-specific optimization

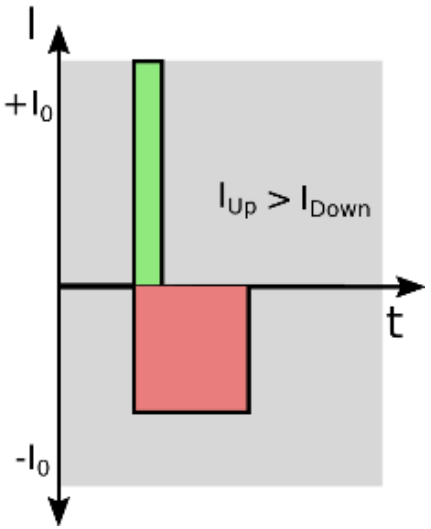
More measurements presented during HPTD meeting
https://indico.cern.ch/event/800774/

Latency issue discovered during testing

- Different CDAC codes lead to different tuning voltages
- PLL charge pumps have finite output resistance → up/down current imbalance, depending on tuning voltage
- Static phase offset to counteract current imbalance (equal Q_{up} and Q_{down}) ≈ 30 ps/code
- Selected CDAC setting may differ between power-ups
  - Could change with voltage, temperature, total dose
  - Possible impact on latency-determinism
- Improved charge pump already designed for next prototype







Single Event Effects Testing (1/3)

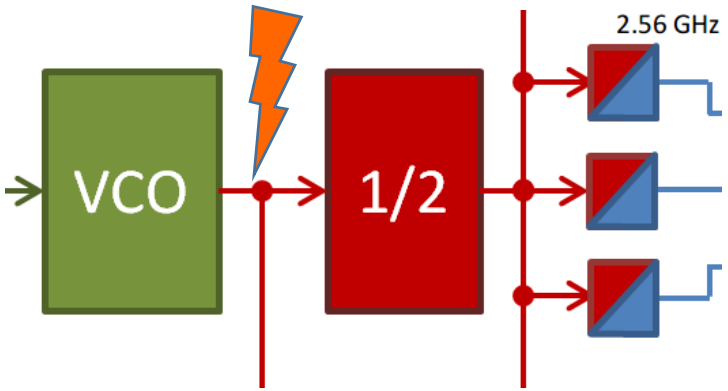
- Two complementing SEE/SEU test campaigns carried out

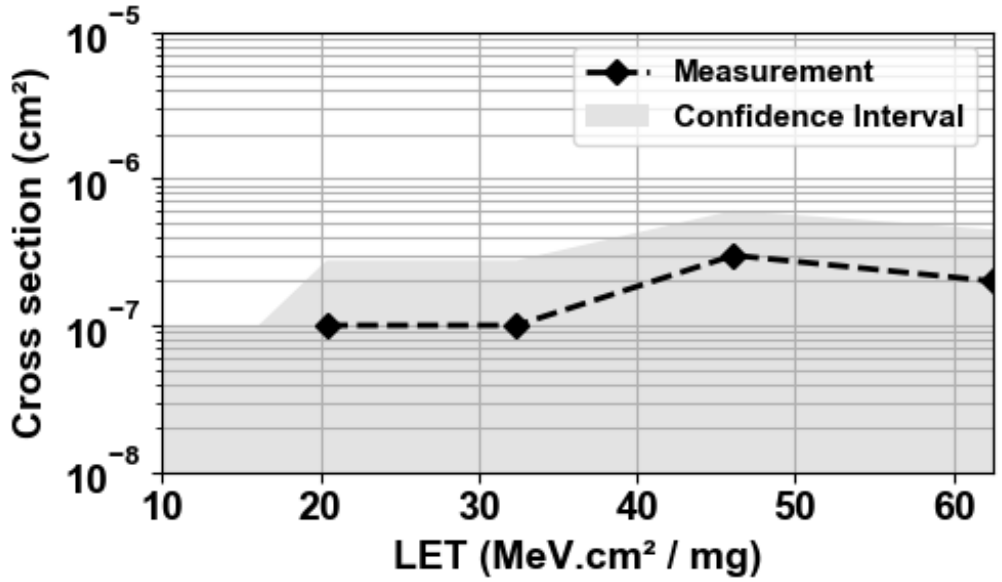
- Heavy Ion Test Campaign at UC Louvain (CRC Heavy Ion Facility)
  - Used ion LETs between 9.9 (Ar) and 62 (Xe) MeV cm^2 mg^{-1}
  - Highest possible ion flux ($15 \cdot 10^3$ s^{-1} cm^{-2})
  - Went for higher LETs first in order to capture also rare event types

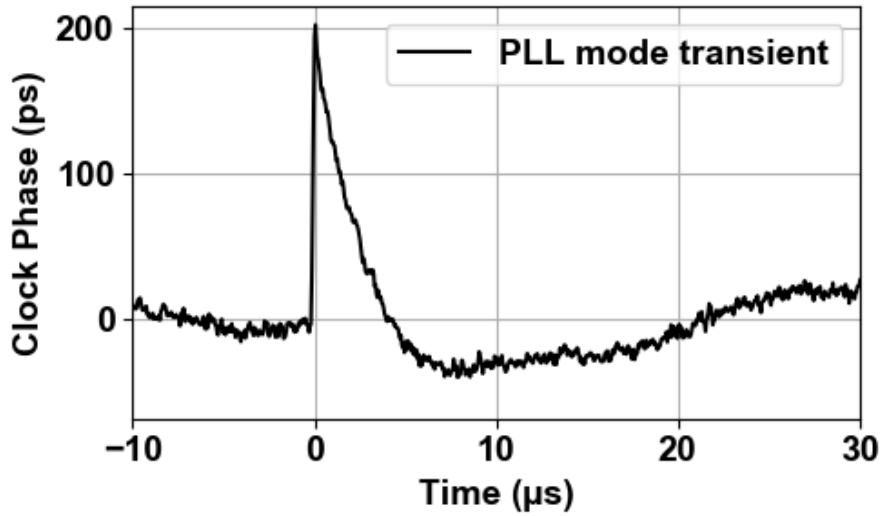
- Dual Photon Absorption Laser Test at KU Leuven (ADVISE Laboratory)
  - Systematic scan of PLL/CDR blocks to identify sensitive areas
  - Confirmation of hypotheses set up after Heavy Ion tests

Single Event Effects Testing (2/3)

- 200 ps phase jumps on output clocks (CDR & PLL)
  - Resulting in up/downlink data error bursts
  - Transient length depends on mode and bandwidth
  - 5.12 clock for CML divide-by-two not triplicated!
  - Upsets in clock distribution network suspected
  - Laser testing confirmed clock buffers to be sensitive
  - Cross section < $5 \cdot 10^{-7}$ cm^2

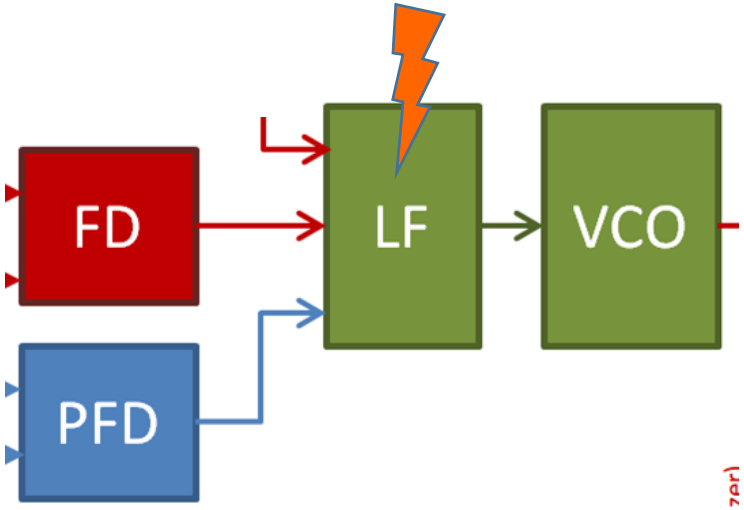


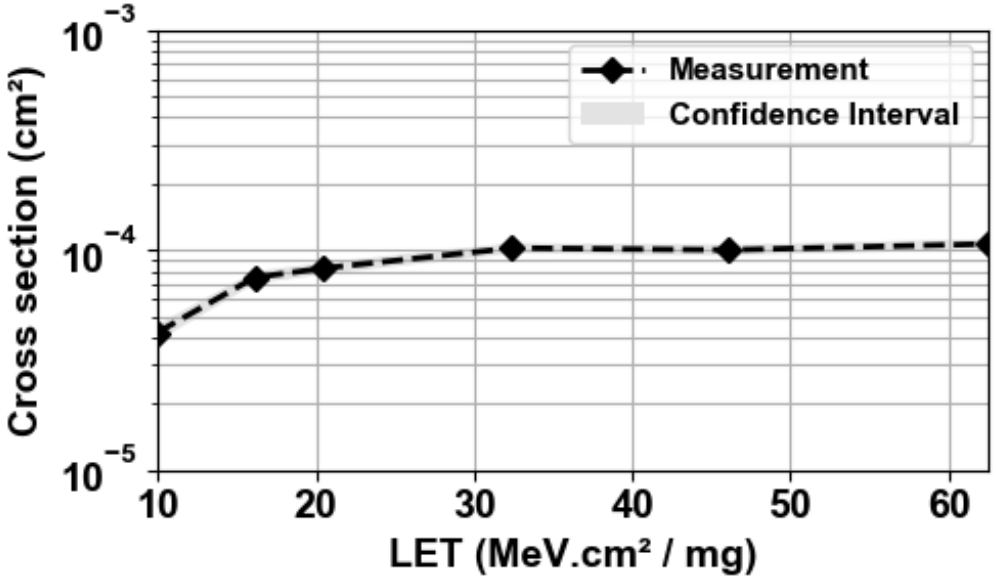


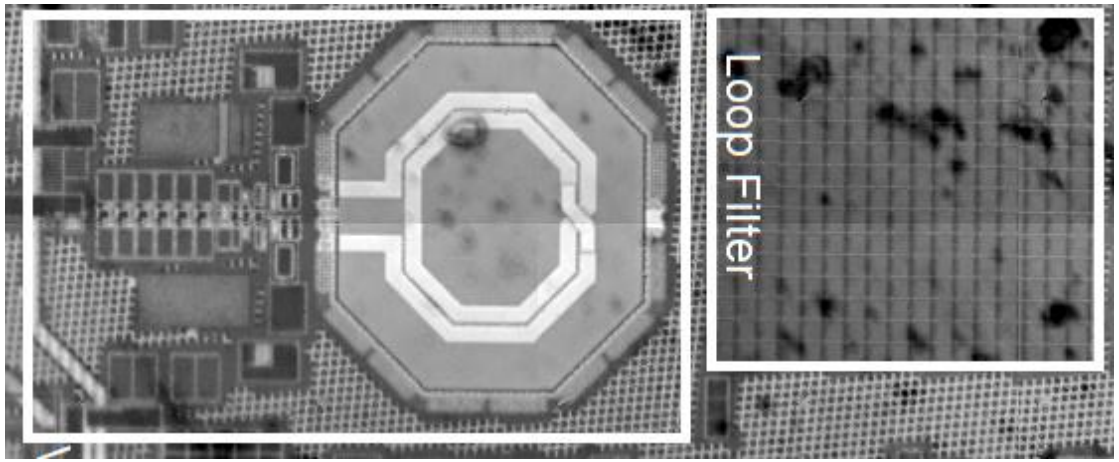


Single Event Effects Testing (3/3)

- 100 - 300 ps phase transients (PLL mode only)
  - No data errors, only clock phase affected
  - Hypothesis: Charge deposition in loop filter capacitor
  - Test structure designed to verify, to be tested soon
  - Cross section ≈ 10^{-4} cm^2
  - Capacitor area ≈ $7 \cdot 10^{-4}$ cm^2

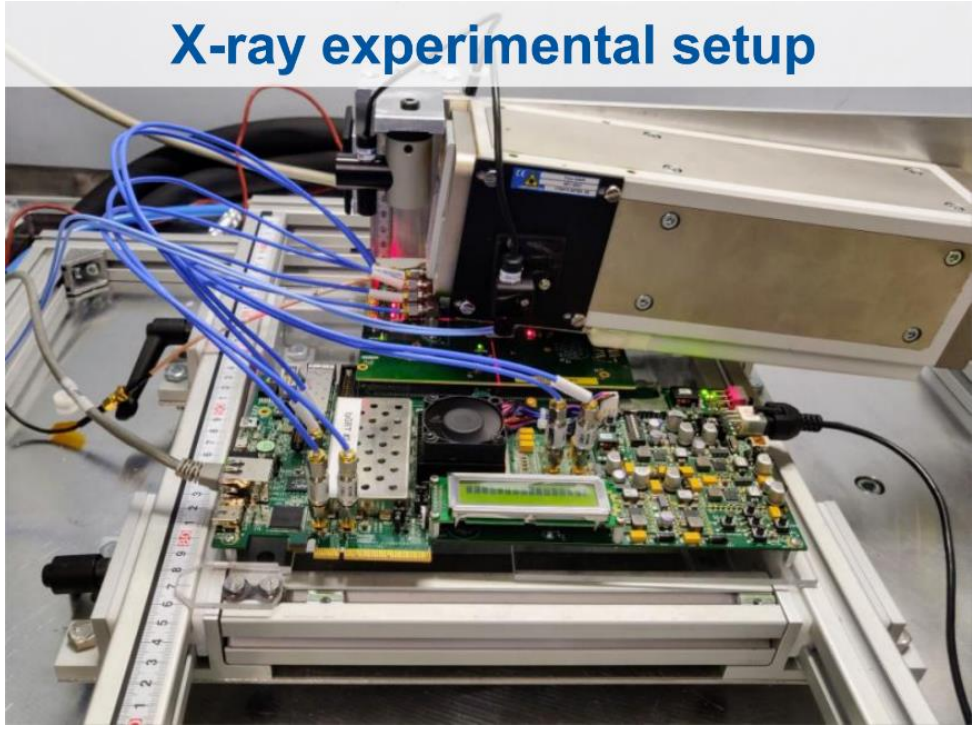






Total Ionizing Dose Testing (1/2)

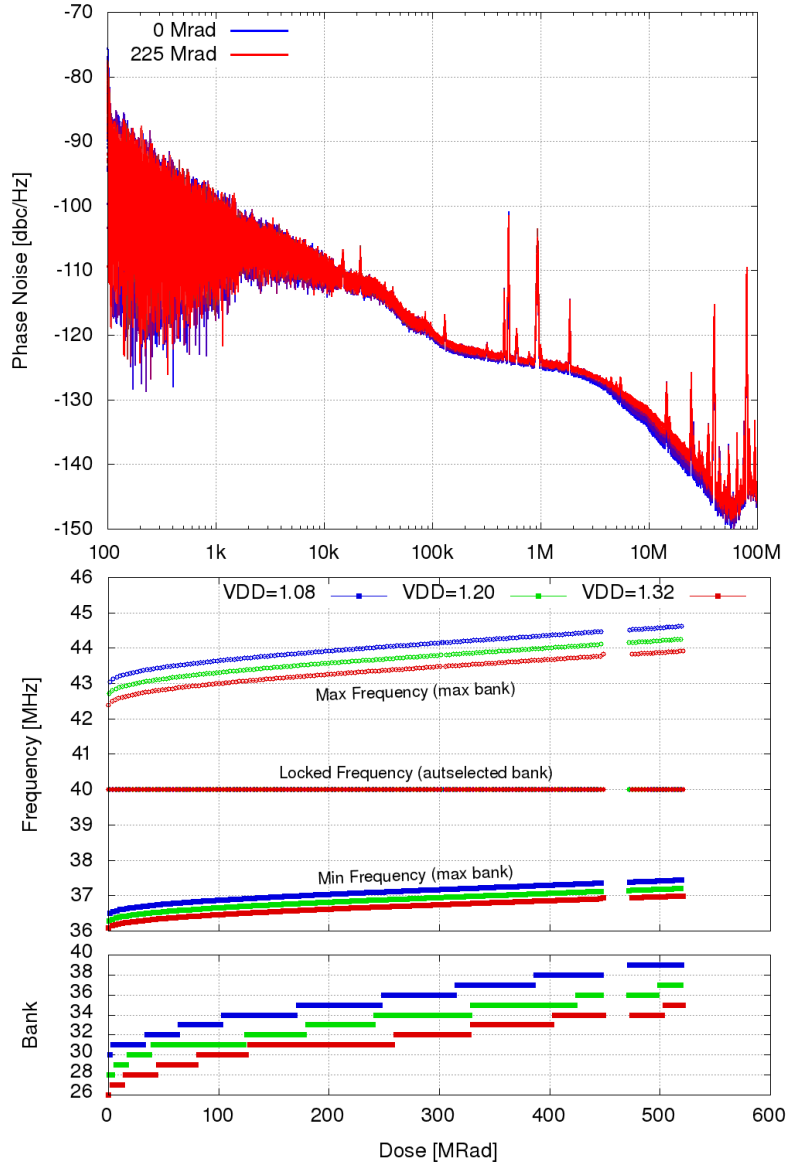
- Test campaign using CERN X-ray machine
- Effective dose rate ≈3 Mrad/h
- Total accumulated dose higher than 500 Mrad



- Automated test sequence, PLL and CDR mode
  - Supply voltages from 1.02 to 1.38 V (1.2 V ± 15 %)
  - PLL / CDR functionality
  - VCO free running minimum/maximum frequency
  - Phase noise profile
  - Integrated jitter

Total Ionizing Dose Testing (2/2)

- PLL / CDR is functional inside specified radiation dose range (200 Mrad)
  - 1.2 V – 15 %: up to 330 Mrad
  - 1.2 V – 10 %: up to 420 Mrad
  - 1.2 V and above: > 500 Mrad
- No significant change of phase noise with increasing TID
- Slight shift of VCO center frequency
  - Automatically compensated by CDAC
- Failure mechanism for high TIDs: VCO fails to start up / sustain oscillation



Summary

- High performance, low-jitter PLL and CDR circuit for the lpGBT ASIC
- Circuit performs according to specifications
  - Excellent jitter performance demonstrated (PLL <1 ps rms, CDR <2 ps rms)
  - No PLL/CDR unlocks in presence of Heavy Ions (SEE robust VCO)
  - No performance degradation due to radiation up to 200 Mrad
- Thorough testing revealed small performance shortcomings, mitigations put in place for all identified issues
- More circuit details and results in upcoming TCAS1 paper [1]

[1] S. Biereigel et al: A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOS

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Environmental Testing

- Thermal cycling performed in CERN climate chamber
- Supply voltage scan performed throughout cycles

- VCO free running frequency insensitive to temperature and supply voltage, well-centered

- No changes in operation in circuit performance or functionality observed over all voltage/temperature conditions

lpGBT Link Architecture