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The lpGBT PLL and CDR Architecture, Performance and SEE Robustness

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This paper presents the design, architecture and experimental results of the ljCDR (Low Jitter CDR) in the lpGBT (Low Power Gigabit Transceiver). The chip includes a low noise radiation-tolerant integrated LC-oscillator with a nominal frequency of 5.12 GHz to support a 10.24 Gbps uplink and a 2.56 Gbps downlink CDR. The CDR employs a novel loop architecture with a high-speed feed forward loop stabilization. The circuit was fabricated in a 65 nm CMOS technology and has been tested experimentally with heavy ions from 10.0 MeV.cm²/mg up to 62.5 MeV.cm²/mg.

Summary

Future upgrades in high-energy physics experiments such as the ATLAS, CMS, ALICE or LHCb detectors at CERN require ever-increasing data throughputs to collect tremendous amounts of data, leading to exciting discoveries in fundamental physics. In this work, the design and testing of the timing generator for the lpGBT chip are discussed. As the lpGBT will be installed close to the inner detectors, it is designed and tested for a radiation tolerance up to 200 Mrad.

In serial communication modules, the timing reference is generated by a high-speed phase-locked loop (PLL) for uplinks. For downlinks, a Clock and Data Recovery circuit recovers the high-speed clock from the data stream. The ljCDR, which is included in the lpGBT, supports both operation modes with an integrated oscillator at 5.12 GHz. For data transmission, double data rate is used to generate 10.24 Gbps data. The CDR has a dedicated frequency detector to enhance the pull-in range of the CDR loop and features gear-shifting to enhance the lock-time. The VCO was hardened by-design by using a varactor tuning topology at the cost of a reduced frequency modulation bandwidth, which can potentially destabilize the loop, especially in CDR mode. However, this was overcome by including a dedicated feed-forward cancellation that stabilizes the CDR loop and reduces the limit cycle jitter of the PLL. TID tolerance of the design was ensured by using enclosed layout devices (ELT) and/or large devices in analogue blocks. High-speed digital blocks were implemented with CML logic. Triple Modular Redundancy was employed in all digital circuits where state machines are present such as the feedback divider or the phase-frequency detector to protect against SEUs.

The lpGBT test system was used to characterize the prototypes. The LC-oscillator phase noise performance is -110 dBc/Hz at 1 MHz offset. With a low-noise reference clock, the ljCDR provides RMS jitter performance of better than 1 ps in PLL mode and 2 ps in CDR mode. During operation, the circuit power consumption is 50 mW (PLL mode) and 70 mW (CDR mode), respectively.

During a test campaign at the Heavy Ion Facility in Louvain (Belgium), the circuit was characterized for sensitivity to single event effects at different LETs. To understand the root cause of the observed effects a further test campaign using Two-Photon-Absorption laser scanning was completed. Detailed results will be presented at the conference.

Primary authors: BIEREIGEL, Stefan (BTU - Branderburg University of Technology (DE)); DE OLIVEIRA FRANCISCO, Rui (CERN); KULIS, Szymon (CERN); VICENTE LEITAO, Pedro (CERN); LEROUX, Paul (KU Leuven (BE)); RODRIGUES SIMOES MOREIRA, Paulo (CERN); PRINZIE, Jeffrey (KU Leuven)

Presenter: BIEREIGEL, Stefan (BTU - Branderburg University of Technology (DE))

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