CLICTD: A monolithic HR-CMOS sensor chip for the CLIC silicon tracker

I. Kremastiotis [a,b], R. Ballabriga [a], N. Egidos [a,c]

on behalf of the CLIC detector and physics (CLICdp) collaboration

TWEPP 2019 Topical Workshop on Electronics for Particle Physics
Santiago de Compostela, Spain, 02-06 September 2019

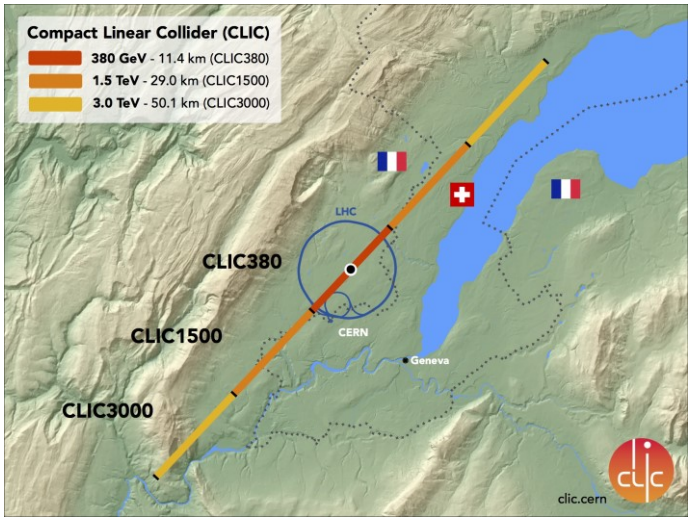
[a] CERN, Geneva, Switzerland
[b] Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany
[c] University of Barcelona, Barcelona, Spain

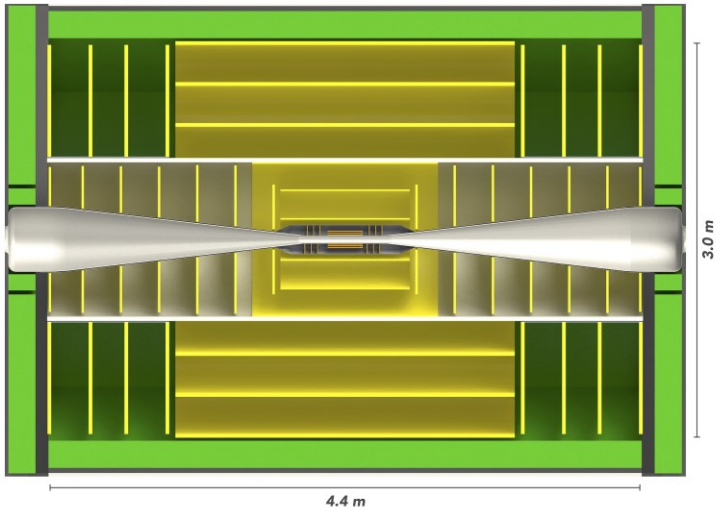
Overview

- Requirements for the CLIC silicon tracker
- The selected process
- The CLIC Tracker Detector (CLICTD) chip
- Measurement setup
- Measurement results
- Summary and outlook

Requirements for the CLIC silicon tracker

- Single point resolution in one dimension ≤7 µm (transverse plane)
- Energy measurement with 5-bit resolution
  - Time over Threshold - ToT
- Time measurement with 10 ns bins and 8-bit resolution
  - Time of arrival - ToA
- No multi-hit capability
- Material budget 1-1.5% X_0 (i.e. ~200 µm for silicon detector and readout)
- Power consumption < 150 mW/cm^2 (Power pulsing, duty cycle 156 ns / 20 ms)



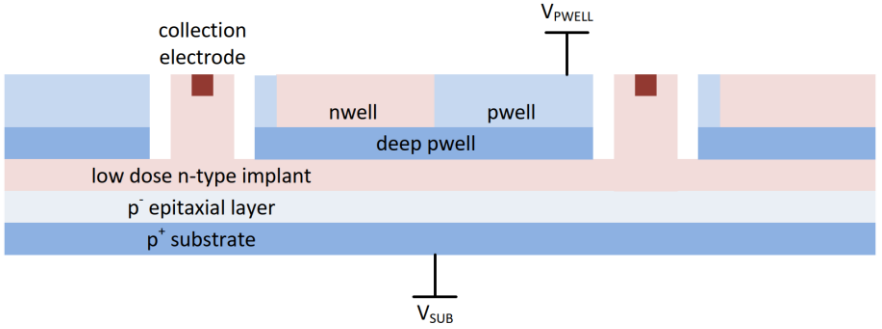


Requirements available at CLICdp-Note-2017-002 (D. Dannheim, A. Nurnberg): https://cds.cern.ch/record/2261066

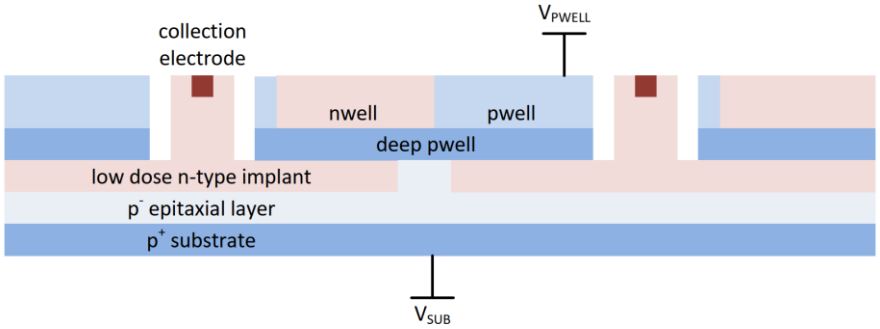
The process

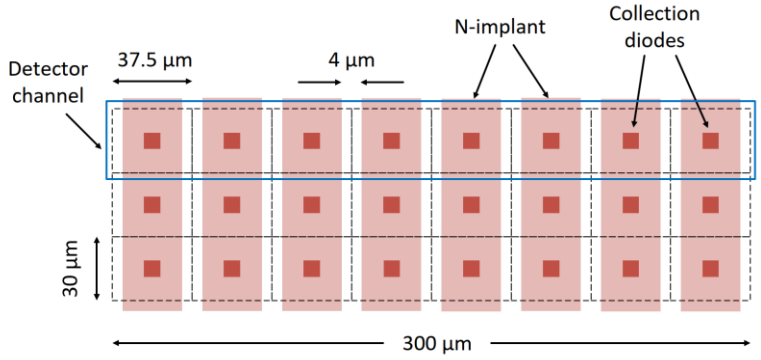
- The CLICTD chip was designed in a 180 nm CMOS imaging process
  - The signal is collected with a small N-well on the P-type high resistivity epitaxial layer (30 µm thick) (small detector capacitance → minimise analog power consumption)
  - Deep P-well shielding the on-channel electronics from the collection electrode
  - The sensor volume is fully depleted by including an additional deep N-type implant
  - Using a process split, additional wafers are produced with a segmented deep N-type implant

- 1st process split: continuous N-layer



- 2nd process split: gap in N-layer (only in the long dimension)
  - To increase the lateral field and thereby to reduce the charge collection time

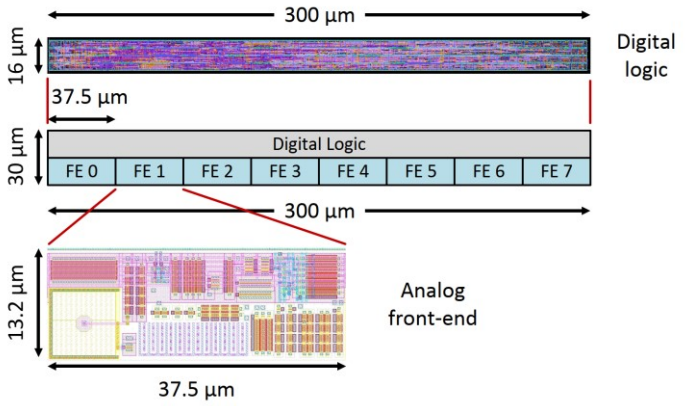


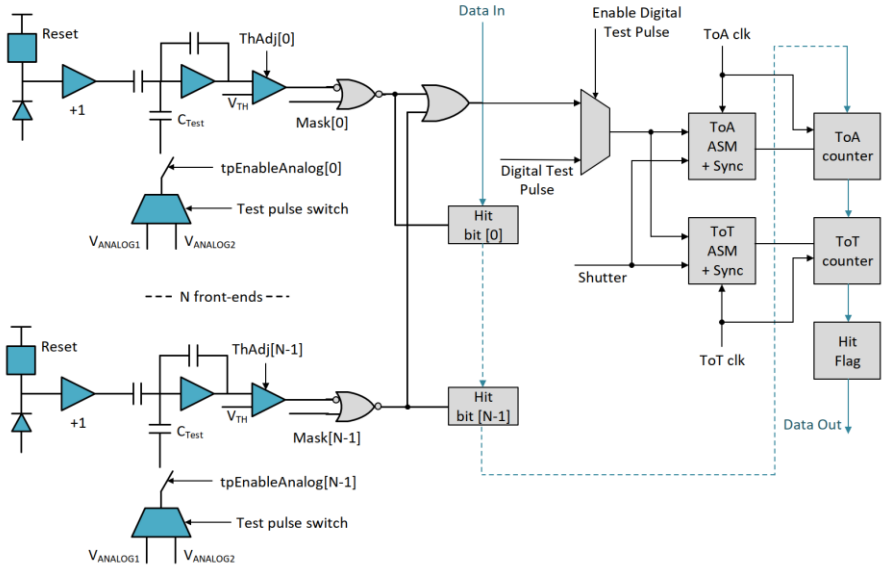


M. Munker et al. JINST 14 C05013, 2019

The CLICTD channel

- The CLICTD pixel:
  - Pixel area: $300 \times 30\ \mu m^2$
  - In each pixel, the analog part is segmented in 8 front-ends:
    - To ensure prompt charge collection in the diodes
    - Each front-end includes a collection diode, amplifier, discriminator and a 3-bit tuning DAC
  - The discriminator outputs are combined in the digital logic by means of an OR gate:
    - Binary hit information for each individual front-end (hit map)
    - Different measurement options:
      - 8-bit ToA (10 ns bins), 5-bit ToT (programmable ToT range: 600 ns – 4.8 µs)
      - 13-bit long ToA counter
      - 13-bit photon counting
  - Readout data: zero compression algorithm:
    - 22 bits read out for channels that have been hit (hit-flag + 8 bits ToA + 5 bits ToT + 8 bits hit map)
    - 1 bit read out for channels that are not hit
  - Front-ends can be masked or test pulsed individually





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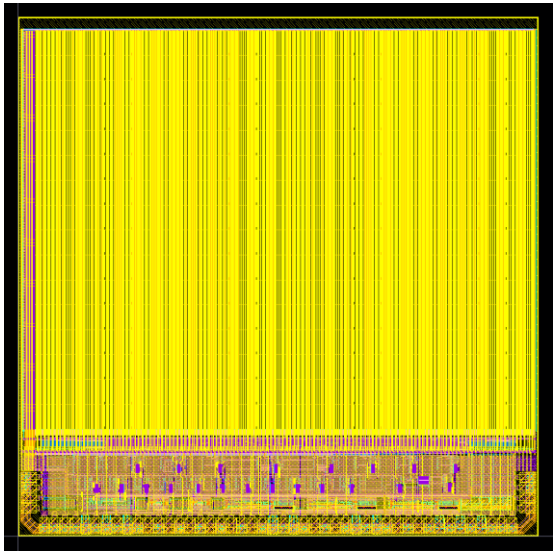
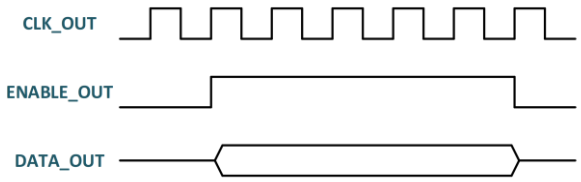
The CLICTD chip

- The CLICTD chip:
  - Chip area: 5×5 mm^2
  - Sensitive area (pixel matrix): 4.8×3.84 mm^2
  - Number of pixels: 16×128
  - Power pulsing:
    - Analog front-end is set to a standby power mode between subsequent bunch trains
    - Clock is gated when the digital logic is not active
  - Verified using UVM
    (Universal Verification Methodology)

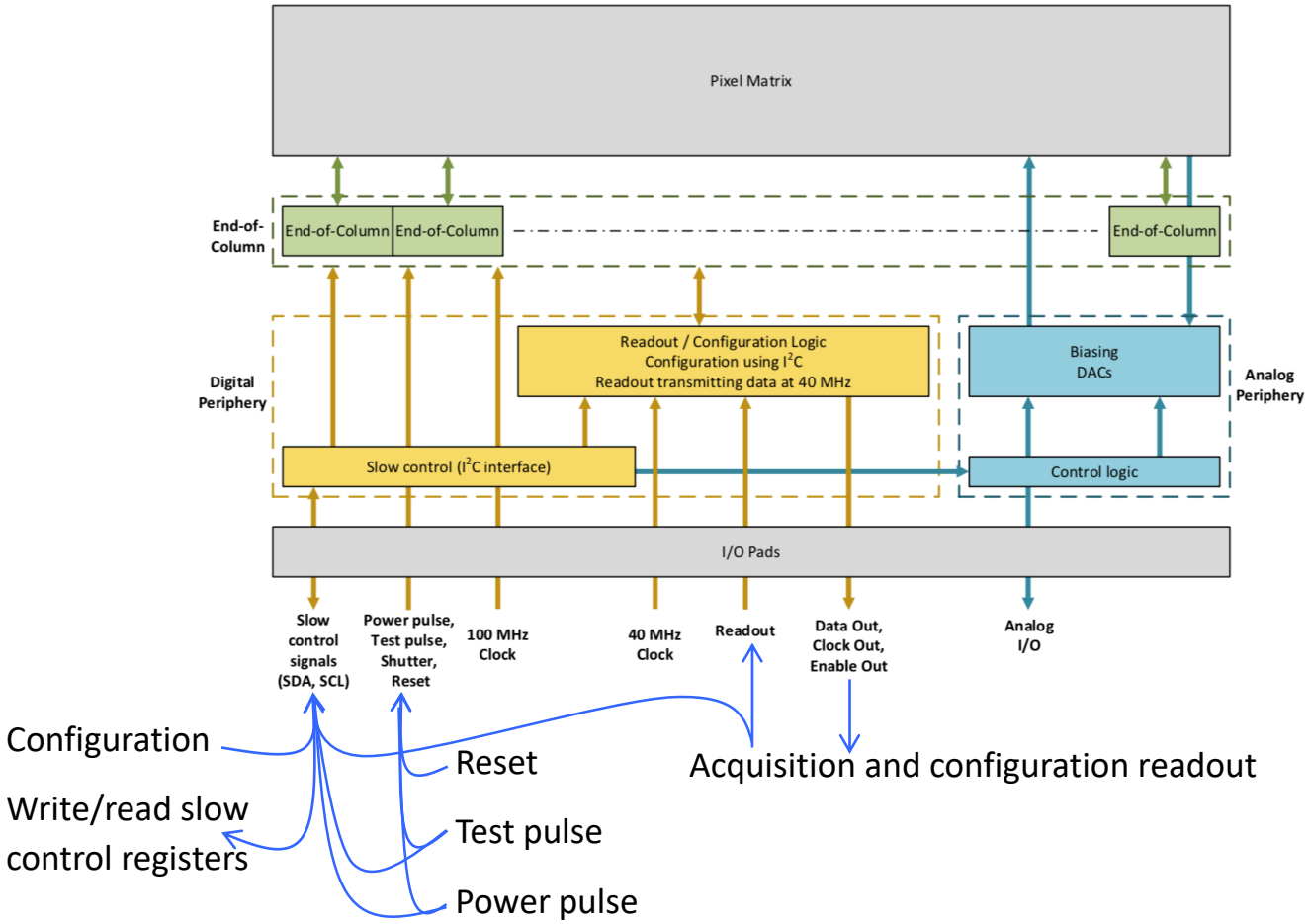


- The CLICTD periphery and interface:
  - Analog periphery:
    - 20 DACs for biasing the analog part
    - Internal bandgap reference
  - Digital periphery:
    - I^{2}C interface for the slow control
      - Reading / writing internal registers
      - Matrix configuration
    - Serial readout at 40 MHz
      - Readout time ~ 70 µs
        (CLICTD matrix size, using compression, 1% occupancy)



CLICTD verification (I)

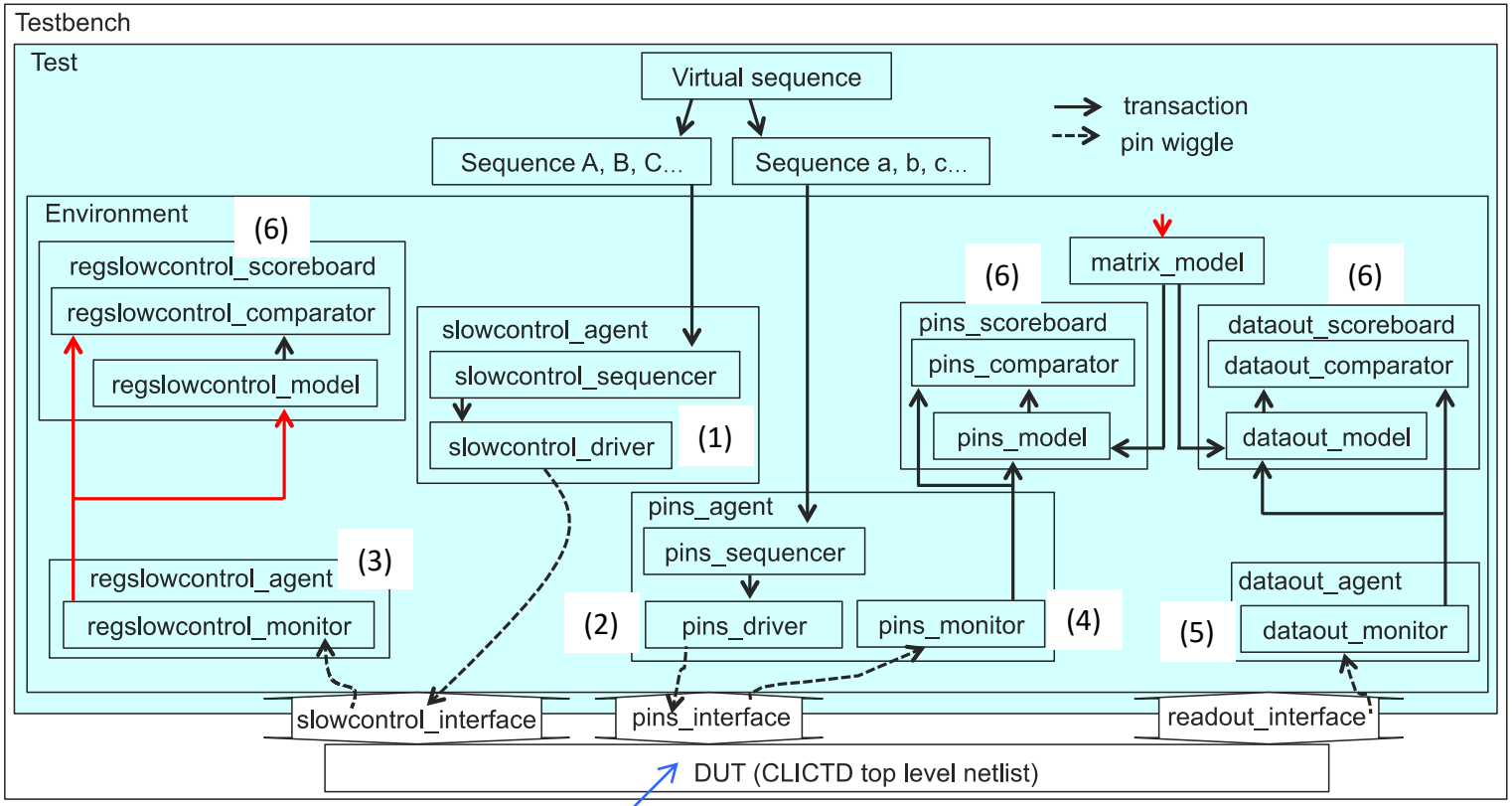
- Implemented using UVM (Universal Verification Methodology):
  - Randomized stimuli to maximize the number of operation scenarios simulated
- Simulated scenarios include the chip main operations:



CLICTD verification (II)

The framework has been run on the intermediate and final versions of the RTL and post-layout netlist. Logic and implementation bugs (e.g. timing errors when switching between acquisition and readout clocks) were detected during verification and successfully fixed.

UVM framework to verify the CLICTD



Device Under Test: in the last iteration, CLICTD post-layout top level netlist

(1) Send commands via the slow control

(2) Send commands by activating pins

(3) Read slow control registers

(4) Read pin values

(5) Read serial readout pin values

(6) Report whether the chip response matches the expected values

Measurement setup

- CLICTD chips received: July 2019

- First samples wire-bonded on PCB received shortly after
  - 2 samples from “Rev. A” – continuous N-implant
  - 1 sample from “Rev. B” – gap in N-implant

- Communication established using CaRIBOu DAQ (see poster from T. Vanat)
  - Modular DAQ setup
  - Uses SoC architecture
  - Based on a ZC-706 evaluation kit
    - ARM microprocessor + Kintex-7 FPGA
  - DAQ system provides:
    - Power supplies
    - Clocks
    - Communication interfaces
    - Analog I/O
    - Differential and single-ended digital signals

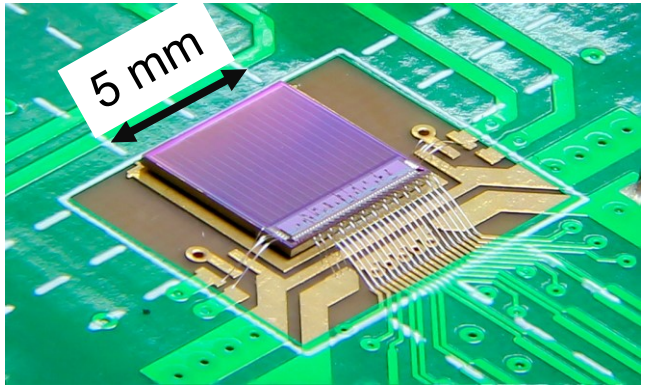


Photo of the CLICTD chip

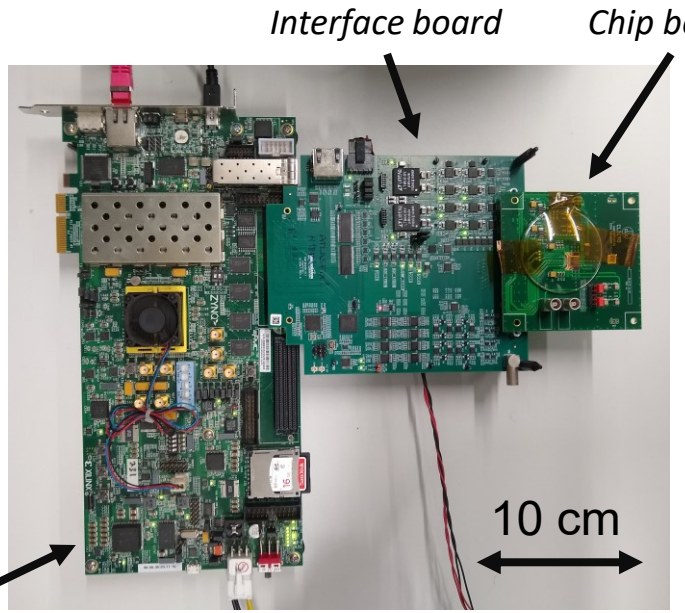
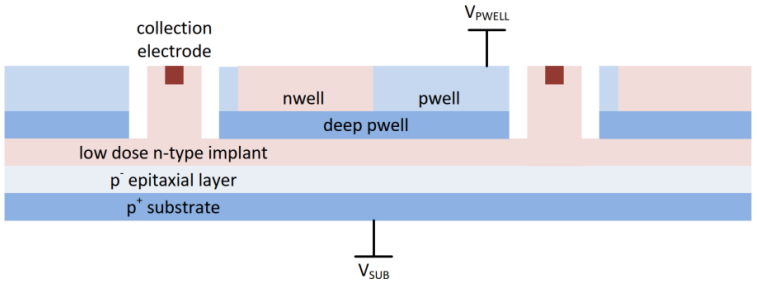


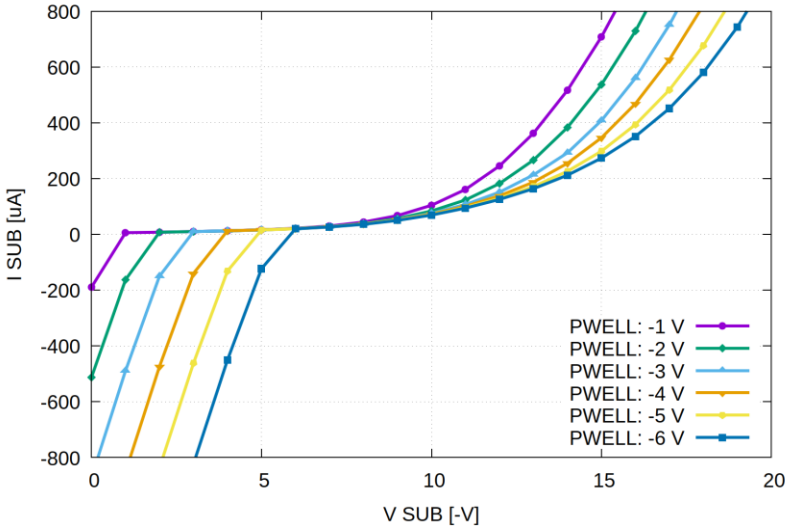
Photo of the CaRIBOu setup

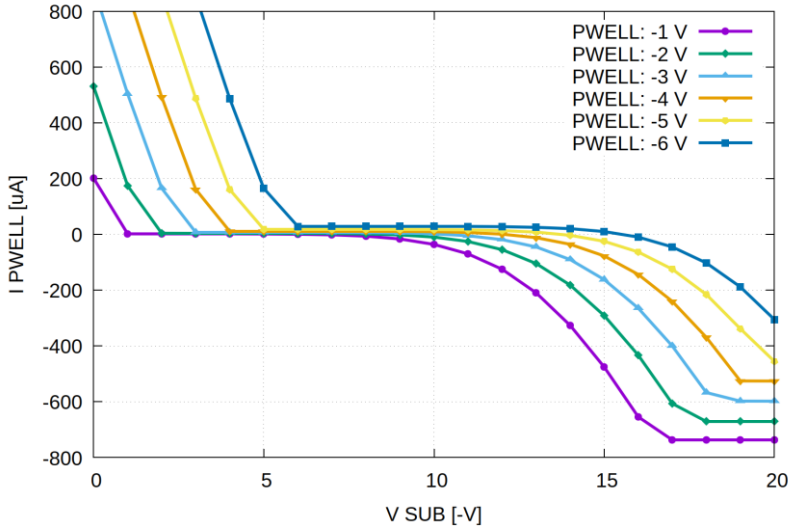
gitlab.cern.ch/Caribou

I-V characteristics

- Sensor I-V measured by scanning the substrate bias, for different values of the deep P-well bias
- Leakage current was measured at both nodes: SUB and PWELL (using two external power supplies)
- 1st process split: continuous N-layer
- Sensor can be operated in the “plateau” region where the leakage current stays < 20 µA

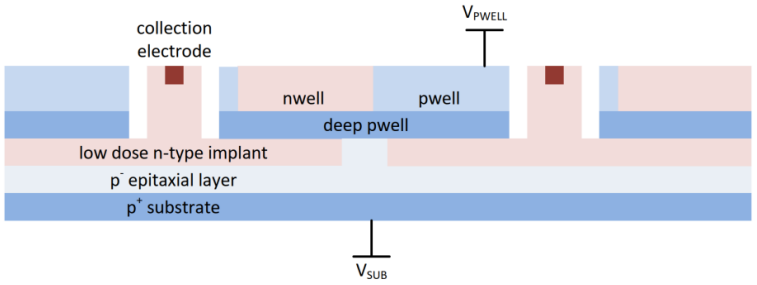


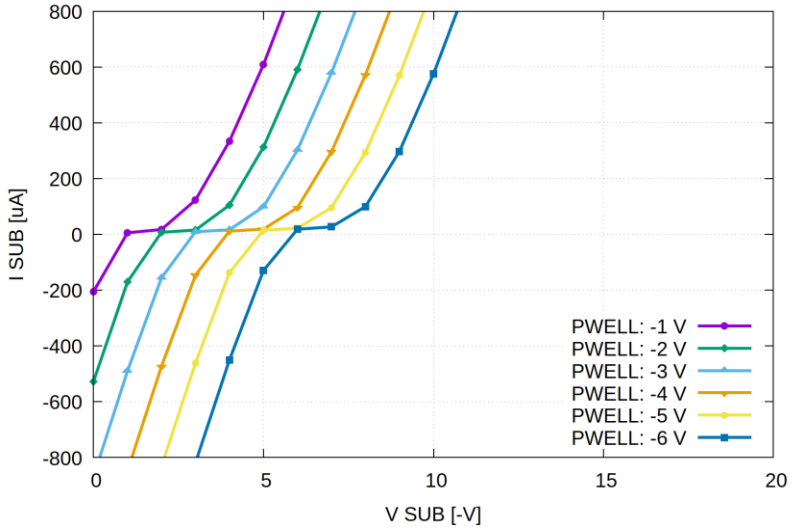


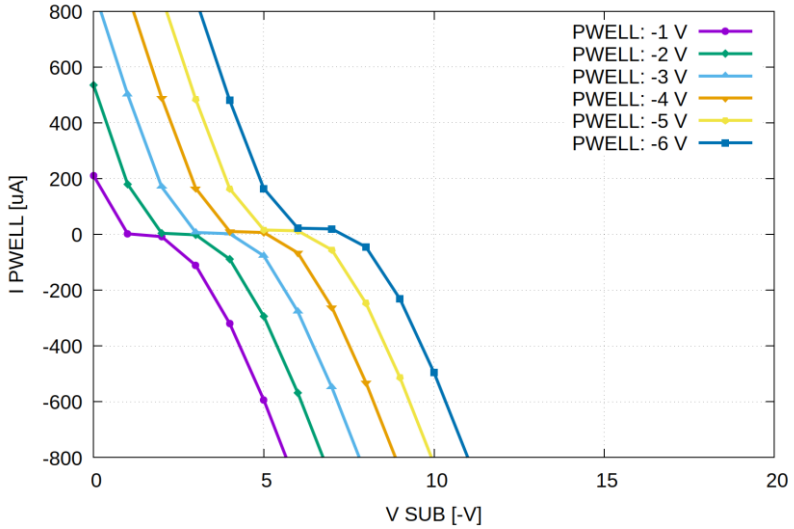


I-V characteristics

- 2nd process split: gap in N-layer
- Reduced isolation due to the gap in the N-layer
- Sensor can be operated when the SUB and PWELL nodes are biased to similar voltage

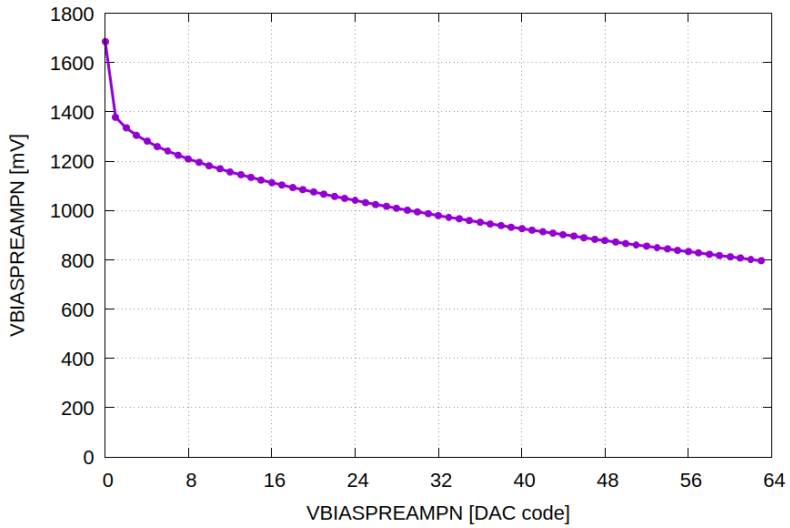


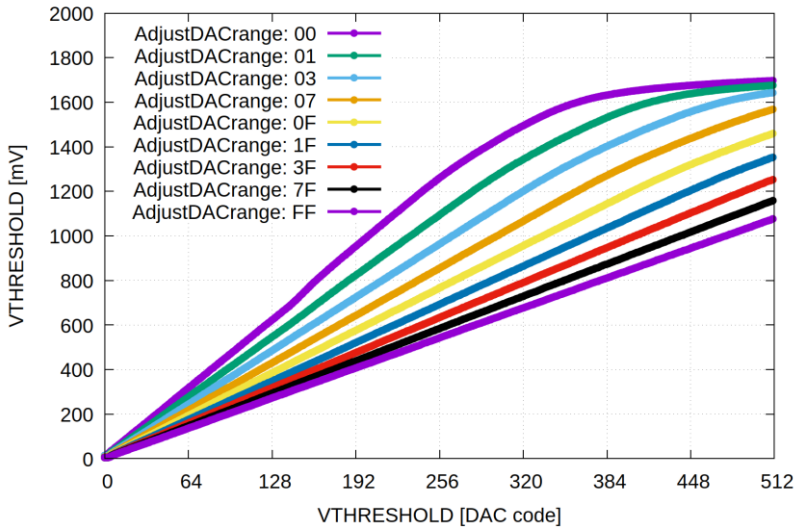




DAC scans

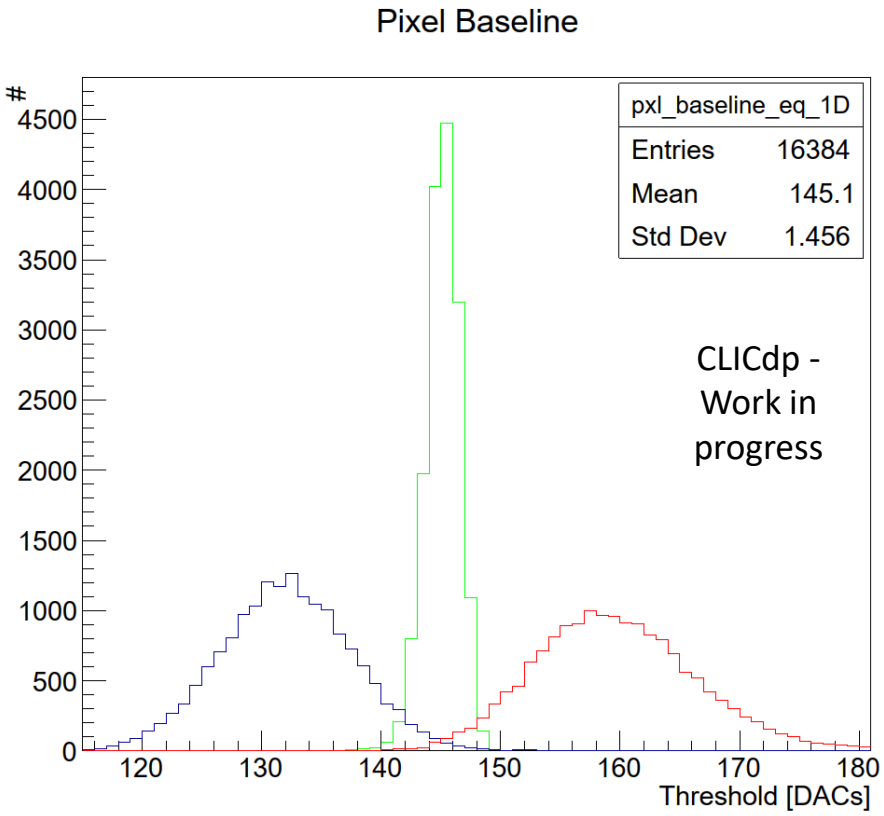
- Current and voltage DACs were scanned, confirming that they operate as expected
  - Example current DAC (left): preamplifier bias current
  - Example voltage DAC (right): threshold voltage
    - Threshold voltage scanned for different values of the register for tuning the DAC range





Threshold equalisation

- Threshold scan for lowest (blue) / highest (red) / equalised (green) local threshold tuning DAC code
- Front-end operating point not optimised
- V_{PWELL} = -2 V, V_{SUB} = -4 V, Shutter length: 4 ms
- Threshold dispersion value (1.5 DAC steps, or ~13.5 e^-) is close to the expected from simulations

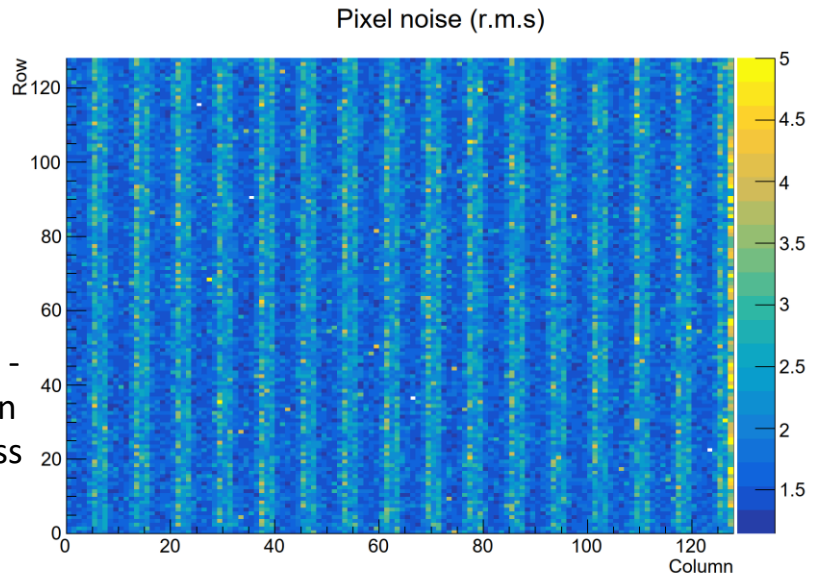


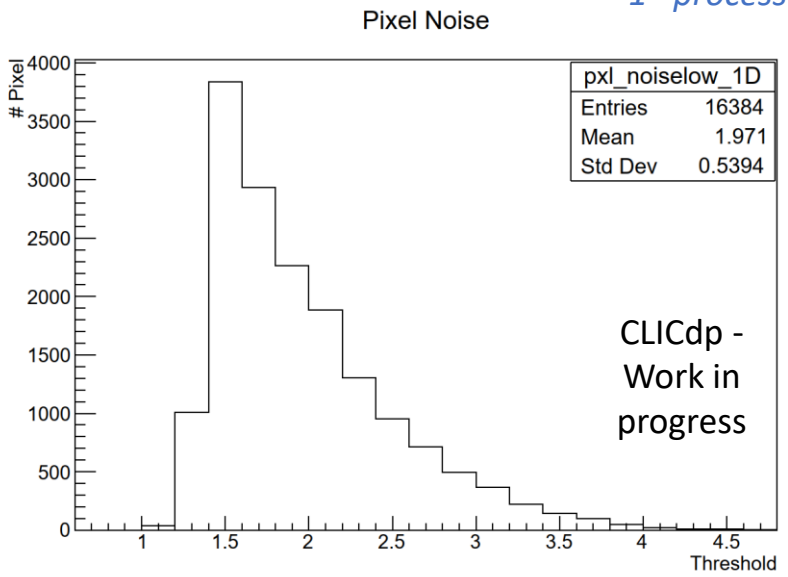
Sample from 1st process split

Noise measurements

- Noise RMS pixel map (left) and distribution (right). Plotted in threshold DAC code values
  Mean pixel noise RMS: 2 threshold DAC steps (or ~18 e^-)
- RMS of threshold DAC codes where hits have been detected during the frame (100 repetitions for each channel)
- V_{PWELL} = -2 V, V_{SUB} = -4 V, Shutter length: 400 µs
- Internal threshold DAC (9 bits) can be overwritten by an external DAC (14 bits) to achieve higher precision for this measurement.

Sample from 1st process split

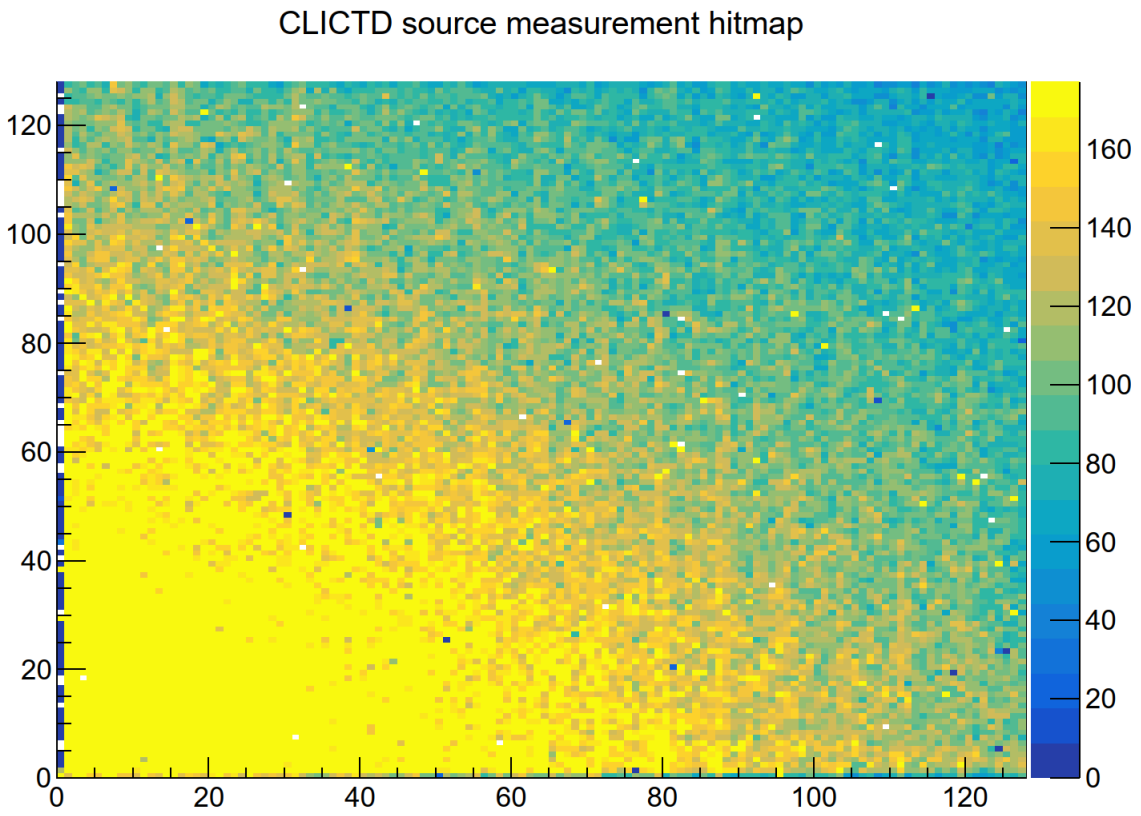




Measurement with Sr90 source

- Unequalised matrix, number of frames with one or more hits is plotted
- Global threshold set to ~240 e^- above mean baseline. Local threshold tuning DACs set to mid-range
- Front-end operating point not optimised
- V_{PWELL} = -4 V, V_{SUB} = -4 V, Shutter length: 40 ms, 10000 frames

Sample from 1st process split



CLICdp - Work in progress

Power consumption

- Power pulsing:
  - Analog front-end is set to a standby power mode between subsequent bunch trains
  - Clock is gated when the digital logic is not active

CLICdp - Work in progress

	Power ON	Standby	Average over CLIC cycle *
Analog – pixel matrix	170 mW/cm^2	2 mW/cm^2	2.25 mW/cm^2
Analog – periphery	8 mW	8 mW	8 mW
Digital – pixel matrix	240 mW/cm^2	~0.6 mW/cm^2 (standby) 100 mW/cm^2 (readout) **	2.65 mW/cm^2
Digital – periphery	35 mW	35 mW	35 mW
Total	410 mW/cm^2 + 43 mW peri.	2.6 mW/cm^2 + 43 mW (standby) 102 mW/cm^2 + 43 mW (readout)	5 mW/cm^2 + 43 mW peri.

* Calculated assuming a duty cycle of 30 µs / 20 ms,
in order to allow the front-end to be ready for detecting particles.
** Readout of a 1 cm^2 matrix, with the same scheme would take 340 µs
(assuming 1% occupancy)

- Power consumption of the analog front-end is configurable by periphery DACs and can be further optimised
- Numbers are extrapolated based on static measurements and estimates / simulations. Test of the power pulsing functionality with precise timing to be done

Summary and outlook

- The CLICTD chip:
  - Targeting at the CLIC tracker requirements
  - Designed and produced in a modified 180 nm CMOS imaging process

- First results with the chip obtained:
  - Sensor I-V characteristics indicate that the sensor can be operated at its nominal bias
  - CLICTD chip periphery (slow control, DACs) performs as expected
  - First results from the matrix readout obtained

- Next steps:
  - Characterisation of ToA / ToT performance
  - Study of the front-end operating point
  - Timing and charge sharing studies in order to compare the two process options
  - First beam test with the CLICTD chip planned for late September 2019 at DESY

Acknowledgements

This work is a combined effort between the CERN EP-ESE-ME and EP-LCD groups

Thanks to everyone who contributed to this work:

M. Campbell, T. Kugathasan, X. Llopart, W. Snoeys,
D. Dannheim, K. Dort, L. Linssen, M. Munker, S. Spannagel, T. Vanat et al.