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CLICTD: A monolithic HR-CMOS sensor chip for the CLIC silicon tracker

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The CLIC Tracker Detector (CLICTD) is a monolithic pixelated sensor chip produced in a 180nm HR-CMOS Imaging Process. The chip, designed in the context of the CLIC tracking detector study, comprises a matrix of 16×128 detector channels, each measuring $300 \times 30 \mu m^2$. To ensure prompt charge collection, each channel is segmented in eight collection diodes, each containing a separate analog front-end. A simultaneous time and energy measurement is performed in the on-channel digital logic. Simulations show a minimum detectable charge of $93e^-$ for 210mW/cm^2 (continuous operation). The main design aspects, as well as the first results from laboratory measurements are presented.

Summary

A novel monolithic pixel sensor chip, the CLIC Tracker Detector (CLICTD) chip, is presented. The chip was designed according to the requirements for the silicon tracker at the future Compact Linear Collider (CLIC). These requirements include an 8-bit Time of Arrival (ToA) measurement with 10ns time bins and a 5-bit Time over Threshold (ToT) measurement for time walk correction and precise hit spatial allocation. Other requirements involve a single point resolution of 7um along the transverse plane, a total material budget of 1-1.5% X0 per detection layer (allowing for ˜200um for the silicon layers) and an average power consumption below 150mW/cmˆ2. Taking advantage of the low duty cycle of the CLIC beam, the analog front-end can be set to a standby power mode between bunch trains to minimise the average analog power consumption (power pulsing). The digital power consumption is minimised by means of clock gating. The resulting average power consumption over the CLIC cycle is 5mW/cmˆ2 for the matrix, plus 70mW for the periphery (for 3% occupancy).

The design was implemented in a 180nm High-Resistivity (HR) CMOS imaging process, where a deep P-well is used in order to shield the on-channel electronics from the collection electrode [1]. The signal is collected with a small N-well on the P-type high resistivity epitaxial layer. The small detector capacitance helps to minimise the analog power consumption and the noise in the front-end. The epitaxial layer is fully depleted by including an additional deep N-type implant. Using a process split, additional wafers are produced with a segmented deep N-type implant to increase the lateral field and thereby to reduce the charge collection time.

The CLICTD matrix comprises 16x128 detecting cells of 300x30umˆ2. Each cell is segmented in eight collection diodes each read out by its own Charge Sensitive Amplifier (CSA) to ensure prompt charge collection. The diodes are therefore spaced by 37.5um along the long direction. Every front-end includes a CSA, a discriminator and a 3-bit local threshold tuning DAC. Simulations show a minimum detectable charge of 93e-, an in-time charge of 720e- (where the time walk remains below 10ns) for 210mW/cmˆ2 (continuous operation, without power pulsing). Binary hit information is stored for each diode, while the simultaneous 8-bit ToA and 5-bit ToT measurement is performed in the on-channel digital logic for the combined output (by means of an “OR” gate) of all eight discriminator outputs.

The slow control is based on the I2C protocol, while a serial readout at 40 MHz, with a zero suppression algorithm, is employed. The chip was verified using the Universal Verification Methodology (UVM).

Along with the main design aspects, the first laboratory measurement results with the CLICTD chip will be presented. Measurement results will include a scan of the sensor I-V characteristics, DAC scans and a test of

the slow control and readout logic. In addition, the first results on the pixel performance, using internal test pulses as well as a radiation source, will be presented.

[1] W. Snoeys et al., NIMA 871 (2017) 90-96

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