Contribution ID: **78** Type: **Oral**

Development of ultra-low power 10-bit SAR ADC in 65 nm CMOS technology

Thursday, 5 September 2019 10:15 (25 minutes)

The design and measurement results of different versions of ultra-low power fast 10-bit SAR ADC prototypes, fabricated in CMOS 65 nm technology, are presented. The prototypes use different capacitive DACs, different DAC switching schemes and different asynchronous logic. All prototypes are fully functional, achieving good linearity (with both INL and DNL below 1 LSB) and ENOB around 9.3 for sampling rates up to 60-90 MSps, depending on the ADC version. The power consumption is linear with sampling frequency and at 40 MSps it is between 450-600 uW.

Summary

In modern and future detectors for particle physics experiments a fast, ultra-low power, area-efficient Analog-to-Digital Converter (ADC) becomes an indispensable component needed to build complex multi-channel readout ASIC. This work presents the development of a 10-bit 60-90 MSps Successive Approximation Register (SAR) ADC meeting the above mentioned requirements and adapted to multi-channel implementation in readout ASICs.

A fully differential ADC architecture was chosen, comprising a pair of bootstrapped switches, a differential capacitive Digital-to-Analog Converter (DAC), a dynamic comparator, and an asynchronous dynamic control logic. A fully dynamic architecture is used to eliminate the static power while asynchronous logic eliminates a fast bit-cycling clock distribution. The implemented switching schemes (Merge Capacitor Switching and a scheme without common mode reference voltage, proposed by Sanyal and Sun) of capacitive DAC result in 93-96% switching energy reduction in comparison to conventional switching scheme. The minimal capacitor size together with a split DAC architecture was used to reduce the total DAC capacitance. Two versions of asynchronous control logic were implemented, focused either on smallest power or on fastest operation. The prototypes were fabricated in CMOS 65 nm technology, which has been proven to be a radiation hard technology. In the design some basic precautions have been taken (like not using minimum size transistors) to improve the ADC immunity to radiation damages. The ADC layout was drawn in 60 um pitch, with the length between 235-330 um, depending on the ADC version. This was done to facilitate the implementation of ADC in a multi-channel readout ASIC.

All prototypes have been tested confirming expected functionality. They achieve a good linearity with DNL and INL errors below 1 LSB and work up to 60-90 MSps sampling rates. Typically, the effective resolution ENOB of around 9.3 bits is measured at 40 MSps for input signal at 0.1 Nyquist frequency. It decreases slightly (˜0.3) when going to maximum sampling rate. Power consumption is linear with sampling rate and at 40 MSps it is around 450 uW or 600 uW for the ADC with low or standard power asynchronous control logic, respectively.

In this presentation the architecture of the developed ADCs will be discussed together with differences in implementation in different versions. The complete set of measurements showing the static and dynamic performance will be also presented.

Primary authors: MORON, Jakub (AGH University of Science and Technology (PL)); FIRLEJ, Miroslaw (AGH

University of Science and Technology (PL)); FIUTOWSKI, Tomasz Andrzej (AGH University of Science and Technology (PL)); IDZIK, Marek (AGH University of Science and Technology (PL)); SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL))

Presenter: MORON, Jakub (AGH University of Science and Technology (PL))

Session Classification: ASIC

Track Classification: ASIC