ALTIROC,
a 25 ps time resolution ASIC for ATLAS HGTD


TWEPP 2019
In the forward region, between the Inner Tracker and the End Cap of EM Calorimeter

- $2.4 < \eta < 4.0$ (120 mm < R < 640 mm), $\Delta Z = 75$ mm (+50 mm moderator)
- TID up to 9.5 MGy (SF 2.25) at R = 120 mm after 4000 fb-1 ($10^{16}$ n/cm$^2$ SF =1.5) => Ring 3.1 < $\eta$ < 4.0 replaced half the HL-LHC lifetime = 32 % of modules.

- $\sigma_t \sim 30$ ps/track at start, 50 ps/track at the end, dominated by electronic jitter and < 10% occupancy
  - Si (Low Gain Avalanche Diodes) sensors
  - 1.3 x 1.3 mm$^2$ granularity
  - 2 hits/track $\eta$< 3.2 ; 3 hits/track $\eta$> 3.2
- Use as counting detector at 40 MHz for luminosity measurements

2 disks, 2 layers/disk equipped on both sides with Low Gain Avalanche Diodes (LGAD)

Sensor overlap: 20% for $r$>320 mm and 80% for $r$<320 mm
HGTD module

- **Module** = LGAD sensor (450 PADs of 1.3 x 1.3 mm²) + 2 ASICs (225 channels/ASIC) bump bonded to sensor + **Flex** to *peripheral electronic boards* (LpGBT, DC-DC, flex connectors)
  - 2 ASICs = 2 x 2 cm x 2 cm (15x30 channels) with 1.3 x 1.3 mm² pads granularity
- **Flex**: wire bonded to sensor (bias voltage) and to ASICs (signals and power)

See Marisol Robles’ poster (144) : « Test results of a flexible printed circuit for the ATLAS HGTD »
Requirements for the ASIC

HGTD key requirement: Time resolution per track, combining multiple hits, is 30 ps at the start of lifetime to 50 ps after 4000 fb-1 => Time resolution /hit must be < 40 ps at start and 85 ps (70 ps) at the end of lifetime for the inner radius (outer radius)

Main contributors:

\[
\sigma_{\text{hit}}^2 = \sigma_{\text{Landau}}^2 + \sigma_{\text{clock}}^2 + \sigma_{\text{elec}}^2 \\
\text{with } \sigma_{\text{elec}}^2 = \sigma_{\text{Time walk}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2
\]

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum jitter ((\sigma_{\text{elec}}))</td>
<td>25 ps at 10 fC at the start of the HL-LHC and 70 to 85 ps after 4000 fb-1 for 2.5 fC</td>
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<tr>
<td>TDC contribution</td>
<td>&lt; 10 ps</td>
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<tr>
<td>Time walk contribution</td>
<td>&lt; 10 ps</td>
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<tr>
<td>TDC conversion time</td>
<td>&lt; 25 ns</td>
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- **PAD size**: 1.3 x 1.3 mm\(^2\) x 50 \(\mu\)m \(\Rightarrow\) \(C_{\text{det}} = 4\) pF
- **ASIC size and channels /ASIC**: 2x2 cm\(^2\) 225 channels/ASIC
- **Single PAD noise (ENC)**: < 1500 e- or 0.25 fC
- **Minimum threshold**: 1 fC
- **Dynamic range**: 2.5 fC to 100 fC

- **TID Tolerance**: Inner region (R<320 mm): **4.7 MGy** (Modules replaced after 2000 fb\(^{-1}\))  Worst case at R=320mm: **5.1 MGy**
  \(\Rightarrow\) ASIC designed in CMOS 130 nm

- **Voltage and Power dissipation per ASIC**: 1.2V and 300 mW cm\(^{-2}\) \(\Rightarrow\) 1.2 W/ASIC (225 ch) or **4.4 mW/channel** and 200 mW for the common part
ALTIROC1 single channel FE readout

ALTIROC1 FE integrates:

- A **preamplifier** followed by a **discriminator**: Time walk correction made with a Time over Threshold (TOT) architecture
- Two **TDC** (Time to Digital Converter) to provide digital **Hit data** = Time of Arrival (TOA) + Time Over Threshold (TOT)
  - TOA TDC: range of 2.5 ns and a bin of 20 ps (7 bits)
  - TOT TDC: range of 20 ns and a bin of 40 ps (9 bits)
- One Local memory (**SRAM**): to store the 17 bits of the time measurement (Hit data) until L0/L1 trigger (~ 1 MHz) => trigger latency = 35 µs

*Altiroc1 integrates a standalone phase shifter designed by SMU*
- \( I_d \) tuneable: \( I_d (M1) = I_{d1} \ (150 \ \mu A) + I_{d2} \) (tuneable up to 850 \( \mu A \))
- BW tuneable with \( C_p \): 1 GHz down to 200 MHz
- \( R2=25K \): for DC bias, \( R_{in} \approx 1.6 \ K\Omega \), Fall time= 2.2 \( R_{in}Cd \)
- I leakage sensor: absorbed by \( R2 \)

$$V_{out_{-pa}} = G_{pa} V_{in} = G_{pa} \frac{Q_{IN}}{C_d} \sim \alpha I_d \frac{Q_{IN}}{C_d}$$

- Noise independent of \( C_d \), depends of \( \sqrt{BW} \) and of \( 1/\sqrt{I_d} \)

$$N = G.e_n \sqrt{\frac{\pi}{2}} BW = G.e_n \sqrt{\frac{\pi}{2}} \frac{0.35}{t_{10-90\_PA}} = \frac{G.e_n}{\sqrt{2t_{10-90\_PA}}}$$

with \( e_n \) given by:

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$

- Signal rise time is the convolution of signal duration \( t_d \) and amplifier risetime \( t_{10-90\_PA} \)

$$\frac{dV}{dt} = \frac{G.Q_{in}}{C_d \sqrt{t_{10-90\_PA}^2 + t_d^2}}$$

\( e_n \) in (nV/\( \sqrt{Hz} \))

\( I_d \) (mA)

\( \sigma_t \) = \( \frac{e_n C_d}{Q_{in}} \) \( \sqrt{t_d} \)
TOA TDC Architecture (Simplified): Vernier Delay Line

TDC Power consumption $0.4 \text{ mA} \times 1.2V = 0.5 \text{ mW} @ 10\%$ occupancy

**TOA TDC**
- **Resolution:** 20 ps
- **Range:** 2.5 ns
- **7 bits**

@ Bojan Markovic, SLAC

**Simplified Block Diagram:**

- The **START** pulse comes first and initializes the TDC operation.
- The **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized.
- At each tap of the Delay Line the **STOP** signal catches up to the **START** signal by the deference of the propagation delays of cells in Slow and Fast branches of the delay line: i.e. $140\text{ps} - 120\text{ps} = 20\text{ps}$ that represents the LSB of time measurement.
- The number of cells necessary for **STOP** signal to surpass the **START** signal represents the result of TDC conversion
- Cycling configuration used in order to reduce the total number of Delay Cells.
- TDC range is equal to $128*20\text{ps} = 2.56\text{ns}$

Differential shunt capacitor voltage-controlled delay cells
TDC for TOT measurement

TDC Power consumption $0.4 \text{ mA} \times 1.2\text{V} = 0.5\text{ mW} @ 10\%$ occupancy

TOT TDC
- Resolution: 40ps
- Range: 20 ns
- 9 bits

TOT: coarse delay line (160 ps) + TOA TDC

@ Bojan Markovic, SLAC
PROTOTYPES DONE SO FAR (all CMOS 130 nm)

- **ALTIROC0**: contains only PA + discriminator – for 2x2 1x1 mm² sensors
  - Altiroc0_V1 (Dec 2016): 4 channels for 2 pF (1x1 mm² sensor) and 4 channels for 20 pF (3x3 mm² sensors), Voltage PA (=VPA) for all channels
  - Altiroc0_V2 (December 2017): 4 channels with faster VPA preamp and and 4 channels with TZ preamp. All for Cd ~ 2pF
  - Testbench and testbeam measurements

- **ALTIROC1_V1**: 5x5 complete readout channels (PA, discri, TDC, SRAM) to readout 1.3 x 1.3 mm² LGAD pixels, 15 channels with VPA, 10 with Transimpedance amplifier (TZ)
  - Testbench measurements (debug) since beg. of Dec. 2018
  - Irradiation tests

- **ALTIROC1_V2**: submitted March 2019 (CMS eng run) but thinned/diced dies received beg of July => first tests begun mid July 2019
  - Minor modifications between V1 and V2: 1.2V MOSCAPs used to filter DLL Vctrl voltages changed to 2.5 MOSCAPs to get rid of the leakage current on these nodes
  - Testbeam 19-25 August @DESY
  => measurements shown with Altiroc1_V2 are quite preliminary

Wire bonding and bump bonding done by IFAE, CNM and IHEP

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Altiroc1 layout

ZOOM of one pixel

Submission:
V1  13 June 2018, V2  March 2019

VPA: Voltage preamp
TZ: Transimpedance preamp

Measurements shown in this presentation only with VPA
SETUP for ALTIROC1 measurements

Altiroc1 die

Wire bonding @

Output 50 Ohm Single-Ended 40 MHz reference

Output 100 Ohm differential 40 MHz reference

TOT_BUSYB SMA Input

PCIe connector to ASIC board

Input 50 Ohm Single-Ended 40 MHz reference

Input 100 Ohm differential 40 MHz reference

Power: 6VDC ~ 12VDC

Dual LEMO: TOP: +3.3V Output Bottom: +3.3V Input

5V TTL OUT

5V TTL IN

Ethernet 1000BASE-X

MAC burned in the FPGA eFUSE

LED: ETH Phy Ready

LED: FPGA CLK Ready

LED: UDP RX Link Up

LED: FPGA PLL Locked

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- Injection of charge (0 fC up to 50 fC) using the ASIC internal pulser controlled by `cmd_pulse` input
- `cmd_pulse` signal generated by the FPGA, synchronous to 40 MHz clock
- **External trigger** pulse to characterize the TOT TDC alone (as well as TOA TDC)

### ALTIROC FPGA Board (C01):

- Using **SY89295UMG** as a programmable delay, the `cmd_pulse` can be delayed by software with steps ~10 ps in ~10 ns range
ALTIROC1_V2: TOA Measurements using PA+Discri

In Altiroc1_V1, LSB was 28 ps and range 1.8 ns (due to leakage in MOS filtering Cap used in the DLL): corrected in Altiroc1_V2 by replacing 1.2V MOS transistors capacitors by 2.5V MOS transistors.
ALTIROC1_V2: TOT measurement using external trigger

TOT TDC of Altiroc1_V1: range was only 5 ns. Due to a larger than expected initial pulse-width (higher parasitics) of signals circulating within the cyclic delay lines => corrected in Altiroc1_V2 with a better control the initial pulse width

**ALTIROC1_V2**

LSBc = 163 ps
LSBf = 35 ps
Range = 20 ns

Jitter = 10 ps
Measurements done on the 15 VPA channels only
Qinj=10 fC, C_d =0
*Individual tunings of the pixel TDC not done*

**VPA:** Voltage preamp
**TZ:** Transimpedance preamp
Measurements done with the internal TOA TDC

Floor (~ 13 ps) from clock, command pulse and TDC bin not subtracted

5fC, $\sigma = 36$ ps (33 ps after floor subtraction)

10fC, $\sigma = 23$ ps (19 ps after floor subtraction)

- Board 1 Ch4 Vth <= 1 fC Cd 3.5 pF
- Board 1 Ch9 Vth <= 1 fC Cd 3.5 pF

Measurements done with the internal TOA TDC

Floor (~ 13 ps) from clock, command pulse and TDC bin not subtracted

5fC, $\sigma = 36$ ps (33 ps after floor subtraction)

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- Board 1 Ch4 Vth <= 1 fC Cd 3.5 pF
- Board 1 Ch9 Vth <= 1 fC Cd 3.5 pF
Measurements done with scope as TOT TDC didn’t work properly in Altiroc1_V1
Clock tree (pulser command, clocks): good distribution for 4x4 channels

RMS = 18 ps ± 4ps

Ch8: to be checked on another ASIC

VPA: Voltage preamp
TZ: Transimpedance preamp
• Time resolution of a 2x2 x1x1 mm² LGAD array bump bonded on an Altiroc0 ASIC as a function of the discr threshold (DAC Units) before (black points) and after TW correction (red points)

Time reference given by SiPM with a time resolution = 40 ps, which has been substracted
TEST BEAM measurements with Altiroc1_V2 (19-25 Aug. 2019)

Board2 - ch 13
DAC 10bit 470

$\text{LSB} = 20 \text{ ps}$
Irradiations tests with Altiroc1_V1 (June 28- July 8, 2019)

- CERN facility, TID up to 340 Mrad

Altiroc1_V1: Internal pulser before and after 340 Mrad

\[ y = 0.8071x + 0.3038 \]

Altiroc1_V1: 10-bit DAC (Threshold) after 340 Mrad

\[ y = 0.4289x + 671.84 \]

Slope before and after irrad: - 0.4 mV/DACU
Irradiation tests with Altiroc1_V1 (June 28 – July 4, 2019)

- TOA jitter could be measured up to 23 Mrad but then water pb on the setup … => TDC didn’t work anymore

=> Measurements (after 340 Mrad) of the jitter vs Qinj performed on scope (using discrim output) and compared to measurements performed with the TDC done on the very same channel before irrad:

45 ps jitter @ Qinj=5 fC after TID to be compared with 35 ps obtained before irrad.

- Test of PLL (designed by OMEGA) used in the phase shifter after irrad. Ref clock = 40 MHz. After 340 Mrad, PLL can still lock up to 50 MHz
• ALTIROC0 and ALTIROC1 prototypes crucial to measure the analog performance, which is rather good (25 ps @ 10 fC) but still a lot of measurements to be done in particular with the sensor (testbench and testbeam)

• Still points to be understood:
  - Leakage currents in the DLL and the internal pulser

• Next steps: ALTIROC2 with 225 channels (1.3 x 1.3 mm2 LGAD pixels) to be submitted in Jan. 2020
  - Digital part quite complicated (IFAE, IHEP and LPC Clermont)
  - Analog part performance vs 2x2 cm2 ASIC
  - Plan to combine « Digital On Top » for matrix part (with an exclusion area for 1/3 of the pixel = PA + Discri + TDC) and « Analog On Top » design for off pixel electronics and the floorplan (distribution of the power supplies)
ALTIROC1 prototype (June 2018 submission)

ALTIROC1 = Second ALTIROC ASIC prototype with 25 complete FE channels to readout 5 x 5 sensor cells of 1.3 mm x 1.3 mm (6.5 mm x 6.5 mm) + Phase shifter

3 Labs involved: OMEGA (analog Part, floorplan), SLAC (Digital part: TDC and FIFO), SMU (Phase shifter)

ASIC size: 7.5 x 7 mm² taking into account the pads on the right side of the ASIC (7.5 mm) and also pads (for bias, probes ...) on the top side for debug (top pads only for this prototype version)
Voltage-Controlled Delay Cell

Differential Shunt-Capacitor Delay Cell:

- Differential architecture: reduced jitter and improved supply noise rejection.
- Additional source transistors for supply noise rejection.
- Compared to Current-Starved approach, the Shunt-Capacitor approach guarantees a more contained and linear Voltage-Delay characteristic with benefit of reducing jitter due to control voltage noise and ripple.
- The MOS diodes in parallel to MOS capacitors prevent leakage currents from altering the capacitor voltage, thus improving delay accuracy.
- Additional delay-control transistors for trimming/calibration purposes.
- Separate buffered outputs for time measurement operations.
Local FIFO 19x400 (SRAM)

SRAM word length: 19 bits
- 1 HIT bit
- 7 TOA bits
- 9 TOT bits
- 2 extra debugging bits:
  - TOA overflow bit
  - 1 extra Vernier TDC bit for TOT measurement

SRAM depth: 400 (10µs data)

Dimensions: 6.57um x 2.18um = 14.3226um^2
ALTIROC1: jitter and out_pa amplitude vs Cd Vth = 1 fC

Jitter increases with Cd as expected

Amplitude goes as 1/Cd as expected

\[ \sigma_t^J = \frac{e_n C_d}{Q_{inj}} \sqrt{t_d} \]

\[ \frac{1}{V_{out\_pa}} = \frac{C_d}{G_{pa} * Q_{inj}} + \frac{C_{parasitic}}{G_{pa} * Q_{inj}} \]
Jitter decreases with Qinj and is better for larger Vth as expected.

\[ C_d = 3.5 \text{ pF} \]

- Threshold 1 fC
- Threshold 2 fC
VPA jitter vs TZ jitter (Altiroc0_V2)
Single-channel readout in ALTIROC2