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ALTIROC1, a 25 pico-second time resolution ASIC for the ATLAS High Granularity Timing Detector (HGTD)

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ALTIROC1 is a 25-channel ASIC designed to readout the 5 x 5 matrix of 1.3 mm x 1.3 mm x 50 µm Low Gain Avalanche Diodes (LGAD) of the ATLAS HGTD detector. The targeted combined time resolution of the sensor and the readout electronics is 50 ps/hit. Each ASIC channel integrates a RF preamplifier followed by a high speed discriminator and two TDCs for Time-of-Arrival and Time-Over-Threshold measurements as well as a local memory. This front-end must exhibit an extremely low jitter noise while keeping a challenging power consumption of less than 4.5 mW. Detailed measurements will be presented.

Summary

The expected increase of the particle flux at the high luminosity phase of the LHC (HL-LHC) will have a severe impact on jet reconstruction performance in the forward region.
A High Granularity Timing Detector is proposed in front of the Liquid Argon end-cap calorimeters for pile-up mitigation and for bunch per bunch luminosity measurements. This detector will cover the pseudo-rapidity range of 2.4 to about 4.0 and will be made of two double sided layers of Low Gain Avalanche Detectors (LGAD) with 1.3 x 1.3 mm2 pads. The aim is to provide a precision timing information for minimum ionizing particle with a resolution better than 50 ps over the entire detector lifetime.

To preserve the intrinsic time resolution of LGAD sensors (25 ps before irradiation for gain larger than 20), the front-end ASIC, ALTIROC, must exhibit an electronics jitter smaller than 25 ps for a MIP signal (10 fC for a LGAD gain of 20 and a capacitance of 3.4 pF). The impact of the 500 ps time-walk after correction using the Time Over Threshold (TOT) measurement, must remain negligible. The ASIC FE electronics is designed to cope with the high radiation levels (up to 4.5 MGy), while keeping a challenging power dissipation smaller than 4.5 mW/readout channel.

ALTIROC1 has been designed in CMOS 130nm to readout a 5x5 LGAD matrix with a complete on-pixel readout. The analog part consists of a 1 GHz RF preamplifier followed by a high speed discriminator, which are both critical elements for the overall electronics time performance. Each discriminator is followed by a TOA (Time-of-Arrival) and a TOT (Time-Over-Threshold) TDC as well as by a SRAM memory to store the digitized data.
The TOA is digitized over 7 bits with a bin of 20 ps and is done within a 2.5 ns window centred on the bunch crossing. A Vernier delay line configuration has been chosen to achieve the 20 ps quantisation step. The conversion is initiated only upon signal detection, enabling power saving.
The TOT measurement is digitized over 9 bits with a bin of 40 ps. The TDC employs an additional coarse delay line for extending the range to 20 ns while the Vernier delay line (identical to the one used in TOA TDC) provides the high resolution of 40 ps.
The total power consumption for both TDCs is 1.1 mW/channel assuming a maximal channel occupancy of 10%.
The memory is also custom designed to minimize the power dissipation to less than 0.5 mW/ch with a 10% occupancy. It has a width of 19 bits and a depth of 400 columns to provide the 10 µs L0 latency.

A first prototype, ALTIROC1_V1, was received in November 2018. It exhibits good performance, with a jitter of 25 ps using the full chain and a detector capacitance of 3.5 pF. A second prototype with minor modifications,

ALTIROC1_V2, is expected in June 2019.
The overall test bench characterization obtained with the ASIC alone as well as measurements performed with a bump-bonded sensor will be presented.

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