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Depleted monolithic active pixel prototypes for MIP detection and photon counting

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The LF2 is a depleted MAPS prototype chip produced in the LFoundry 150 nm HV-CMOS process on 500 Ωcm and 1900 Ωcm wafers. The chip includes two monolithic matrices. One matrix of 40 rows x 78 columns contains 50 x 50 µm2 pixels each with a charge sensitive amplifier, a shaper, and a discriminator, which are readout by a digital block with FE-I3 column drain architecture. A 26 x 52 photon counter matrix of 75 x 75 µm2 pixels each with a 16-bit counter completes the LF2. Testbench measurements, including charge collection, have been carried out and will be presented.

Summary

The ATLAS and RD50 collaborations have been investigating the use of depleted Monolithic Active Pixel Sensors (DMAPS) for HEP experiments. This technology could offer a cost effective solution for the pixel and strip vertex detectors, where the radiation requirements are not exceedingly high, replacing the traditional hybrid solution. Furthermore, photon counting DMAPS could also be an interesting technology for various imaging applications.

The LF2 is a depleted MAPS prototype chip produced in 2018 in the LFoundry 150 nm HV-CMOS process on 500 Ωcm and 1900 Ωcm wafers by the collaboration of IFAE, University of Liverpool, University of Geneva and KIT with the support of RD50. The ASIC includes two monolithic matrices which are completely independent and only share the substrate: a tracking pixel detector and a photon counting device. Both matrices integrate analog and digital readout electronics. The sensor is implemented by means of a p-substrate/deep n-well junction. The p-substrate is biased at a negative voltage to create a depleted volume. The main components of the analog readout electronics, very similar in both matrices, are a sensor bias circuit based on a high ohmic resistor, a charge sensitive amplifier, a source follower, filter and a CMOS comparator with a local 4-bit DAC to compensate for offset variations. Each pixel also includes an injection circuit to test the readout electronics. With respect to the digital readout electronics, the photon counting array contains a 16-bit counter while in the tracking matrix the circuits follow an FE-I3 readout approach. The analog and digital readout electronics are embedded inside the pixel sensitive area in both matrices.

The readout of the tracking matrix is asynchronous, zero suppressed and triggerless. The matrix is handled by a control unit that reads sequentially the content of each EOC cell at 40MHz. The data are passed to 2 serializers and transmitted off-chip at a speed of up to 320 MHz through LVDS pads. The readout of the photon counting matrix is simple and not conceived for high speed, only to test the monolithic concept. Pixels are read individually. The content of the 16-bits counter of the accessed pixel is loaded in parallel to a 16-bits shift register at the periphery. Then, the data is serialized at a maximum speed of 40MHz.

The LF2 ASICs were received in 2018 and a readout system, based on the Xilinx ZC706 FPGA board, was developed. The initial results of the table-top characterization of the devices will be presented, including charge collection studies with radiation sources and Transient Current Technique measurements.

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